SiI9125 HDMI Receiver with Deep Color Outputs

Data Brief

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Further Information

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Introduction

The SiI9125 HDMI Receiver with Deep Color Outputs is a second-generation dual-input High Definition Multimedia Interface (HDMI®), HDCP, and DVI compliant receiver. It is software-compatible with the SiI9133 receiver with Deep Color outputs as well as the SiI9033 receiver. Digital televisions that can display 10- or 12-bit color depth can now provide the highest quality protected digital audio and video over a single cable. The SiI9125 device can receive Deep Color video up to 12-bit, 1080p @ 60 Hz. Backward compatibility with the DVI 1.0 specification allows HDMI systems to connect to existing DVI 1.0 hosts, such as HD set-top boxes and PCs.

The latest generation Integrated Transition Minimized Differential Signaling™ (TMDS™) core runs at 25–225 MHz and passes all HDMI compliance tests.

The SiI9125 receiver is pre-programmed with High-bandwidth Digital Content Protection (HDCP) keys and contains an integrated HDCP decryption engine for receiving protected audio and video content. This set of keys helps reduce programming overhead, lowers manufacturing costs, and provides the highest level of security.

The specialized audio and video processing contained in the receiver can add HDMI capability to earlier-generation consumer electronics. Efficient color space conversion receives RGB video data and delivers either standard-definition or high-definition YCbCr formats.

This receiver supports high end audio systems. An industry standard I^{2}S port allows direct connection to low cost audio DACs at up to 192 kHz. Audio down-sampling allows the device to share the audio bus with a high-sample-rate audio DAC while down-sampling audio for an attached display supporting only lower rates.

The device provides flexible power management.

Digital Video Interface

- automatic video mode configuration simplifies firmware design
- 36-bit RGB/YCbCr 4:4:4
- 16/20/24-bit YCbCr 4:2:2
- 8/10/12-bit YCbCr 4:2:2 (ITU BT.656)
- 12/15/18-bit Digital Multimedia Output (DMO) RGB/YCbCr 4:4:4 (clocked with rising and falling edges)
- color space conversion for both RGB-to-YCbCr and YCbCr to RGB (both 601 and 709)
- true 12-bit accurate data using 14-bit processing

Digital Audio Interface

- sends and receives 2-channel digital audio up to 192 KHz
- I^{2}S output supports up to 2-channel 192 kHz digital audio
- The S/PDIF port supports 192 kHz compressed streams
- S/PDIF output supports PCM, Dolby Digital, and DTS
- IEC60958 or IEC61937 compatible
- 2:1 and 4:1 down-sampling to handle 96 kHz and 192 kHz audio streams

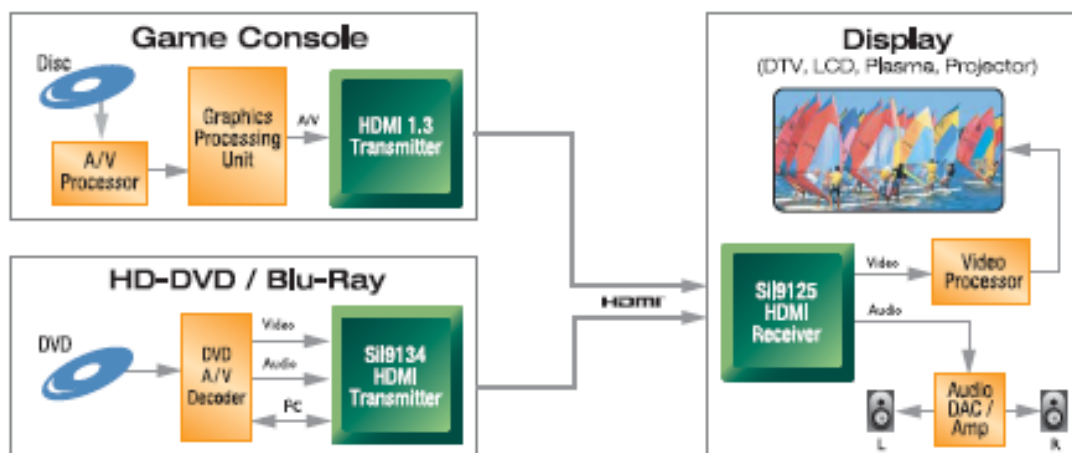## Package

- 20 mm x 20 mm 144-pin TQFP package with an ePad™

Figure 1. Typical Application

Comparing SiI9125 with SiI9133 and SiI9023

Table 1 summarizes the functional differences among the SiI9023/9025, the SiI9133, and the SiI9125 receivers.

Table 1. Summary of New Features

Feature	SiI9023/9025	SiI9133	SiI9125
HDMI Input Connections			
TMDS Input Ports	2	2	2
Color Depth	8-bit	8/10/12-bit	8/10/12-bit
DDC Input Ports	2	2	2
Maximum TMDS Input Clock	165 MHz	225 MHz	225 MHz
Output Ports			
Digital Video Output Ports	1	1	1
Maximum Output Pixel Clock	165 MHz.	165 MHz.	165 MHz.
Maximum Output Bus Width	24	36	36
Analog Video Output Ports	0	0	0
S/PDIF Output Ports	1	1	1
I^2S Output	1	4	1
Video Processing			
Color Space Converter	RGB to/from YCbCr	RGB to/from YCbCr	RGB to/from YCbCr
Pixel Clock Divider	0.25, 0.5	0.25, 0.5	0.25, 0.5
Digital Video Bus Mapping	swap Cb, Cr pins	swap Cb, Cr pins	swap Cb, Cr pins
Maximum Audio Sample Rate (Fs)			
2-channel (I^2S or S/PDIF)	192 kHz	192 kHz	192 kHz
8-channel (I^2S)	N/A	192 kHz	N/A
High Bit Rate Audio Support Compressed DTS-HD and Dolby True-HD	No	No	No
Other Features			
MCLK Generation	No external connection required.	No external connection required.	No external connection required.
HDCP Repeater Support	No	Not Used	No
Interlaced Format Detection Pin	Yes	Yes	Yes
TMDS R$_{EXT\_SWING}$	Not Used	Not Used	Not Used
Package	144-pin TQFP ePad	404-pin BGA w/Heat Slug	144-pin TQFP ePad

Pin Diagram

Figure 2 shows the SiI9125 pin assignments of the receiver. Pin names are generalized by type for this document. The list below the diagram describes the purpose of each type. The package is a 20 mm x 20 mm 144-pin TQFP with an ePad.

Figure 2. Pin Diagram

TMDS0/1 -- TMDS Port-Specific Signals
DDC0/1_BUS -- DDC Port-Specific Bus, OD, 5-V Tolerant
SIGx_0/1_LVTTL_O -- TMDS Port Detect, 5-V Tolerant
SIG0/1_LVTTL_I -- TMDS Port Power Signal, 5-V Tolerant
VIDEO_IF -- Video Data Output Interface, 3.3V
CLK_LVTTL_O -- Clock Signal, Output

CLK_LVTTL_I -- Clock Signal, 5-V Tolerant, Input
AUDIO_IF -- Audio Output Interface, 3.3V
I2C_BUS -- I2C Bus, 5-V Tolerant
I2C_BUS_CTL -- I2C Bus Control
CHIP_EN -- Chip Enable, 3.3V
RSVD -- Reserved
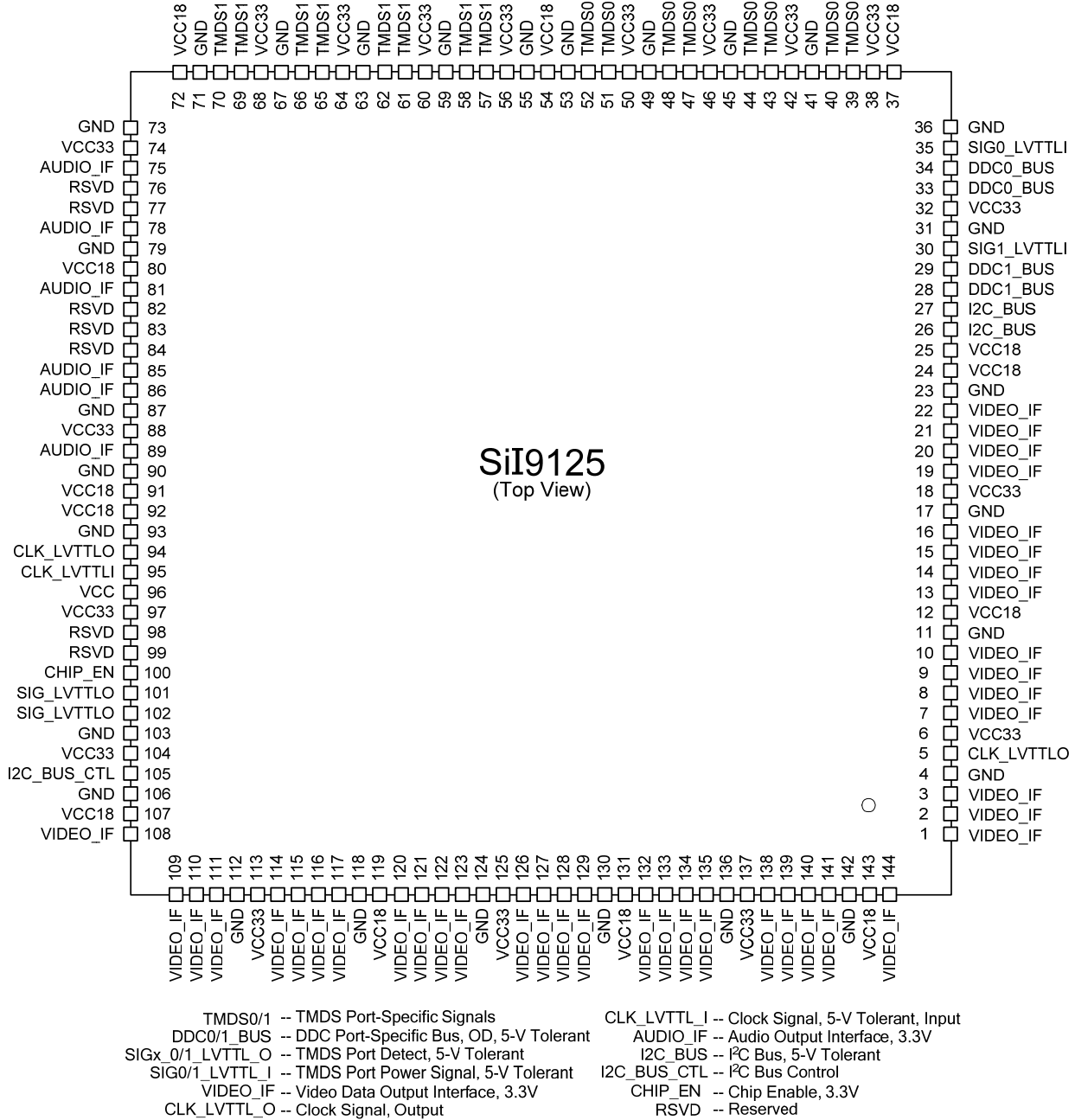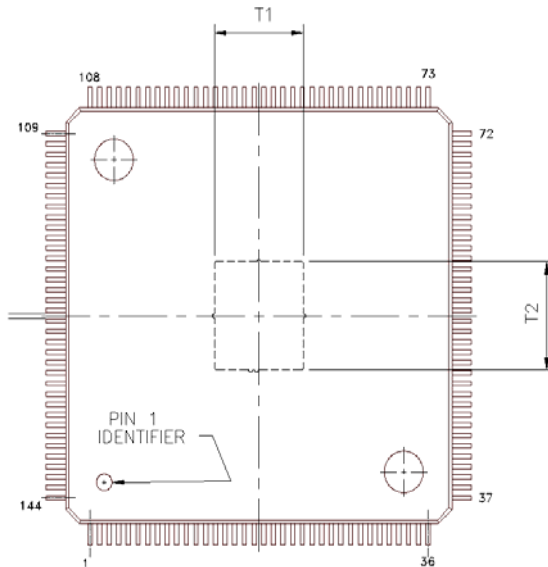
Packaging

ePad Enhancement

The SiI9125 receiver is packaged in a 144 pin TQFP package with an ePad™. The ePad dimensions are shown in Figure 3.

ePad Dimensions: Amkor and SPIL

Item	Description	Typ	Max
T1	ePad height	4.60	4.64
T2	ePad width	5.20	5.24

ePad Dimensions: ASE

Item	Description	Typ	Max
T1	ePad height	5.25	5.29
T2	ePad width	5.25	5.29

All dimensions are in millimeters.

The ePad is centered on the package center lines. The measurement tolerance is ±0.04 mm for all manufacturers. The ePad tab dimensions may vary.

A clearance of at least 0.25 mm should be provided on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid the possibility of electrical shorts.

Silicon Image recommends that the ePad be soldered to the PCB and electrically grounded on the PCB. The ePad must not be connected to any other voltage level.

Figure 3. ePad Diagram

PCB Layout Guidelines

PCB layout designers should refer to Silicon Image application note *PCB Layout Guidelines: Designing with Exposed Pads* (SiI-AN-0129) for basic design guidelines when designing with thermally enhanced packages using the Exposed Pad.

Package Dimensions
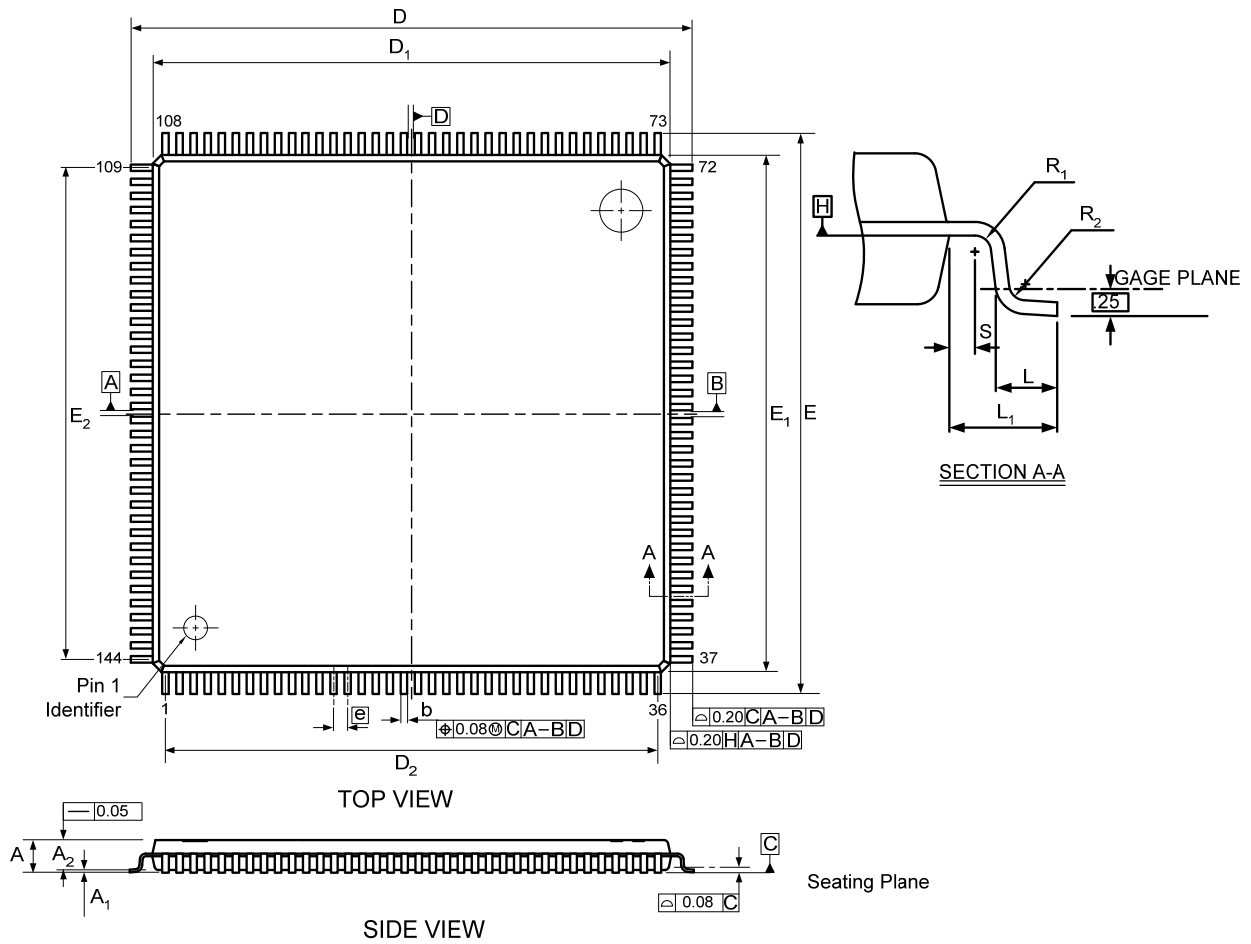
JEDEC Package Code MS-026-AFB

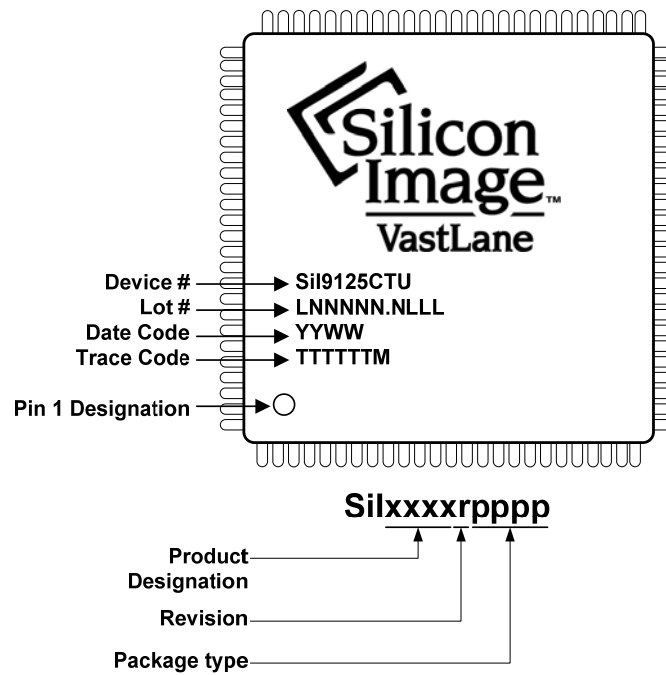| Item	Description	Min	Typ	Max		Item	Description	Min	Typ	Max
A	Thickness	1.00	1.10	1.20		b	Lead width	0.17	0.22	0.27
A1	Stand-off	0.05	0.10	0.15		C	Lead thickness	0.09	—	0.20
A2	Body thickness	0.95	1.00	1.05		e	Lead pitch	0.50 BSC		
D	Footprint	22.00 BSC				L	Lead foot length	0.45	0.60	0.75
E	Footprint	22.00 BSC				L_1	Total lead length	1.00 REF		
D_1	Body size	20.00 BSC				R_1	Lead radius, inside	0.08	—	—
E_1	Body size	20.00 BSC				R_2	Lead radius, outside	0.08	—	0.20
D_2	Lead Row Width	17.5 BSC				S	Lead horizontal run	0.20	—	—
E_2	Lead Row Width	17.5 BSC								

Dimensions in millimeters.

Overall thickness A = A1 + A2.

Figure 4. Package Diagram

Marking Specification

Drawing is not to scale and pin count shown is representative. Refer to specifics in Figure 5 on page 5.

Device # → SiI9125CTU
Lot # → LNNNNN.NLLL
Date Code → YYWW
Trace Code → TTTTTTM

Pin 1 Designation →

SiIxxxxrpppp

Product Designation
Revision
Package type

The universal package may be used in lead-free and ordinary process lines.

Figure 5. Marking Diagram

Legend	Description
LNNNNN.NLLL	Lot number
YY	Year of manufacture
WW	Week of manufacture
TTTTTT	Trace code
M	Maturity code

Ordering Information

Production Part Numbers:

TMDS Input Clock Range	Part Number
25–225 MHz	SiI9125CTU

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