SiI9187B HDMI Port Processor

Data Brief

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Introduction

The SiI9187B HDMI Port Processor is the second generation of HDMI® devices that support the HDMI Specification. With four HDMI inputs and a single output, the SiI9187B port processor enhances the functionality of digital TVs using single system on a chip (SoC) solutions with integrated HDMI receivers. The port processor provides a simple, low-cost method of retransmitting digital audio and video to give consumers a truly all-digital experience. Built-in backward compatibility with DVI 1.0 allows HDMI systems to connect to any DVI 1.0 source.

Features

The SiI9187B device brings cutting edge innovations, such as:

- Enhanced cable equalization for long cable support, even at Deep Color resolutions that enables the SiI9187B device to work with noisy signals and many sources, making the sink devices highly interoperable
- Integrated EDID and CEC functions
- Improved ESD protection on all signals connected to the HDMI connector.

HDMI Inputs and Output

- Four HDMI input ports and single output port
- HDMI, HDCP, and DVI compatibility
- TMDS™ cores run at 25–225 MHz
- Supports video resolutions up to 1080p, 60 Hz, 12-bit or 720p/1080i, 120 Hz, 12-bit.

Control Capability

- Consumer Electronics Control (CEC) interface incorporates an HDMI-compliant CEC I/O and an integrated CEC Programming Interface (CPI); these simplify design and lower cost and software overhead
- Integrated EDID and DDC support for 4 HDMI/DVI ports and 1 VGA port with a 256-byte NVRAM shared between ports that loads into separate 256-byte SRAM for each of 5 ports
- Individual control of Hot Plug Detect (HPD) for each of the 4 HDMI/DVI ports
- TPWR (TMDS clock detect) output to help speed soft mute of audio while plugging and unplugging cables
- Controllable by the local I^2C bus.

Power Management

- Flexible power management provides extremely low standby power consumption
- Standby power can be supplied from a separate +3.3 V or 5 V standby power pin
- Port power only can be used to read EDID
- Single power 3.3-V source
- Integrated 5 V to 3.3 V Voltage regulator.

Package

- 72-pin, 10 mm x 10 mm, 0.5 mm pitch QFN package with enhanced ePad™.

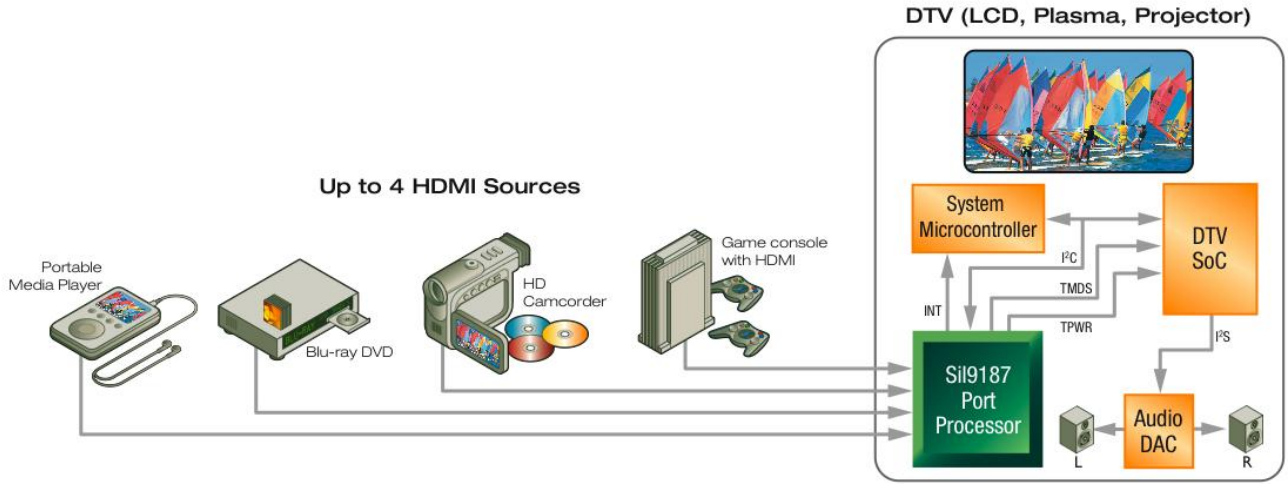

Figure 1. Typical Application of SiI9187B HDMI Port Processor

Pin Diagram

Figure 2 shows the pin diagram for the SiI9187B port processor. Pin names are generalized by type for this document. The list below the diagram describes the purpose of each type.

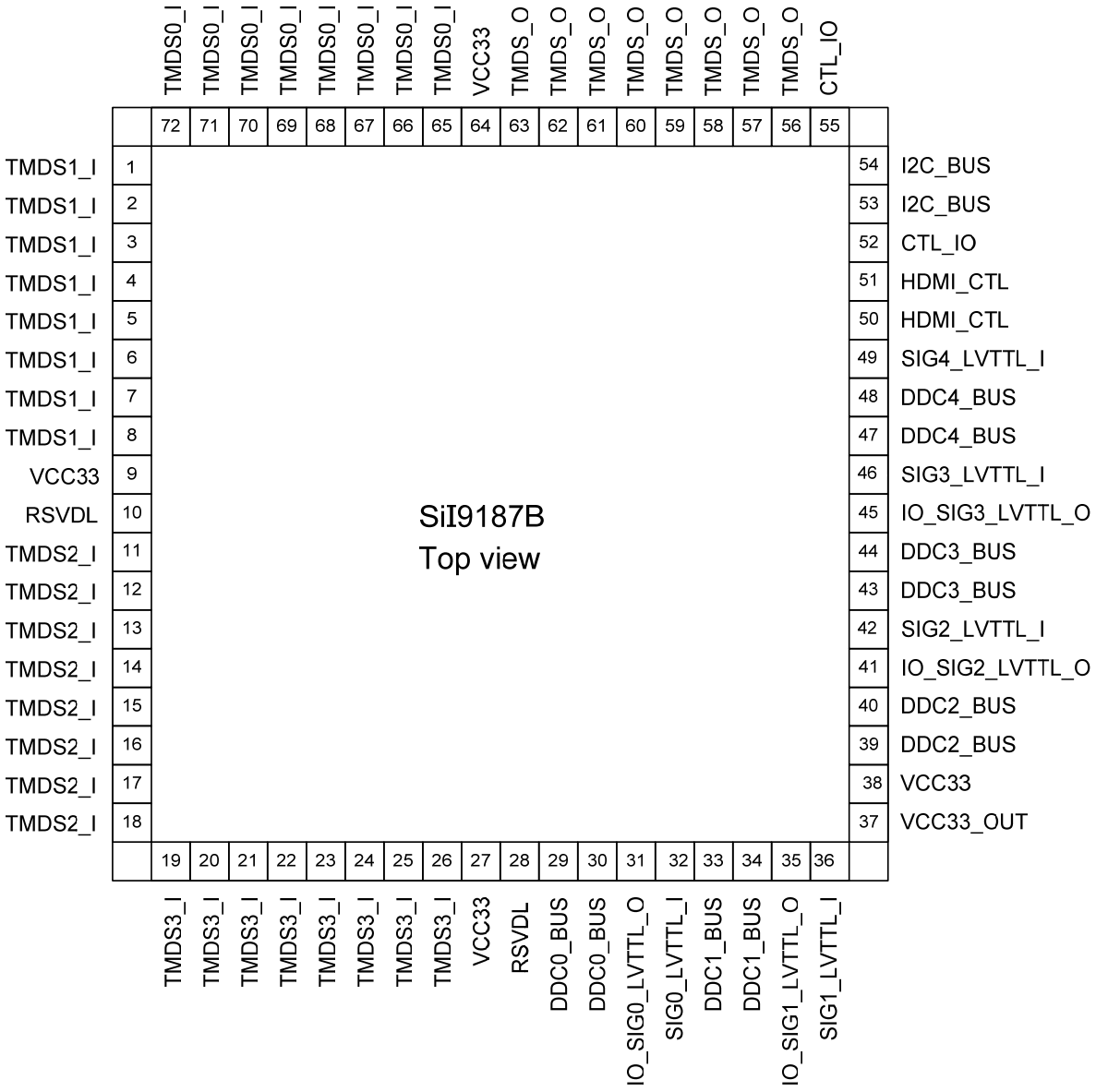

Figure 2. Pin Diagram (Top View)

Package Information

ePad Requirements

The SiI9187B HDMI Port Processor is packaged in a 72-pin 10 mm x 10 mm QFN package with an ExposedPad™ (ePad) that is used for the electrical ground of the chip and for improved thermal transfer characteristics. The ePad dimensions are 4.7 mm x 4.7 mm with a tolerance of ±0.15 mm. Soldering the ePad to the ground plane of the PCB is ***required*** to meet package power dissipation requirements at full speed operation and to connect the chip circuitry to electrical ground. A clearance of at least 0.25 mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid electrical shorts.

The thermal land area on the PCB can use thermal vias to improve heat removal from the package. These thermal vias can double as ground connections, attaching internally in the PCB to the ground plane. An array of vias can be designed into the PCB beneath the package. For optimum thermal performance, Silicon Image recommends that the via diameter be 12 to 13 mils (0.30 to 0.33 mm) and the via barrel be plated with 1-ounce copper to plug the via. This plating helps avoid solder wicking inside the via during the soldering process, which can result in voids in solder between the exposed pad and the thermal land. If the copper plating does not plug the vias, the thermal vias can be tented with solder mask on the top surface of the PCB to avoid solder wicking inside the via during assembly. The solder mask diameter should be at least 4 mils (0.1 mm) larger than the via diameter.

Package stand-off is also a consideration. For a nominal stand-off of approximately 0.1 mm the stencil thickness of 5 to 8 mils should provide a good solder joint between the ePad and the thermal land.

Figure 3 on the next page shows the package dimensions of the SiI9187B package.

Package Dimensions

These drawings are not to scale.

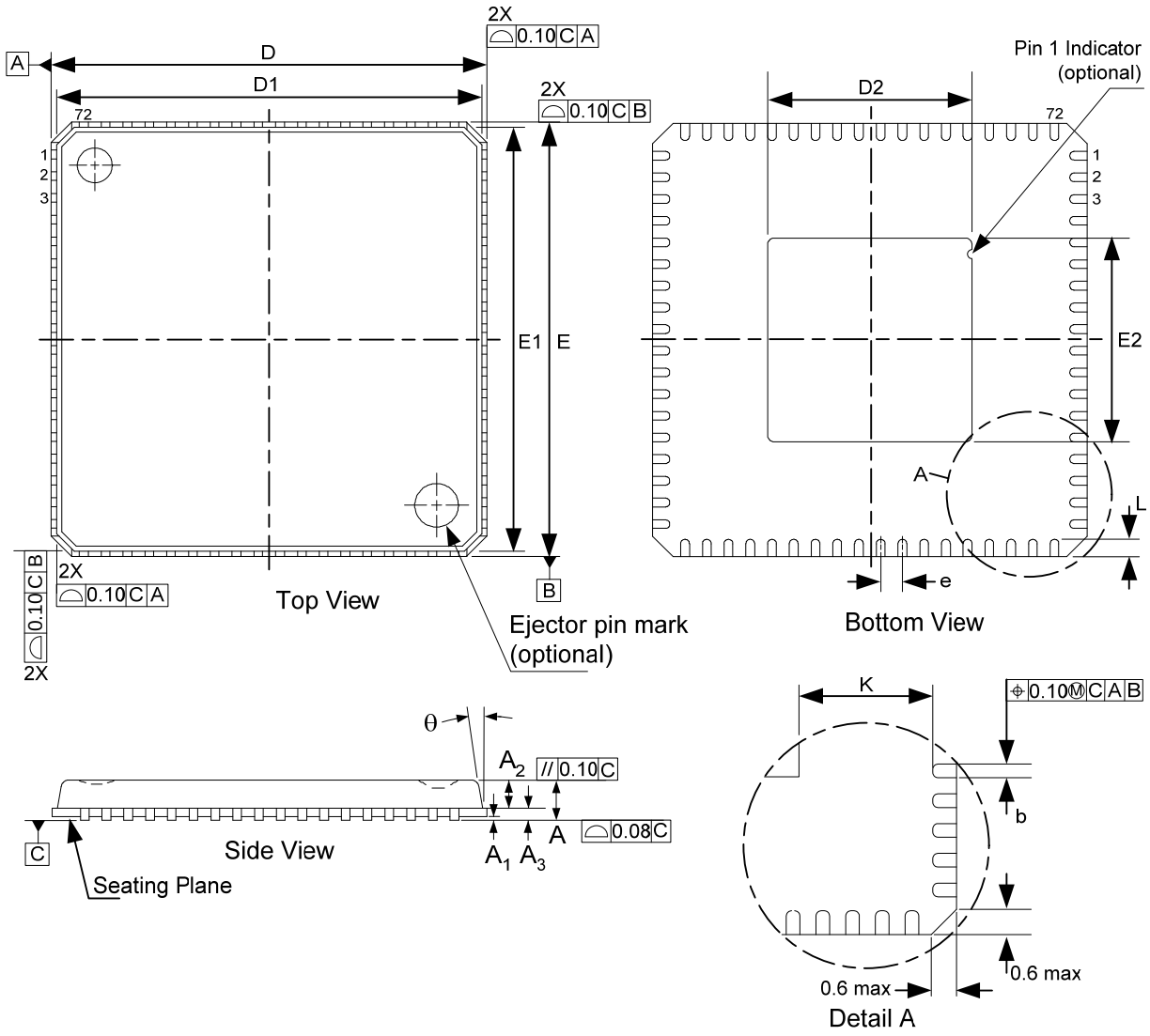

Figure 3. Package Diagram
JEDEC Package Code MO-220

Item	Description	Min	Typ	Max
A	Thickness	—	0.85	0.90
A1	Stand-off	0.00	0.01	0.05
A2	Body thickness	—	0.65	0.70
A3	Base thickness		0.20 REF	
D	Footprint		10.00 BSC	
E	Footprint		10.00 BSC	
D1	Body size		9.75 BSC	
E1	Body size		9.75 BSC	

Item	Description	Min	Typ	Max
D2	ePad size	4.55	4.70	4.85
E2	ePad size	4.55	4.70	4.85
b	Plated lead width	0.18	0.23	0.30
e	Lead pitch		0.50 BSC	
K	ePad-to-pin clearance	0.20	—	—
L	Lead foot length	0.30	0.40	0.50
θ	Lead foot angle	—	—	14°

Marking Specification

This drawing is not to scale.

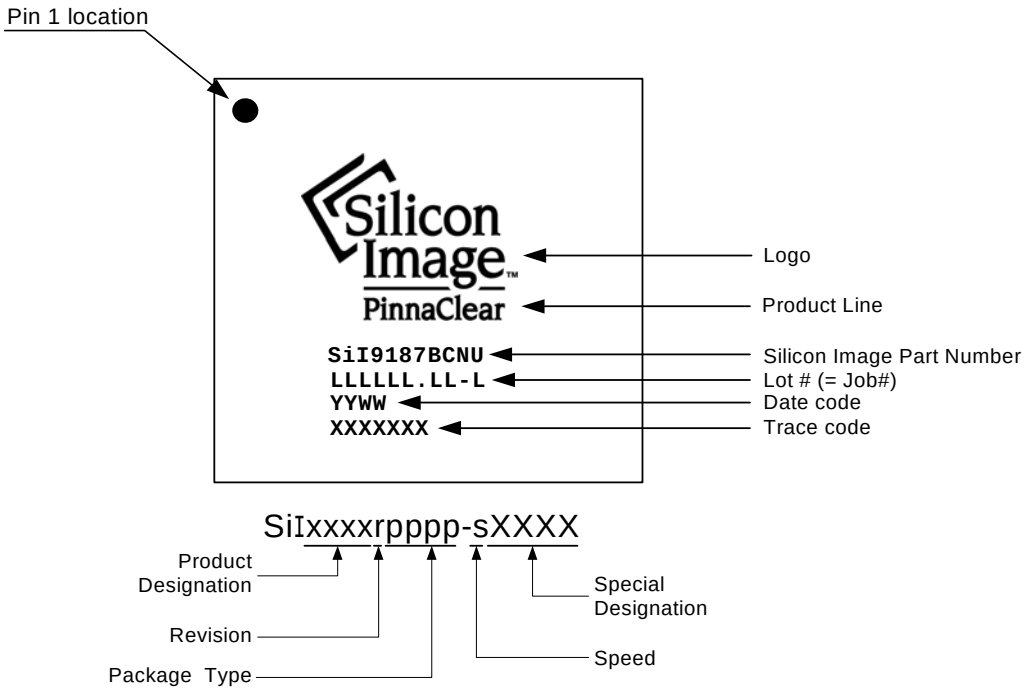

Figure 4. Marking Diagram

Ordering Information

Production Part Numbers:

Device	Part Number
Standard	SiI9187BCNU

The universal package may be used in lead-free and ordinary process lines.

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