



# **SiI9233A HDMI Receiver with Repeater, Multi-channel Audio, and Deep Color**

## **Data Sheet**

SiI-DS-1061-D

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# 1. General Description

The Lattice Semiconductor SiI9233A HDMI Receiver with Repeater, Multi-channel Audio, and Deep Color is a 4-port HDMI® receiver device. AV receivers that connect to DTVs displaying 10/12-bit color depth can now provide the highest quality protected digital audio and video, including common 3D formats up to 12-bit, 1080p at 24 Hz resolution. The receiver supports Deep Color video up to 12-bit, 1080p at 60 Hz. Efficient color space conversion receives RGB or YCbCr video data and sends either standard-definition or high-definition RGB or YCbCr formats.

The SiI9233A receiver supports the extended gamut YCC or xvYCC color space, described in the IEC 61966-2-4 specification, that supports approximately 1.8 times the number of colors as the RGB color space. The xvYCC color space also makes full use of the range on the standard 8-bit resolution per pixel.

The SiI9233A receiver device is pre-programmed with High-bandwidth Digital Content Protection (HDCP) keys; this helps reduce programming overhead and lowers manufacturing costs.

An integrated Extended Display Identification Data (EDID) block stored in non-volatile memory (NVM) can be programmed at the time of manufacture using the local I<sup>2</sup>C bus. On-board RAM can also be loaded with EDID data from the system microcontroller during initialization if the NVM is not used. The EDID is reflected on the four HDMI ports through the DDC bus. Flexibility allows mixing different EDID formats in an application. This feature can eliminate up to four EDID ROMs while also saving board space.

Flexible power management provides extremely low standby power consumption; standby power can be supplied from an HDMI 5 V signal or from a separate standby power pin. If the NVM stores the EDID, only the 5 V power from the source device is needed to read the EDID.

## 1.1. Inputs

- Four HDMI/DVI-compatible ports
- TMDS™ core runs at 25 MHz – 225 MHz

## 1.2. Digital Video Output

- xvYCC to extended RGB
- 36-bit RGB / YCbCr 4:4:4
- 16/20/24-bit YCbCr 4:2:2
- 8/10/12-bit YCbCr 4:2:2 (ITU BT.656)
- True 12-bit accurate output data using an internal 14-bit wide processing path
- Programmable drive strength from 2 mA to 14 mA

## 1.3. Digital Audio Interface

- DTS-HD and Dolby® TrueHD high bit rate audio
- I<sup>2</sup>S output with 4 data signals for multi-channel formats and flexible, programmable channel mapping
- S/PDIF output supports PCM, Dolby® Digital, DTS digital audio transmission with a 32 kHz – 192 kHz F<sub>s</sub> sample rate
- Intelligent audio mute capability avoids pops and noise with automatic soft mute and unmute
- IEC60958 or IEC61937 compatible

## 1.4. Control

- Consumer Electronics Control (CEC) interface incorporates an HDMI CEC I/O and an integrated CEC Programming Interface (CPI)
- Automatic Feature Abort response for unsupported commands and automatic message retry on transmit

## 1.5. Package

20 mm × 20 mm 144-pin TQFP package with exposed pad (ePad)

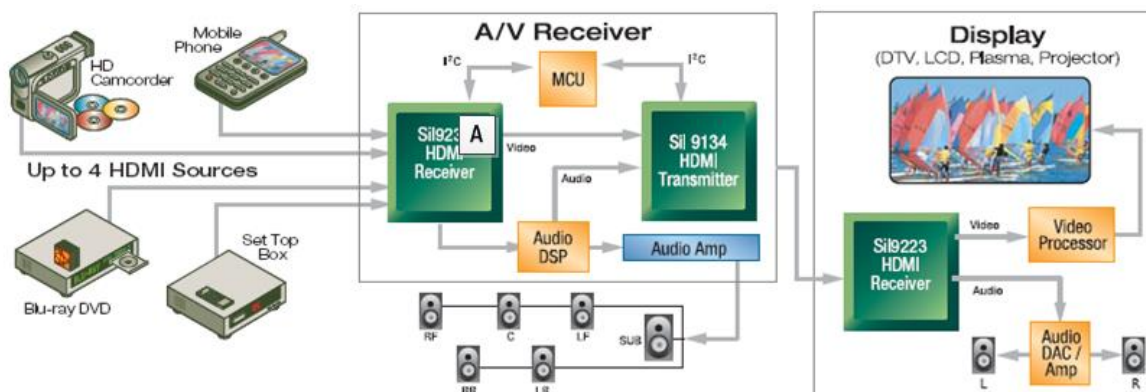


Figure 1.1. Typical Application

## 2. System Applications

The SiI9233A receiver device is designed for digital televisions that require support for HDMI Deep Color. The device allows receipt of 10/12-bit color depth up to 1080p resolutions. A single receiver provides four HDMI input ports. The video output interfaces to a video processor and the audio output can interface directly to an audio DAC or an audio DSP for further processing as shown in [Figure 1.1](#) on the previous page.

## 3. Comparing Features of Lattice Semiconductor Receiver Devices

[Table 3.1](#) compares the features of the SiI9127A, SiI9125, SiI9135A, SiI9223A, and SiI9233A receiver devices.

**Table 3.1. Comparison of Lattice Semiconductor Receiver Devices**

Feature	SiI9125	SiI9127A	SiI9135A	SiI9223A	SiI9233A
<b>HDMI Input Connections</b>					
TMDS Input Ports	2	2	2	4	4
Color Depth	8/10/12-bit				
DDC Input Ports	2	2	2	4	4
Maximum TMDS Input Clock	225 MHz				
<b>Video Output</b>					
Digital Video Output Ports	1	1	1	1	1
Maximum Output Pixel Clock	165 MHz				
Maximum Output Bus Width	36	36	36	36	36
<b>Audio Formats</b>					
S/PDIF Output Ports	1	1	1	1	1
I <sup>2</sup> S Output	2 channel	2 channel	8 channel	2 channel	8 channel
DSD Output	2 channel	NA	6 channel	NA	8 channel
High Bit Rate Audio Support Compressed DTS-HD and Dolby True-HD	No	No	Yes	No	Yes
Maximum Audio Sample Rate (Fs)	192 kHz				
<b>Video Processing</b>					
Color Space Converter	RGB to/from YCbCr	RGB to/from YCbCr xvYCC to RGB	RGB to/from YCbCr	RGB to/from YCbCr xvYCC to RGB	RGB to/from YCbCr xvYCC to RGB
Pixel Clock Divider	÷ 4, ÷ 2				
Digital Video Bus Mapping	Swap Cb, Cr pins				
<b>Other Features</b>					
Local fixed I <sup>2</sup> C Device Address <sup>1</sup>	0x60/0x68 or 0x62/0x6A				
Programmable I <sup>2</sup> C Device Address <sup>1</sup>	NA	0x64, 0xC0, 0xE0	NA	0x64, 0xC0, 0xE0	0x64, 0xC0, 0xE0
Reserved I <sup>2</sup> C Device Address <sup>2</sup>	NA	0x90, 0xD0, 0xE6	NA	0x90, 0xD0, 0xE6	0x90, 0xD0, 0xE6
3D Support	No	Yes	No	Yes	Yes
CEC	No	Yes	No	Yes	Yes
EDID	No	NVRAM	No	NVRAM	NVRAM
HDCP Repeater Support	No	No	Yes	No	Yes
Interlaced Format Detection Pin	Yes	Yes	Yes	Yes	Yes
Package	144-pin TQFP ePad	128-pin TQFP ePad	144-pin TQFP ePad	144-pin TQFP ePad	144-pin TQFP ePad

**Notes:**

1. Refer to the SiI9223A/9233A/9127A HDMI Receivers Programmer Reference for a description of these I<sup>2</sup>C register addresses.
2. These are reserved I<sup>2</sup>C register addresses which are within the I<sup>2</sup>C register address map of the chip. Do not access these registers on the chip, and do not use these addresses for other devices in the system which use the same I<sup>2</sup>C bus.

## 4. Functional Description

The SiI9233A receiver provides a complete solution for receiving HDMI digital audio and video. Specialized audio and video processing is available within the receiver to add HDMI capability to consumer electronics such as DTVs.

Figure 4.1 is a block diagram showing the SiI9233A receiver device incorporated into an AV receiver. Figure 4.2 on the next page shows the functional blocks of the chip. The receiver supports four HDMI input ports. Only one port can be active at any time.

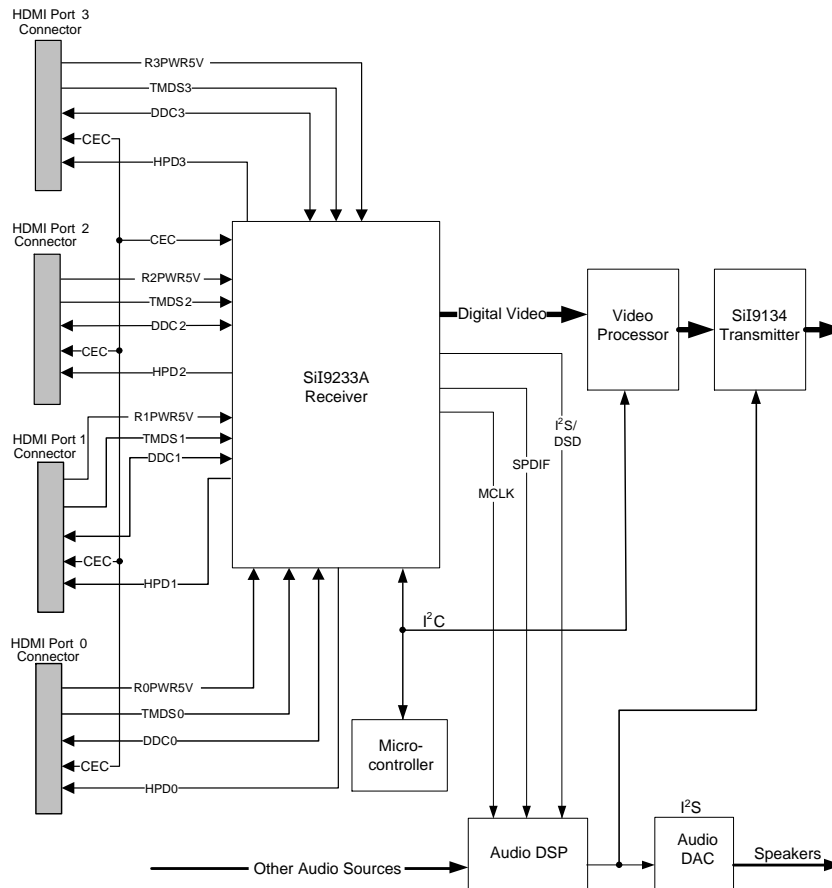


Figure 4.1. A/V Receiver Block Diagram

### 4.1. TMDS Digital Cores

The TMDS Digital core can receive TMDS data at up to 225 MHz. Each core performs 10-to-8-bit TMDS decoding on the video data and 10-to-4 bit TMDS decoding on the audio data received from the three TMDS differential data lines along with a TMDS differential clock. The TMDS core can sense a stopped clock or stopped video and software can put the receiver device into power-down mode.

### 4.2. Active Port Detection and Selection

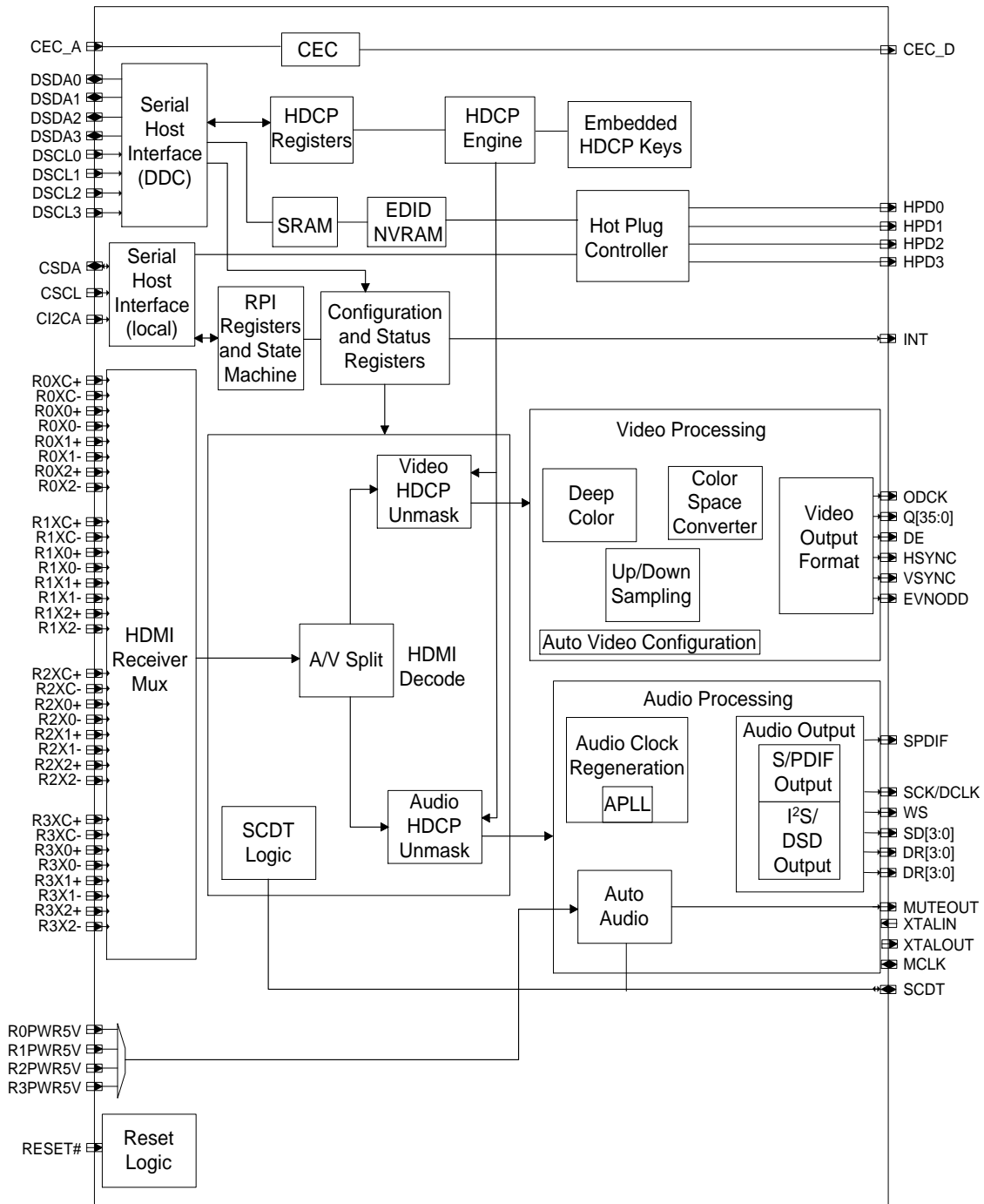
Only one port can be active at a time, under control of the receiver firmware. Active TMDS signaling can arrive at any port, but only one has internal circuitry enabled. The firmware in the display controls these states using register settings.

Other control signals are associated with the TMDS signals on each HDMI port.

The receiver can monitor the +5 V supply from each attached host. The firmware can poll registers to check on which ports are connected. The firmware also controls functional connection to one of the four Extended DDC (E-DDC) buses, enabling one while disabling the others. An attached host determines the active status of an attached HDMI device by



polling the E-DDC bus to the device. See the Programmer Reference (see the [References](#) section on page 72) for a description of port detection and selection. *The Programmer's Reference requires an NDA with Lattice Semiconductor.*



**Figure 4.2. Functional Block Diagram**

### 4.3. HDCP Decryption Engine/XOR Mask

The HDCP decryption engine contains all the necessary logic to decrypt the incoming audio and video data. The decryption process is entirely controlled by the host side microcontroller/microprocessor through a set sequence of register reads and writes through the DDC channel. Pre-programmed HDCP keys and a Key Selection Vector (KSV) stored in the on-chip non-volatile memory are used in the decryption process. A resulting calculated value is applied to an XOR mask during each clock cycle to decrypt the audio/video data.

The SiI9233A receiver also contains all the necessary logic to support full HDCP repeaters. The KSV values of up to 16 downstream devices (up to 16 total) are written to the receiver through the local I<sup>2</sup>C bus (CSDA/CSCL). As defined in the HDCP specification, Vi' is calculated and made available to the host on the DDC bus (DSDA/DSCL).

### 4.4. HDCP Embedded Keys

The receiver comes pre-programmed with a set of production HDCP keys stored on-chip in non-volatile memory. System manufacturers do not need to purchase key sets from the Digital-Content LLC. All purchasing, programming, and security for the HDCP keys is handled by Lattice Semiconductor. The pre-programmed HDCP keys provide the highest level of security, as keys cannot be read out of the device after they are programmed. Before receiving samples of the SiI9233A receiver, customers must sign the HDCP license agreement (available from Digital Content Protection, LLC) or a special NDA with Lattice Semiconductor.

### 4.5. Data Input and Conversion

#### 4.5.1. Mode Control Logic

The mode control logic determines if the decrypted data is video, audio, or auxiliary information and directs it to the appropriate logic block.

#### 4.5.2. Video Data Conversion and Video Output

The SiI9233A receiver can output video in many different formats (see examples in [Table 4.1](#)) and can process the video data before it is sent, as shown in [Figure 4.3](#) on page 13. It is possible to bypass each of the processing blocks by setting the appropriate register bits.

**Table 4.1. Digital Video Output Formats**

Color Space	Video Format	Bus Width	HSYNC/VSYNC	Output Clock (MHz)								Notes
				480i/576i <sup>2-3</sup>	480p	XGA	720p	1080i	SXGA	1080p	UXGA	
RGB	4:4:4	36	Separate	27	27	65	74.25	74.25	108	148.5	162	—
		30	Separate	27	27	65	74.25	74.25	108	148.5	162	—
		24	Separate	27	27	65	74.25	74.25	108	148.5	162	—
		12/15/18	Separate	27	27	65	74.25	74.25	—	—	—	4
YCbCr	4:4:4	36	Separate	27	27	65	74.25	74.25	108	148.5	162	—
		30	Separate	27	27	65	74.25	74.25	108	148.5	162	—
		24	Separate	27	27	65	74.25	74.25	108	148.5	162	—
		12/15/18	Separate	27	27	65	74.25	74.25	—	—	—	4
	4:2:2	16/20/24	Separate	27	27	—	74.25	74.25	—	148.5	162	—
		16/20/24	Embedded	27	27	—	74.25	74.25	—	148.5	162	1
		8/10/12	Separate	27	54	—	148.5	148.5	—	—	—	—
		8/10/12	Embedded	27	54	—	148.5	148.5	—	—	—	1

**Notes:**

1. Embedded syncs use SAV/EAV coding.
2. 480i and 576i modes can output a 13.25 MHz clock using the internal clock divider.
3. Output clock frequency depends on programming of internal registers. Differential TMDS clock is always 25 MHz or faster.
4. Output clock supports 12/15/18-bit mode by using both edges.

#### 4.5.2.1. Color Range Scaling

The color range depends on the video format, according to the CEA-861D specification. In some applications the 8-bit input range uses the entire span of 0x00 (0) to 0xFF (255) values. In other applications the range is scaled narrower. The receiver cannot detect the incoming video data range and there is no required range specification in the HDMI AVI packet. The device chooses scaling depending on the detected video format. 10 and 12-bit color range scaling are both handled the same way. Refer to the Programmer Reference for more details.

When the receiver outputs embedded syncs (SAV/EAV codes), it also limits the YCbCr data output values to 1 to 254.

#### 4.5.2.2. Up Sample / Down Sample

Additional logic can convert from 4:2:2 to 4:4:4 (8/10/12-bit) or from 4:4:4 (8/10/12-bit) to 4:2:2 YCbCr format. All processing is done with 14 bits of accuracy for true 12-bit data.

### 4.5.3. Deep Color Support

The SiI9233A device supports color depth modes greater than 24 bits, known as Deep Color modes, introduced in the HDMI v1.3 Specification. The Deep Color modes employ a new pixel packing scheme to enable the extra bits of higher color depth data to be carried over the existing TMDS data encoding scheme. Currently, three Deep Color modes are defined: 30-bit, 36-bit and 48-bit. The SiI9233A receiver supports two of these three Deep Color modes: 30 and 36-bit modes. In addition, each Deep Color mode is supported to 1080p HD format.

For Deep Color modes, the TMDS clock is run faster than the pixel clock in order to create extra bandwidth for the additional bits of the higher color depth data. The increase in the TMDS clock is by the ratio of the pixel size to 24 bits, as follows:

30-bit mode: TMDS clock = 1.25x pixel clock (5:4)

36-bit mode: TMDS clock = 1.5x pixel clock (3:2)

Because the receiver supports 36-bit mode at 1080p, the highest TMDS clock rate it supports is 225 MHz. When in Deep Color mode, the transmitter periodically sends a General Control Packet with the current color depth and pixel packing phase information to the receiver. The receiver captures the color depth information in a register, which the firmware can then use to set the appropriate clock divider to recover the pixel clock and data.

#### 4.5.4. xvYCC Support

The SiI9233A receiver adds support for the extended gamut xvYCC color space; this extended format has roughly 1.8 times more colors than the RGB color space. The use of the xvYCC color space is made possible because of the availability of LED and laser-based light sources for the next generation displays. This format also makes use of the full range of values (1 to 254) in an 8-bit space instead of 16 to 235 in the RGB format. The use of xvYCC along with Deep Color helps in reducing color banding and allows the display of a larger range of colors than is currently possible.

##### 4.5.4.1. Color Space Conversion

Color space converter (CSC) blocks are provided to convert RGB data to Standard-Definition (ITU.601) or High-Definition (ITU.709) YCbCr formats, and vice-versa. To support the latest extended-gamut xvYCC displays, the SiI9233 device implements color space converter blocks to convert RGB data to extended-gamut Standard-Definition (ITU.601) or High-Definition (ITU.709) xvYCC formats, and vice-versa.

**RGB to YCbCr** The RGB→YCbCr color space converter (CSC) can convert from video data RGB to standard definition (ITU.601) or to high definition (ITU.709) YCbCr formats. The HDMI AVI packet defines the color space of the incoming video.

**YCbCr to RGB** The YCbCr→RGB color space converter is available to interface to MPEG decoders with RGB-only inputs. The CSC can convert from YCbCr in standard-definition (ITU.601) or high-definition (ITU.709) to RGB.

## 4.6. 3D Video Formats

The SiI9233A receiver has support for the 3D video modes described in the HDMI 1.4 Specification. All modes support RGB 4:4:4, YCbCr 4:4:4, and YCbCr 4:2:2 color formats and 8-, 10-, and 12-bit data width per color component. Table 4.2 shows only the maximum possible resolution with a given frame rate; for example, Side-by-Side (Half) mode is defined for 1080p60, which implies that 720p60 and 480p60 are also supported. Furthermore, a frame rate of 24 Hz also means that a frame rate of 23.98 Hz is supported and a frame rate of 60 Hz also means a frame rate of 59.94 Hz is supported. The input pixel clock changes accordingly.

When using Side-by-Side formats the use of 4:2:2 to 4:4:4 up-sampling and 4:4:4 to 4:2:2 down-sampling should not be enabled as it may result in visible artifacts.

Video processing should be bypassed in the case of L + depth format.

**Table 4.2. Supported 3D Video Formats**

3D Format	Extended Definition	Resolution	Frame Rate (Hz)	Input Pixel Clock (MHz)
Frame Packing	—	1080p	24	148.5
	interlaced	720p	50 / 60	
		1080i	50 / 60	
L + depth	—	1080p	24	
		720p	50 / 60	
Side-by-Side	full	1080p	24	
		720p	50 / 60	
	half	1080p	50 / 60	
		1080i	50 / 60	74.25

### 4.6.1. Default Video Configuration

After hardware RESET, the SiI9233A chip is configured in its default mode. This mode is summarized in Table 4.3. For more details and for a complete register listing, refer to the Programmer Reference. *The Programmer's Reference requires an NDA with Lattice Semiconductor.*

**Table 4.3. Default Video Processing**

Video Control	Default after Hardware Reset
HDCP Decryption	HDCP decryption is OFF
Color Space Conversion	No color space conversion
Color Space Selection	BT.601 selected
Color Range Scaling	No range scaling
Upsampling/Downsampling	No upsampling or downsampling
HSYNC & VSYNC Timing	No inversions of HSYNC or VSYNC
Data Bit Width	Uses 8-bit data
Pixel Clock Replication	No pixel clock replication
Power Down	Everything is powered down

**Note:** The receiver device assumes DVI mode after reset, which is RGB 24-bit 4:4:4 video with 0–255 range.

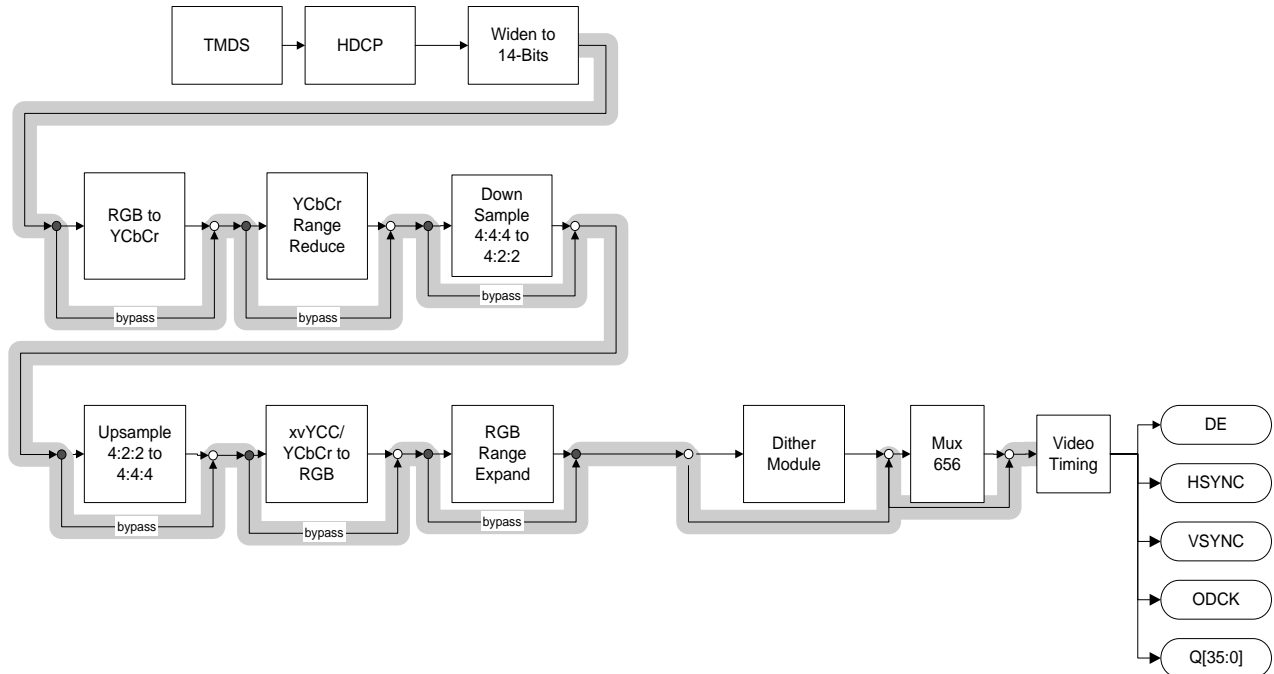


Figure 4.3. Default Video Processing Path

#### 4.6.2. Automatic Video Configuration

The SiI9233A receiver adds automatic video configuration to simplify the firmware’s task of updating the video path whenever the incoming video changes format. Bits in the HDMI Auxiliary Video Information (AVI) InfoFrame are used to reprogram the registers in the video path.

Table 4.4. AVI InfoFrame Video Path Details

AVI Byte 1 Bits [6:5]		AVI Byte 2 Bits [7:6]		AVI Byte 5 Bits [3:0]	
Y[1:0]	Color Space	C[1:0]	Colorimetric	PR[3:0]	Pixel Repetition
00	RGB 4:4:4	00	No Data	0000	No repetition
01	YCbCr 4:2:2	01	ITU 601	0001	Pixel sent 2 times
10	YCbCr 4:4:4	10	ITU 709	0010	Pixel sent 3 times
11	Future	11	Extended Colorimetry Information Valid	0011	Pixel sent 4 times
				0100	Pixel sent 5 times
				0101	Pixel sent 6 times
				0110	Pixel sent 7 times
				0111	Pixel sent 8 times
				1000	Pixel sent 9 times
				1001	Pixel sent 10 times

**Notes on Table 4.4:**

1. The Auto Video Configuration assumes that the AVI information is accurate. If information is not available, then the receiver must choose the video path based on measurement of the incoming resolution.
2. Refer to EIA/CEA-861D Specification for details.
3. The SiI9233A device can support only pixel replication modes 0b0000, 0b0001, and 0b0011. Other modes are unsupported and can result in unpredictable behavior.

The format of the digital video output bus can be automatically configured to many different formats by programming the Auto Output Format Register. The available formats are listed in the table below. For detailed definitions of how to set this register, refer to the Programmer Reference.

**Table 4.5. Digital Output Formats Configurable through Auto Output Format Register**

Digital Output Formats			
Color	Width	MUX	Sync
RGB	4:4:4	N	Separate
YCbCr	4:4:4	N	Separate
YCbCr	4:2:2	N	Separate
YCbCr	4:2:2	Y	Separate
YCbCr	4:2:2	Y	Embedded

## 4.7. Audio Data Output Logic

The SiI9233A receiver can send digital audio over S/PDIF, four I<sup>2</sup>S outputs, or eight one-bit audio outputs.

### 4.7.1. S/PDIF

The S/PDIF stream can carry 2-channel uncompressed PCM data (IEC 60958) or a compressed bit stream for multi-channel (IEC 61937) formats. The audio data output logic forms the audio data output stream from the HDMI audio packets. The S/PDIF output supports audio sampling rates from 32 to 192 kHz. A separate master clock output (MCLK), coherent with the S/PDIF output, is provided for time-stamping purposes. *Coherent* means that the MCLK and S/PDIF are created from the same clock source.

### 4.7.2. I<sup>2</sup>S

The I<sup>2</sup>S bus format is programmable through registers, to allow interfacing with I<sup>2</sup>S audio DACs or audio DSPs with I<sup>2</sup>S inputs. Refer to the Programmer Reference for the different options on the I<sup>2</sup>S bus. Additionally, the MCLK (audio master clock) frequency is selectable to be an integer multiple of the audio sample rate  $F_s$ .

MCLK frequencies support various audio sample rates as shown in [Table 4.6](#).

**Table 4.6. Supported MCLK Frequencies**

Multiple of $F_s$	Audio Sample Rate, $F_s$ : I <sup>2</sup> S and S/PDIF Supported Rates						
	32 kHz	44.1 kHz	48 kHz	88.2 kHz	96 kHz	176.4 kHz	192 kHz
128	4.096 MHz	5.645 MHz	6.144 MHz	11.290 MHz	12.288 MHz	22.579 MHz	24.576 MHz
192	6.144 MHz	8.467 MHz	9.216 MHz	16.934 MHz	18.432 MHz	33.868 MHz	36.864 MHz
256	8.192 MHz	11.290 MHz	12.288 MHz	22.579 MHz	24.576 MHz	45.158 MHz	49.152 MHz
384	12.288 MHz	16.934 MHz	18.432 MHz	33.864 MHz	36.864 MHz		
512	16.384 MHz	22.579 MHz	24.576 MHz	45.158 MHz	49.152 MHz		

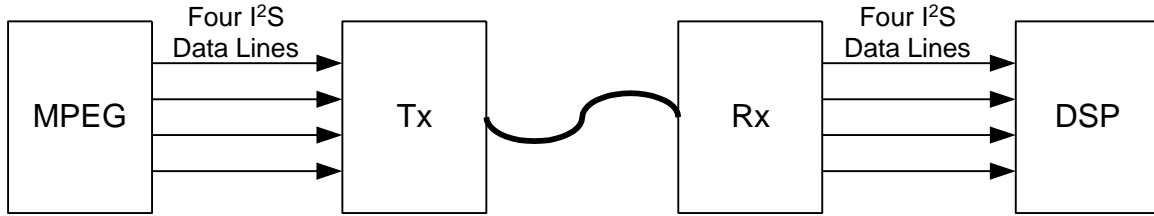
### 4.7.3. One-Bit Audio Input (DSD/SACD)

DSD (direct stream digital) is an audio data format defined for SACD (Super Audio CD) applications. It consists of four data outputs for the left channel, four data outputs for the right channel, and a clock for up to 8-channel support. One-bit Audio supports  $64 \cdot F_s$ , with  $F_s$  being either 44.1 kHz or 88.2 kHz.

The one bit audio outputs are synchronous to the positive edge of the DSD Clock. For one bit audio, the sampling information is carried in the Audio InfoFrame, instead of the Channel Status bits.

### 4.7.4. High-Bitrate Audio on HDMI

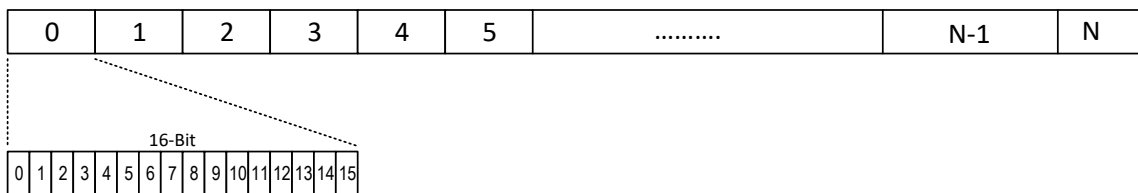
The new high-bitrate compressed standards such as DTS-HD and Dolby TrueHD transmit data at bitrates as high as 18 to 24 Mbps. Because these bitrates are so high, DVD decoders and HDMI transmitters (as source devices), and DSP and HDMI receivers (as sink devices) must carry the data using four I<sup>2</sup>S lines rather than using a single very-high-speed S/PDIF or I<sup>2</sup>S bus (see [Figure 4.4](#) on the next page).



**Figure 4.4. High Speed Data Transmission**

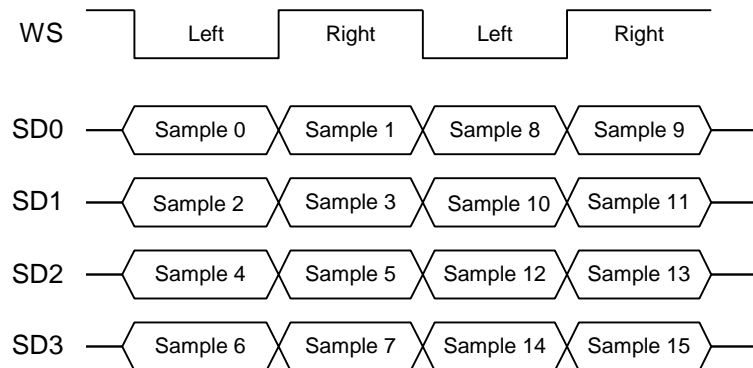
The high-bitrate audio stream is originally encoded as a single stream. To send it over four I<sup>2</sup>S lines, the DVD decoder needs to split this single stream into four streams. Because the single stream of data is being sent over four lines, the programmable ACR (Audio Clock Regeneration) rate is now four times the sample rate of 96 kHz (384 kHz), or 192 kHz (768 kHz).

Figure 4.5 shows the high-bitrate stream before it has been split into four I<sup>2</sup>S lines, and after it has been reassembled.



**Figure 4.5. High-Bitrate Stream Before and After Reassembly and Splitting**

Figure 4.6 shows the same high-bitrate audio stream after being split into four I<sup>2</sup>S lines:



**Figure 4.6. High-Bitrate Stream After Splitting**

**Table 4.7. Maximum Audio Sampling Frequency for All Video Format Timings**

Description	Format Timing	Pixel Repetition	Vertical Freq. (Hz)	Max fs 8 ch (kHz)			Max fs 2 ch (kHz)
				4:2:2 and 4:4:4 24-bit	4:4:4 Deep Color (depth in bits)		
60 Hz Formats				Standard	10	12	
VGA	640x480p	none	59.94/60	48	48	48	192
480i	1440x480i	2	59.94/60	48	48	48	192
480i	2880x480i	4	59.94/60	192	192	192	192
240p	1440x240p	2	59.94/60	48	48	48	192
240p	2880x240p	4	59.94/60	192	192	192	192
480p	720x480p	none	59.94/60	48	48	48	192
480p	1440x480p	2	59.94/60	96	96	96	192
480p	2880x480p	4	59.94/60	192	192	192	192
720p	1280x720p	none	59.94/60	192	192	192	192
1080i	1920x1080i	none	59.94/60	192	192	192	192
1080p	1920x1080p	none	59.94/60	192	192	192	192
50 Hz Formats				Standard	10	12	
576i	1440x576i	2	50	48	48	48	192
576i	2880x576i	4	50	192	192	192	192
288p	1440x288p	2	50	48	48	48	192
288p	2880x288p	4	50	192	192	192	192
576p	720x576p	none	50	48	48	48	192
576p	1440x576p	2	50	96	96	96	192
576p	2880x576p	4	50	192	192	192	192
720p/50	1280x720p	none	50	192	192	192	192
1080i/50	1920x1080i	none	50	192	192	192	192
1080p/50	1920x1080p	none	50	192	192	192	192
1080p @ 24 Hz – 30 Hz				Standard	10	12	
1080p	1920x1080p	none	24	192	192	192	192
1080p	1920x1080p	none	25	192	192	192	192
1080p	1920x1080p	none	29.97/30	192	192	192	192

#### 4.7.5. Auto Audio Configuration

The SiI9233A receiver can control the audio output based on the current states of CablePlug, FIFO, Video, ECC, ACR, PLL, InfoFrame, and HDMI. Audio output is enabled only when all necessary conditions are met. If any critical condition is missing, then the audio output is disabled automatically.

#### 4.7.6. Soft Mute

On command from a register bit or when automatically triggered with Automatic Audio Control (AAC), the receiver progressively reduces the audio data amplitude to mute the sound in a controlled manner. This feature is useful when there is an interruption to the HDMI audio stream (or an error) to prevent any audio pop from being sent to the I<sup>2</sup>S or S/PDIF outputs.



## 4.8. Control and Configuration

### 4.8.1. Register/Configuration Logic

The register/configuration logic block incorporates all the registers required for configuring and managing the features of the SiI9233A receiver. These registers are used to perform HDCP authentication, audio/video/auxiliary format processing, CEA-861B InfoFrame Packet format, and power-down control.

The registers are accessible from one of two serial ports. The first port is the DDC port, which is connected through the HDMI cable to the HDMI host. It is used to control the SiI9233A receiver from the host system for HDCP operation. The second port is the local I<sup>2</sup>C port, which is used to control the SiI9233A device from the display system. This is shown in Figure 4.7. The Local Bus accesses the General Registers and the Common Registers. The DDC Bus accesses the HDCP Operation registers and the Common Registers.

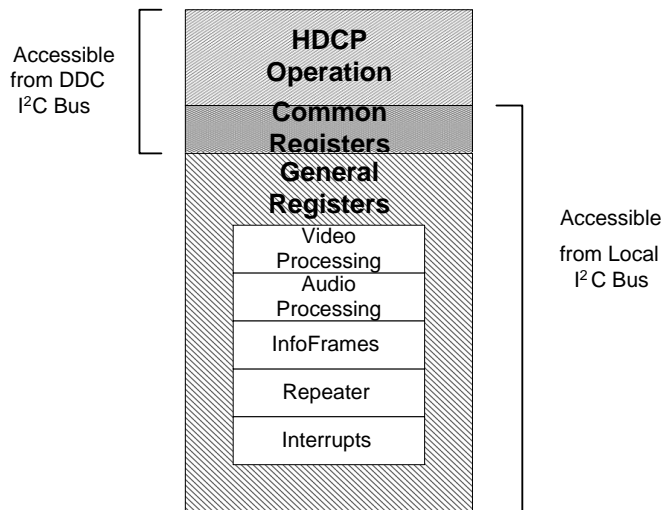


Figure 4.7. I<sup>2</sup>C Register Domains

### 4.8.2. I<sup>2</sup>C Serial Ports

The SiI9233A receiver provides 5 I<sup>2</sup>C serial interfaces: 4 DDC ports to communicate back to the HDMI or DVI hosts; one I<sup>2</sup>C port for initialization and control by a local microcontroller in the display. Each interface is 5 V tolerant.

#### 4.8.2.1. E-DDC Bus Interface to HDMI Host

The four DDC interfaces (DSDA0-3 and DSCL0-3) on the receiver are slave interfaces that can run up to 100 kHz. Each interface is connected to one E-DDC bus and is used for reading the integrated EDID in addition to HDCP authentication.

The SiI9233A receiver is accessible on the E-DDC bus at device addresses 0xA0 for the EDID, and 0x74 for HDCP control. This feature is compliant with the HDCP 1.3 Specification.

### 4.8.3. EDID FLASH and RAM Block

The EDID block consists of 1024 bytes of RAM. Each port has a block of 256 bytes of RAM for EDID data. This feature allows simultaneous reads of all ports from four different source devices that are connected to the SiI9233A device. In addition to the RAM, the EDID block contains 256 bytes of FLASH that is shared by all ports. As a result, the timing information must be identical among all the ports if the internal EDID is used. An additional area of FLASH contains unique CEC physical address and checksum values for each of the four ports. This feature allows simultaneous reads of all ports from four different source devices if they are connected and attempt an EDID read at the same time. If independent EDIDs are required on any of the ports, a CPU can externally load the 256 bytes of RAM for that port, by using the local I<sup>2</sup>C bus.

The internal EDID can be selected on a per-port basis using registers on the local I<sup>2</sup>C bus. For example, Port 0 and Port 1 can use the internal EDID, and Port 2 and Port 3 can use a discrete EEPROM for the EDID.

#### 4.8.4. CEC Interface

The Consumer Electronics Control (CEC) Interface block provides CEC electrically compliant signals between CEC devices and a CEC master. It allows products to meet the electrical specifications of CEC signaling by translating the LVTTTL signals of an external microcontroller (CEC host-side or transmit-side) to CEC signaling levels for CEC devices at the receive-side, and vice versa.

Additionally, a CEC controller compatible with the Lattice Semiconductor CEC Programming Interface (CPI) is included on-chip. This CEC controller has a high-level register interface accessible through the I<sup>2</sup>C interface which can be used to send and receive CEC commands. This controller makes CEC control very easy and straightforward, and removes the burden of having a host CPU perform these low-level transactions on the CEC bus.

##### 4.8.4.1. I<sup>2</sup>C Interface to Display Controller

The Controller I<sup>2</sup>C interface (CSDA, CSCL) on the SiI9233A receiver is a slave interface capable of running up to 400 kHz. This bus is used to configure the chip by reading/writing to the appropriate registers. It is accessible on the local I<sup>2</sup>C bus at two device addresses. Refer to the Programmer Reference for more information. *The Programmer's Reference requires an NDA with Lattice Semiconductor.*

#### 4.8.5. Standby and HDMI Port Power Supplies

The receiver device incorporates a power island that continues to supply power to the EDID memory, the DDC ports, and the CEC bus when power is removed from the VCC pins, as long as power continues to be provided through at least one connected HDMI cable or by system standby power. Refer to Figure 4.8. The internal power multiplexer selects power from either SBVCC5 (if it is available) or from one of the R<sub>n</sub>PWR5V pins.

The power island results in an extremely low power standby mode, but allows the EDID to be readable and the CEC controller to be functional. No damage will occur to the device when in this mode.

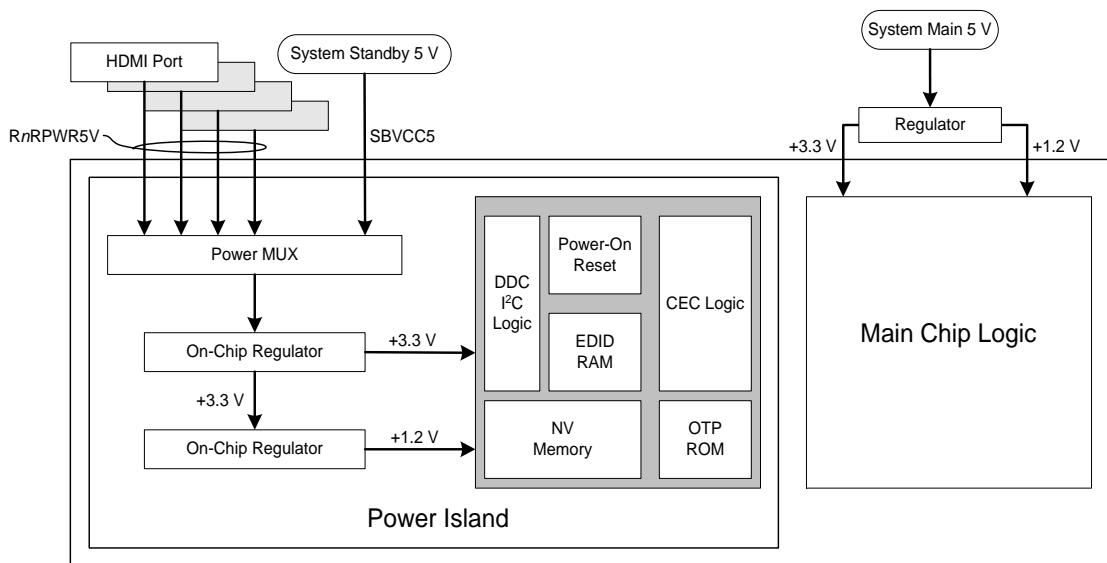


Figure 4.8. Power Island

## 5. Electrical Specifications

### 5.1. Absolute Maximum Conditions

**Table 5.1. Absolute Maximum Conditions**

Symbol	Parameter	Min	Typ	Max	Units	Note
IOVCC33	I/O Pin Supply Voltage	-0.3	—	4.0	V	1, 2, 3
AVCC12	TMD5 Analog Supply Voltage	-0.3	—	1.9	V	1, 2
AVCC33	TMD5 Analog Supply Voltage	-0.3	—	4.0	V	1, 2
APVCC12	Audio PLL Supply Voltage	-0.3	—	1.9	V	1, 2
CVCC12	Digital Core Supply Voltage	-0.3	—	1.9	V	1, 2
XTALVCC33	ACR PLL Crystal Oscillator Supply Voltage	-0.3	—	4.0	V	1, 2
SBVCC5	Standby Supply Voltage	-0.3	—	5.7	V	1, 2
V <sub>I</sub>	Input Voltage	-0.3	—	IOVCC33 + 0.3	V	1, 2
V <sub>5V-Tolerant</sub>	Input Voltage on 5 V tolerant Pins	-0.3	—	5.5	V	5
T <sub>J</sub>	Junction Temperature	—	—	125	°C	—
T <sub>STG</sub>	Storage Temperature	-65	—	150	°C	—

**Notes:**

1. Permanent device damage can occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described under [Normal Operating Conditions](#) on the next page.
3. Voltage undershoot or overshoot cannot exceed absolute maximum conditions.
4. Refer to the SiI9233A Qualification Report for information on ESD performance.
5. All VCCs must be powered to the device. If the device is unpowered and 5 V is applied to these inputs, damage can occur.

## 5.2. Normal Operating Conditions

Table 5.2. Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Note
IOVCC33	I/O Pin Supply Voltage	3.13	3.3	3.47	V	1, 4
AVCC12	TMDS Analog Supply Voltage	1.14	1.2	1.26	V	1, 6
AVCC33	TMDS Analog Supply Voltage	3.13	3.3	3.47	V	3
APVCC12	Audio PLL Supply Voltage	1.14	1.2	1.26	V	—
CVCC12	Digital Core Supply Voltage	1.14	1.2	1.26	V	2
XTALVCC33	ACR PLL Crystal Oscillator Supply Voltage	3.13	3.3	3.47	V	4
SBVCC5	Standby Supply Voltage	4.75	5.0	5.25	V	10
RnPWR5V	DDC I <sup>2</sup> C I/O Reference Voltage	4.7	5.0	5.3	V	11
DIFF33	Difference between two 3.3 V Power Pins	—	—	1.0	V	4
DIFF12	Difference between two 1.2 V Power Pins	—	—	1.0	V	4
DIFF3312	Difference between any 3.3 V and 1.2 V Pin	-1.0	—	2.6	V	4, 5
V <sub>CCN</sub>	Supply Voltage Noise	—	—	100	mV <sub>P-P</sub>	7
T <sub>A</sub>	Ambient Temperature (with power applied)	0	25	70	°C	—
Θ <sub>ja</sub>	Ambient Thermal Resistance (Theta JA)	—	—	27	°C/W	—

**Notes:**

- IOVCC33 and AVCC33 pins should be controlled from one power source.
- CVCC12 should be controlled from one power source.
- AVCC12 pin should be regulated.
- Power supply sequencing must guarantee that power pins stay within these limits of each other; see Figure 6.2 on page 28.
- No 1.2 V pin can be more than DIFF3312[*min*] higher than any 3.3 V pin. No 3.3 V pin can be more than DIFF3312[*max*] higher than any 1.2 V pin.
- The HDMI Specification requires termination voltage (AVCC33) to be controlled to 3.3 V ±5%. The SiI9233A receiver tolerates a wider range of ±300 mV.
- The supply voltage noise is measured at test point VCCTP in Figure 5.1. The ferrite bead provides filtering of power supply noise. The figure is representative and applies to other VCC pins as well.
- Airflow at 0 m/s.
- Figure 9.4 on page 64 and Figure 9.5 on page 65 show decoupling and power supply regulation.
- SBVCC5V should provide a stable 5 V before any other VCC is applied to the device; see the Power-on Sequencing section on page 60.
- Maximum current draw from this source is 50 mA. There is no power-on sequence requirement for this source.

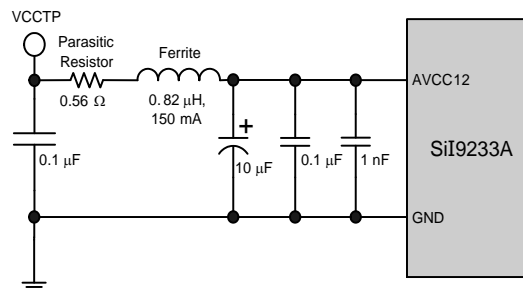


Figure 5.1. Test Point VCCTP for VCC Noise Tolerance Spec

**Notes:**

- The Ferrite (0.82 μH, 150 mA) attenuates the PLL power supply noise at 10 kHz and above.
- The optional parasitic resistor minimizes the peaking. The typical value used here is 0.56 Ω. 1 Ω is the maximum.

### 5.3. DC Specifications

**Table 5.3. Digital I/O Specifications**

Symbol	Parameter	Pin Type <sup>3</sup>	Conditions <sup>2</sup>	Min	Typ	Max	Units	Note
V <sub>IH</sub>	HIGH-level Input Voltage	LVTTTL	—	2.0	—	—	V	—
V <sub>IL</sub>	LOW-level Input Voltage	LVTTTL	—	—	—	0.8	V	—
V <sub>TH+</sub>	LOW to HIGH Threshold RESET # Pin	Schmitt	—	1.46	—	—	V	5
V <sub>TH-</sub>	HIGH to LOW Threshold RESET# Pin	Schmitt	—	—	—	0.96	V	5
DDC V <sub>TH+</sub>	LOW to HIGH Threshold DSDA0, DSDA1, DSCL0 and DSCL1 pins.	Schmitt	—	3.0	—	—	V	—
DDC V <sub>TH-</sub>	HIGH to LOW Threshold DSDA0, DSDA1, DSCL0 and DSCL1 pins.	Schmitt	—	—	—	1.5	V	—
Local I <sup>2</sup> C V <sub>TH+</sub>	LOW to HIGH Threshold CSCL and CSDA pins	Schmitt	—	2.1	—	—	V	11, 13
Local I <sup>2</sup> C V <sub>TH-</sub>	HIGH to LOW Threshold CSCL and CSDA pins	Schmitt	—	—	—	0.86	V	11, 13
V <sub>OH</sub>	HIGH-level Output Voltage	LVTTTL	—	2.4	—	—	V	10
V <sub>OL</sub>	LOW-level Output Voltage	LVTTTL	—	—	—	0.4	V	10
I <sub>OL</sub>	Output Leakage Current	—	High Impedance	-10	—	10	μA	—
V <sub>ID</sub>	Differential Input Voltage	—	—	75	250	780	mV	4
I <sub>OD4</sub>	4 mA Digital Output Drive	Output	V <sub>OUT</sub> = 2.4 V	4	—	—	mA	1, 6, 7
			V <sub>OUT</sub> = 0.4 V	4	—	—	mA	1, 6, 7
I <sub>OD8</sub>	8 mA Digital Output Drive	Output	V <sub>OUT</sub> = 2.4 V	8	—	—	mA	1, 6, 8
			V <sub>OUT</sub> = 0.4 V	8	—	—	mA	1, 6, 8
I <sub>OD12</sub>	12 mA Digital Output Drive	Output	V <sub>OUT</sub> = 2.4 V	12	—	—	mA	1, 6, 9
			V <sub>OUT</sub> = 0.4 V	12	—	—	mA	1, 6, 9
R <sub>PD</sub>	Internal Pull Down Resistor	Outputs	IOVCC33 = 3.3 V	25	50	110	kΩ	1, 12
I <sub>OPD</sub>	Output Pull Down Current	Outputs	IOVCC33 = 3.6 V	—	60	90	μA	1, 12
I <sub>IPD</sub>	Input Pull Down Current	Input	IOVCC33 = 3.6 V	—	60	90	μA	1

**Notes:**

- These limits are guaranteed by design.
- Under normal operating conditions unless otherwise specified, including output pin loading C<sub>L</sub> = 10 pF.
- Refer to the [Pin Diagram and Descriptions](#) section beginning on page 34 for pin type designations for all package pins.
- Differential input voltage is a single-ended measurement, according to DVI Specification.
- Schmitt trigger input pin thresholds V<sub>TH+</sub> and V<sub>TH-</sub> correspond to V<sub>IH</sub> and V<sub>IL</sub>, respectively.
- Minimum output drive specified at ambient = 70 °C and IOVCC33 = 3.0 V. Typical output drive specified at ambient = 25 °C and IOVCC33 = 3.3 V. Maximum output drive specified at ambient = 0 °C and IOVCC33 = 3.6 V.
- I<sub>OD4</sub> Output applies to pins SPDIF, SCK, WS, SD[3:0], DCLK, INT, and CSDA.
- I<sub>OD8</sub> Output applies to pins DE, HSYNC, VSYNC, Q[35:0].and MCLK.
- I<sub>OD12</sub> Output applies to pin ODCK.
- Note that the SPDIF output drives LVTTTL levels, not the low-swing levels defined by IEC958.
- The SCL and SDA pins are not true open-drain buffers. When no VCC is applied to the chip, these pins can continue to draw a small current, and prevent the master IC from communicating with other devices on the I<sup>2</sup>C bus. Therefore, do not power-down the receiver (remove VCC) unless the attached I<sup>2</sup>C bus is completely idle.
- The chip includes an internal pull-down resistor on many of the output pins. When in the high-impedance state, these pins draw a pull down current according to this specification when the signal is driven HIGH by another source device.
- With -10% IOVCC33 supply, the HIGH-to-LOW threshold on DDC and I<sup>2</sup>C bus is marginal. A -5% tolerance on the IOVCC33 power supply is recommended.

### 5.3.1. DC Power Supply Pin Specifications

**Table 5.4. Total Power versus Power-Down Modes**

Symbol	Parameter	Mode	Frequency	Typ <sup>3</sup>			Max <sup>4</sup>			Units	Notes
				3.3 V	1.2 V	SBVCC5	3.3 V	1.2 V	SBVCC5		
I <sub>PDQ3</sub>	Complete Power-Down Current	A	—				63	3	8	mA	1, 6
I <sub>PDS</sub>	Sleep Power-down Current	B	27 MHz				67	21	8	mA	2, 7
			74.25 MHz				90	25	8	mA	
			150 MHz				74	25	8	mA	
			225 MHz				74	25	8	mA	
I <sub>STBY</sub>	Standby Current	C	27 MHz				0	0	8	mA	2, 8
			74.25 MHz				0	0	8	mA	
			150 MHz				0	0	8	mA	
			225 MHz				0	0	8	mA	
I <sub>UNS</sub>	Unselected Current	D	27 MHz	67	112	8	68	147	8	mA	2, 8
			74.25 MHz	70	172	8	72	193	8	mA	
			150 MHz	75	289	8	78	302	8	mA	
			225 MHz	77	310	8	78	322	8	mA	
I <sub>CCD</sub>	Full Power Digital Out Current	E	27 MHz	98	112	8	115	148	8	mA	2, 10
			74.25 MHz	167	175	8	179	185	8	mA	
			150 MHz	266	289	8	289	296	8	mA	
			225 MHz	345	313	8	377	319	8	mA	

**Notes:**

1. Power is not related to input TMDS clock (RxC) frequency because the selected TMDS port is powered down.
2. Power is related to input TMDS clock (RxC) frequency at the selected TMDS port. Only one port can be selected.
3. Typical power specifications measured with supplies at typical normal operating conditions; and a video pattern that combines gray scale, checkerboard and text.
4. Maximum power limits measured with supplies at maximum normal operating conditions, minimum normal operating ambient temperature, and a video pattern with single-pixel vertical lines.
5. Registers are always accessible on local I2C (CSDA/CSCL) without active link clock.
6. Power Down Mode A: Minimum power. Everything is powered off. Host sees no termination of TMDS signals on any of the four TMDS ports. I2C access is still available.
7. Power Down Mode B: Powers down TMDS core. CKDT remains enabled and state can be polled in register. Host device can sense TMDS termination.
8. Power Down Mode C: Power off to 3.3 V and 1.2 V supplies. Power on to SBVCC5 standby supply.
9. Power Down Mode D: Monitor SCDT on selected TMDS port with outputs in the high-impedance state. HDCP continues in the selected port, but the output of the receiver can be connected to a shared bus.
10. Digital Functional Mode E: Full Operation on one port with digital outputs

**Table 5.5. Power-down Mode Definitions**

Mode		3.3 V Supply	1.2 V Supply	SBVCC5	Register Bit States				Description
					PDTOT#	PD_TMDS#	PD_AO#	PD_VO#	
A	Power Down	ON	ON	ON	0	1	1	1	Minimum power. Everything is powered off. Host sees no termination of TMDS signals on any of the four TMDS ports. I <sup>2</sup> C access is still available.
B	Sleep Mode Power	ON	ON	ON	1	0	1	1	Powers down TMDS core. CKDT remains enabled and state can be polled in register. Host device can sense TMDS termination.
C	Standby Power	OFF	OFF	ON	1	1	1	1	Power off to 3.3 V and 1.2 V supplies. Power on to SBVCC5 standby supply.
D	Unselected Power	ON	ON	ON	1	1	0	0	Monitor SCDT on selected TMDS port with outputs in the high-impedance state. HDCP continues in the selected port, but the output of the receiver can be connected to a shared bus.
E	Digital	ON	ON	ON	1	1	1	1	Full operation on one port with digital outputs.

**Notes:**

1. PD Clks include PD\_MCLK#, PD\_XTAL#, PD\_APLL#, and PD\_PCLK# all set to zero.
2. PD Outs include PD\_AO#, and PD\_VO# all set to zero.
3. Refer to the Programmer Reference for register bit descriptions.

## 5.4. AC Specifications

**Table 5.6. TMD5 Input Timings**

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T <sub>DPS</sub>	Intra-Pair Differential Input Skew	—	—	—	T <sub>BIT</sub>	ps	—	2, 4
T <sub>CCS</sub>	Channel to Channel Differential Input Skew	—	—	—	T <sub>CIP</sub>	ns	Figure 6.1	2, 3
F <sub>RXC</sub>	Differential Input Clock Frequency	—	25	—	225	MHz	—	—
T <sub>RXC</sub>	Differential Input Clock Period	—	4.44	—	40	ns	—	—
T <sub>JIT</sub>	Differential Input Clock Jitter tolerance (0.3Tbit)	74.25 MHz	—	—	400	ps	—	2, 5, 6

**Notes:**

- Under normal operating conditions unless otherwise specified, including output pin loading of C<sub>L</sub> = 10 pF.
- Guaranteed by design.
- IDCK Period (refer to the applicable Lattice Semiconductor HDMI Transmitter Data Sheet).
- 1/10 of IDCK Period (refer to the applicable Lattice Semiconductor HDMI Transmitter Data Sheet).
- Jitter defined per HDMI Specification.
- Jitter measured with Clock Recovery Unit per HDMI Specification. Actual jitter tolerance can be higher depending on the frequency of the jitter.

Refer to the Programmer Reference (see the [References](#) section on page 72) for more details on controlling timing modes.

### 5.4.1. Video Output Timings

**Table 5.7. 12/15/18-Bit Data Output Timings**

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
D <sub>LHT</sub>	LOW-to-HIGH Rise Time Transition	C <sub>L</sub> = 10 pF	—	—	1.5	ns	Figure 6.4	2
D <sub>HLT</sub>	HIGH-to-LOW Fall Time Transition	C <sub>L</sub> = 10 pF	—	—	1.5	ns	Figure 6.4	2
R <sub>CIP</sub>	ODCK Cycle Time	C <sub>L</sub> = 10 pF	12.12	—	40	ns	Figure 6.5	8
F <sub>CIP</sub>	ODCK Frequency	C <sub>L</sub> = 10 pF	25	—	82.5	MHz	—	5
T <sub>DUTY</sub>	ODCK Duty Cycle	C <sub>L</sub> = 10 pF	40%	—	60%	R <sub>CIP</sub>	Figure 6.5	3
T <sub>CK2OUT</sub>	ODCK-to-Output Delay	C <sub>L</sub> = 10 pF	0.4	—	2.5	ns	Figure 6.5	—

**Table 5.8. 16/20/24/30/36-Bit Data Output Timings**

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
D <sub>LHT</sub>	LOW-to-HIGH Rise Time Transition	C <sub>L</sub> = 10 pF	—	—	1.5	ns	Figure 6.4	2
D <sub>HLT</sub>	HIGH-to-LOW Fall Time Transition	C <sub>L</sub> = 10 pF	—	—	1.5	ns	Figure 6.4	2
R <sub>CIP</sub>	ODCK Cycle Time	C <sub>L</sub> = 10 pF	6.06	—	40	ns	Figure 6.5	5, 8
F <sub>CIP</sub>	ODCK Frequency	C <sub>L</sub> = 10 pF	25	—	165	MHz	—	5
T <sub>DUTY</sub>	ODCK Duty Cycle	C <sub>L</sub> = 10 pF	40%	—	60%	R <sub>CIP</sub>	Figure 6.5	3
T <sub>CK2OUT</sub>	ODCK-to-Output Delay	C <sub>L</sub> = 10 pF	0.4	—	2.5	ns	Figure 6.5	—

**Notes:**

- Under normal operating conditions unless otherwise specified, including output pin loading of C<sub>L</sub>=10 pF.
- Rise time and fall time specifications apply to HSYNC, VSYNC, DE, ODCK, EVNODD and Q[35:0].
- Output clock duty cycle is independent of the differential input clock duty cycle. Duty cycle is a component of output setup and hold times.
- See [Table 6.2](#) on page 32 for calculation of worst case output setup and hold times.
- All output timings are defined at the maximum operating ODCK frequency, F<sub>CIP</sub>, unless otherwise specified.
- F<sub>CIP</sub> can be the same as F<sub>RXC</sub> or one-half of F<sub>RXC</sub>, depending on OCLKDIV setting. F<sub>CIP</sub> can also be F<sub>RXC</sub> /1.25 or F<sub>RXC</sub> /1.5 if Deep Color mode is being transmitted.
- R<sub>CIP</sub> is the inverse of F<sub>CIP</sub> and is not a controlling specification.
- Output skew specified when ODCK is programmed to divide-by-two mode.



## 5.4.2. Audio Output Timings

**Table 5.9. I<sup>2</sup>S Output Port Timings**

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T <sub>tr</sub>	SCK Clock Period (TX)	C <sub>L</sub> = 10 pF	1.00	—	—	T <sub>tr</sub>	Figure 6.6	1
T <sub>HC</sub>	SCK Clock HIGH Time	C <sub>L</sub> = 10 pF	0.35	—	—	T <sub>tr</sub>		1
T <sub>LC</sub>	SCK Clock LOW Time	C <sub>L</sub> = 10 pF	0.35	—	—	T <sub>tr</sub>		1
T <sub>SU</sub>	Setup Time, SCK to SD/WS	C <sub>L</sub> = 10 pF	0.4T <sub>TR</sub> - 5	—	—	ns		1
T <sub>HD</sub>	Hold Time, SCK to SD/WS	C <sub>L</sub> = 10 pF	0.4T <sub>TR</sub> - 5	—	—	ns		1
T <sub>SCKDUTY</sub>	SCK Duty Cycle	C <sub>L</sub> = 10 pF	40%	—	60%	T <sub>tr</sub>		1
T <sub>SCK2SD</sub>	SCK to SD or WS Delay	C <sub>L</sub> = 10 pF	-5	—	+5	ns		2
T <sub>AUDDL</sub>	Audio Pipeline Delay	—	—	40	80	μs	—	—

**Notes:**

1. Refer to Figure 6.6 on page 30. Meets timings in Philips I<sup>2</sup>S Specification.
2. Applies also to SDC-to-WS delay.

**Table 5.10. S/PDIF Output Port Timings**

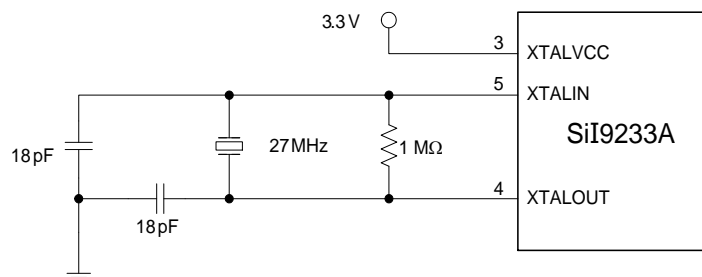
Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T <sub>SPCYC</sub>	SPDIF Cycle Time	C <sub>L</sub> = 10 pF	—	1.0	—	UI	Figure 6.7	1, 2
F <sub>SPDIF</sub>	SPDIF Frequency	—	4	—	24	MHz		3
T <sub>SPDUTY</sub>	SPDIF Duty Cycle	C <sub>L</sub> = 10 pF	90%	—	110%	UI		2, 5
T <sub>MCLKCYC</sub>	MCLK Cycle Time	C <sub>L</sub> = 10 pF	20	—	250	ns	Figure 6.8	1, 2, 4
F <sub>MCLK</sub>	MCLK Frequency	C <sub>L</sub> = 10 pF	4	—	50	MHz		1, 2, 4
T <sub>MCLKDUTY</sub>	MCLK Duty Cycle	C <sub>L</sub> = 10 pF	40%	—	60%	T <sub>MCLKCYC</sub>		2, 4
T <sub>AUDDL</sub>	Audio Pipeline Delay	—	—	40	80	μs	—	—

**Notes:**

1. Guaranteed by design.
2. Proportional to unit time (UI), according to sample rate.
3. SPDIF is not a true clock, but is generated from the internal 128Fs clock, for Fs from 128 to 512 kHz.
4. MCLK refers to MCLKOUT.
5. Intrinsic jitter on S/PDIF output can limit its use as an S/PDIF transmitter. The S/PDIF intrinsic jitter is approximately 0.1 UI.

**Table 5.11. Audio Crystal Timings**

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
F <sub>X TAL</sub>	External Crystal Freq.	—	26	27	28.5	MHz	Figure 5.2	1, 2


**Figure 5.2. Audio Crystal Schematic**

### 5.4.3. Miscellaneous Timings

**Table 5.12. Miscellaneous Timings**

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T <sub>I2CDVD</sub>	SDA Data Valid delay from SCL falling edge	C <sub>L</sub> = 400 pF	—	—	700	ns	—	—
F <sub>DDC</sub>	Speed on TMDS DDC Ports	C <sub>L</sub> = 400 pF	—	—	100	kHz	—	2
F <sub>I<sup>2</sup>C</sub>	Speed on Local I <sup>2</sup> C Port	C <sub>L</sub> = 400 pF	—	—	400	kHz	—	3
T <sub>RESET</sub>	RESET# Signal LOW Time for valid reset	—	50	—	—	μs	Figure 6.3	—
T <sub>STARTUP</sub>	Startup time from power supplies valid	—	—	—	100	ms	—	5
T <sub>BKSVINIT</sub>	HDCP BKS <sub>V</sub> Load Time	—	—	—	2.2	ms	—	4

**Notes:**

- Under normal operating conditions unless otherwise specified, including output pin loading of C<sub>L</sub> = 10 pF.
- DDC ports are limited to 100 kHz by the HDMI Specification, and meet I<sup>2</sup>C standard mode timings.
- Local I<sup>2</sup>C port (CSCL/CSDA) meets standard mode I<sup>2</sup>C timing requirements to 400 kHz.
- The time required to load the KSV values internal to the receiver after a RESET# and the start of an active TMDS clock. An attached HDCP host device should not attempt to read the receiver BKS<sub>V</sub> values until after this time. The T<sub>BKSVINIT</sub> Min and Max values are based on the maximum and minimum allowable XCLK frequencies. The loading of the BKS<sub>V</sub> values requires a valid XCLK and TMDS clock.
- T<sub>STARTUP</sub> is the startup time required for the device to be operational once power is stable. This startup time is due to the on board voltage regulator for the EDID and CEC and a power on reset circuit.

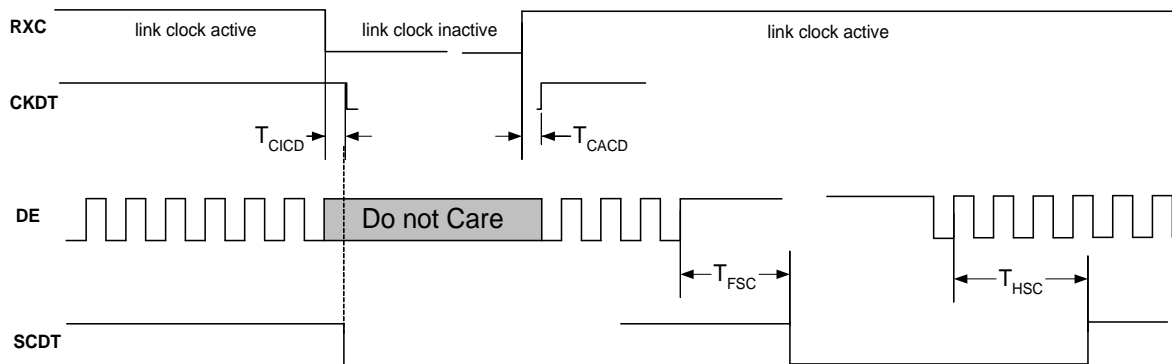
### 5.4.4. Interrupt Timings

**Table 5.13. Interrupt Output Pin Timings**

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
$T_{FSC}$	Link disabled (DE inactive) to SCDT LOW	—	—	0.15	40	ms	Figure 5.3	1, 2, 3, 8
$T_{HSC}$	Link enabled (DE active) to SCDT HIGH	—	—	—	4	DE	Figure 5.3	1, 2, 4, 8
$T_{CICD}$	RXC inactive to CKDT LOW	—	—	—	100	$\mu$ s	Figure 5.3	1, 2, 8
$T_{CACD}$	RXC active to CKDT HIGH	—	—	—	10	$\mu$ s	Figure 5.3	1, 2, 8
$T_{INT}$	Response Time for INT from Input Change	—	—	—	100	$\mu$ s	—	1, 5, 8
$T_{CIOD}$	RXC inactive to ODCK inactive	—	—	—	100	ns	—	1, 8
$T_{CAOD}$	RXC active to ODCK active and stable	—	—	—	10	ms	—	1, 6, 8
$T_{SRRF}$	Delay from SCDT rising edge to Software Reset falling edge	—	—	—	100	ms	Figure 6.3	7

**Notes:**

- Guaranteed by design.
- SCDT and CKDT are register bits in this device.
- SCDT changes to LOW after DE is HIGH for approximately 4096 pixel clock cycles, or after DE is LOW for approximately 1,000,000 clock cycles. At 27 MHz pixel clock, this delay for DE HIGH is approximately 150  $\mu$ s, and the delay for DE LOW is approximately 40 ms.
- SCDT changes to HIGH when clock is active ( $T_{CACD}$ ) and at least 4 DE edges have been recognized. At 720p, the DE period is 22  $\mu$ s, so SCDT responds approximately 50  $\mu$ s after  $T_{CACD}$ .
- The INT pin changes state after a change in input condition when the corresponding interrupt is enabled.
- Output clock (ODCK) becomes active before it becomes stable. Use the SCDT signal as the indicator of stable video output timings, as this depends on decoding of DE signals with active RXC (see  $T_{FSC}$ ).
- Software Reset must be asserted and then de-asserted within the specified maximum time after rising edge of Sync Detect (SCDT). Access to both SWRST and SCDT can be limited by the speed of the I2C connection.
- SCDT is HIGH only when CKDT is also HIGH. When the receiver is in a powered-down mode, the INT output pin indicates the current state of SCDT. Thus, a power-down receiver signals a microcontroller connected to the INT pin whenever SCDT changes from LOW to HIGH or HIGH to LOW.


**Figure 5.3. SCDT and CKDT Timing from DE or RXC Inactive/Active**
**Notes:**

- The SCDT shown in Figure 5.3 is a register bit. SCDT remains HIGH if DE is stuck in LOW while RXC remains active, but SCDT changes to LOW if DE is stuck HIGH while RXC remains active.
- The CKDT shown in Figure 5.3 is a register bit. CKDT changes to LOW whenever RXC stops, and changes to HIGH when RXC starts. SCDT changes to LOW when CKDT changes to LOW.
- SCDT changes to LOW when CKDT changes to LOW. SCDT changes to HIGH at  $T_{HSC}$  after CKDT changes to HIGH.
- The INT output pin changes state after the SCDT or CKDT register bit is set or cleared if those interrupts are enabled.

Refer to the Programmer Reference for more details on controlling timing modes.

## 6. Timing Diagrams

### 6.1. TMDS Input Timing Diagrams

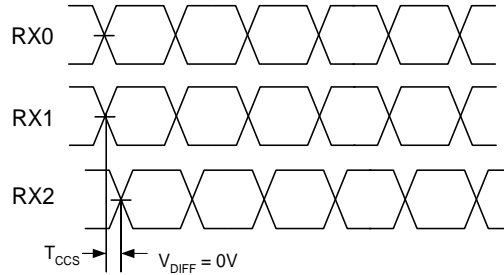


Figure 6.1. TMDS Channel-to-Channel Skew Timing

### 6.2. Power Supply Control Timings

Figure 6.2 illustrates the power supply sequencing.

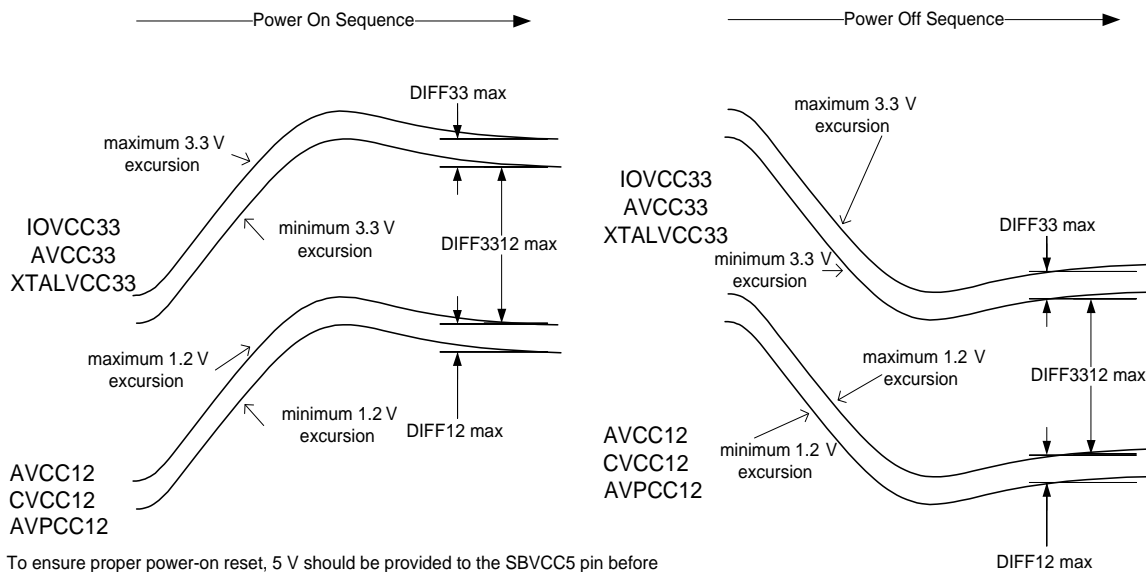
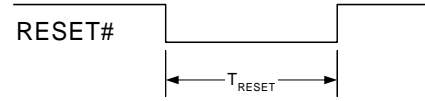
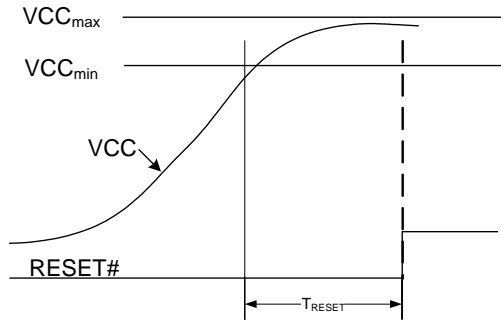


Figure 6.2. Power Supply Sequencing

### 6.3. Reset Timings



RESET# must be pulled LOW for  $T_{RESET}$  before accessing registers. This can be done by holding RESET# LOW until  $T_{RESET}$  after stable power (at left); OR by pulling RESET# LOW from a HIGH state (at right) for at least  $T_{RESET}$ .

Note that VCC must be stable between its limits for Normal Operating Conditions for  $T_{RESET}$  before RESET# is HIGH.

Figure 6.3. RESET# Minimum Timings

### 6.4. Digital Video Output Timing Diagrams

#### 6.4.1. Output Transition Times

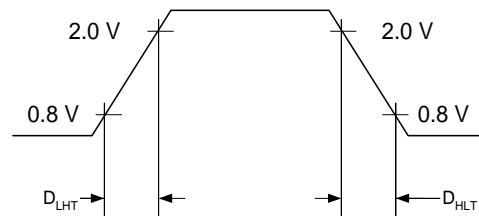


Figure 6.4. Video Digital Output Transition Times

### 6.4.2. Output Clock to Output Data Delay

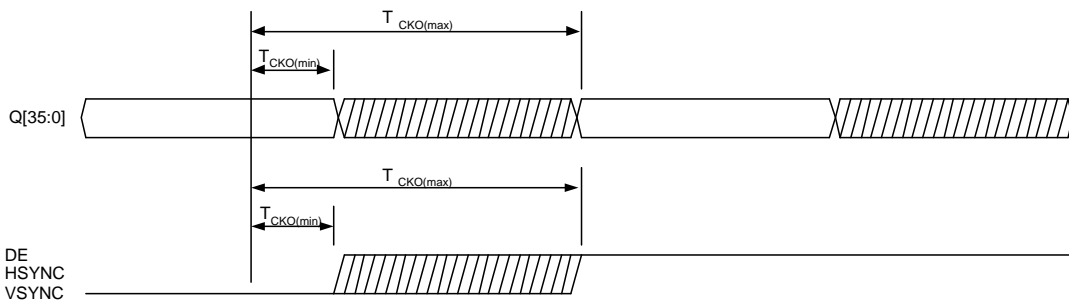
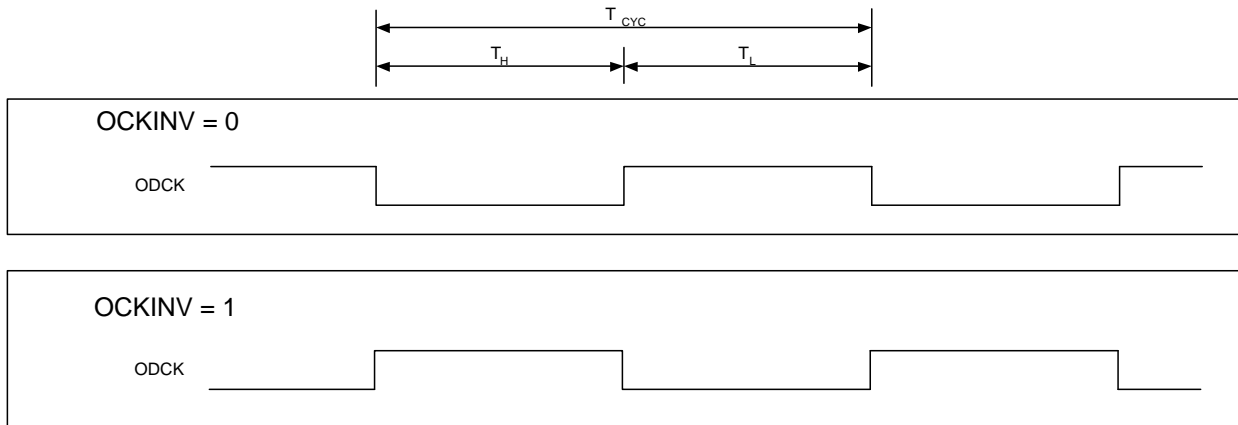


Figure 6.5. Receiver Clock-to-Output Delay and Duty Cycle Limits

### 6.5. Digital Audio Output Timings

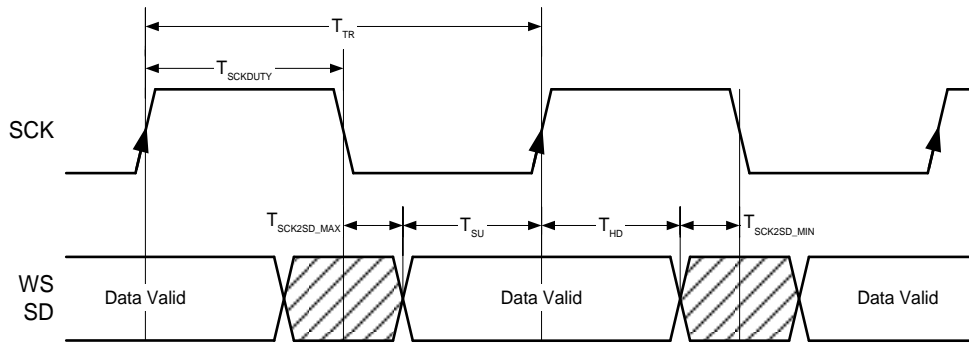


Figure 6.6. I<sup>2</sup>S Output Timings

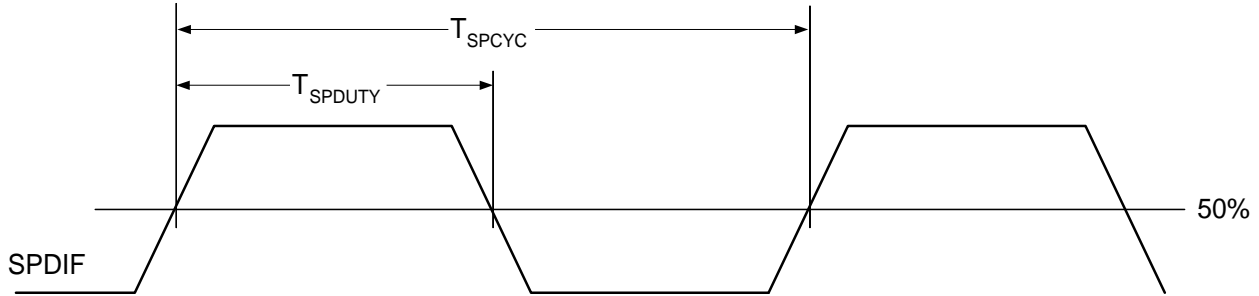


Figure 6.7. S/PDIF Output Timings

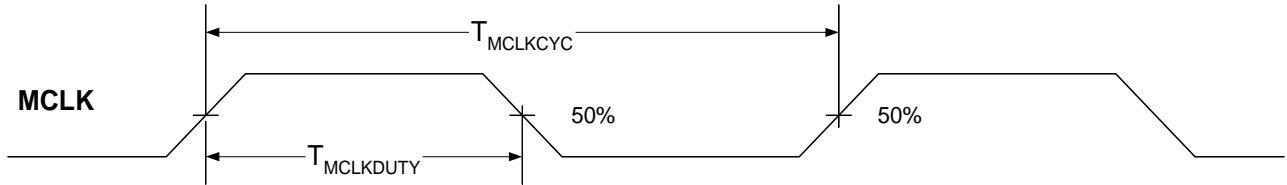


Figure 6.8. MCLK Timings

## 6.6. Calculating Setup and Hold Times for Video Bus

### 6.6.1. 24/30/36-Bit Mode

Output data is clocked out on one rising (or falling) edge of ODCK, and is then captured downstream using the same polarity ODCK edge one clock period later. The setup time of data to ODCK and hold time of ODCK to data are therefore a function of the worst case ODCK to output delay, as shown in Figure 6.9. The active rising ODCK edge is shown with an arrowhead. For OCKINV=1, reverse the logic.

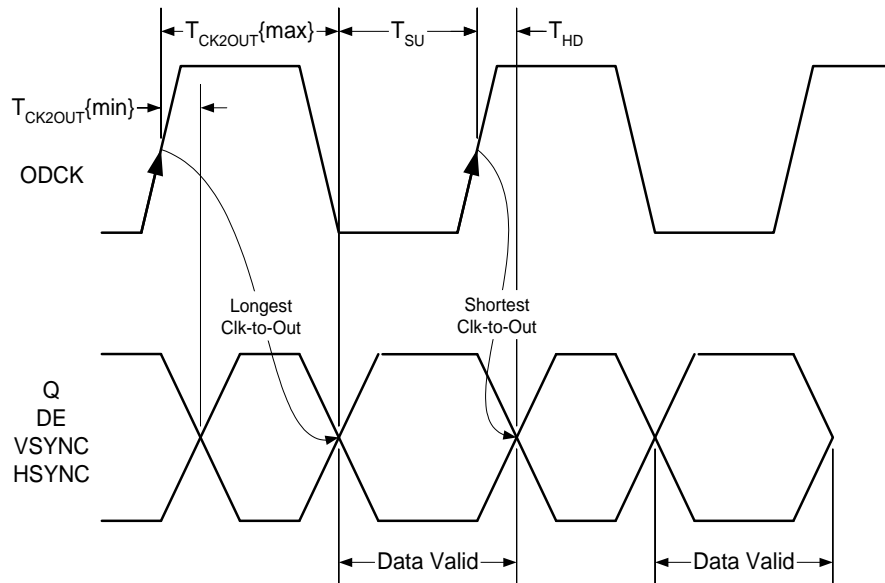


Figure 6.9. 24/30/36-Bit Mode Receiver Output Setup and Hold Times

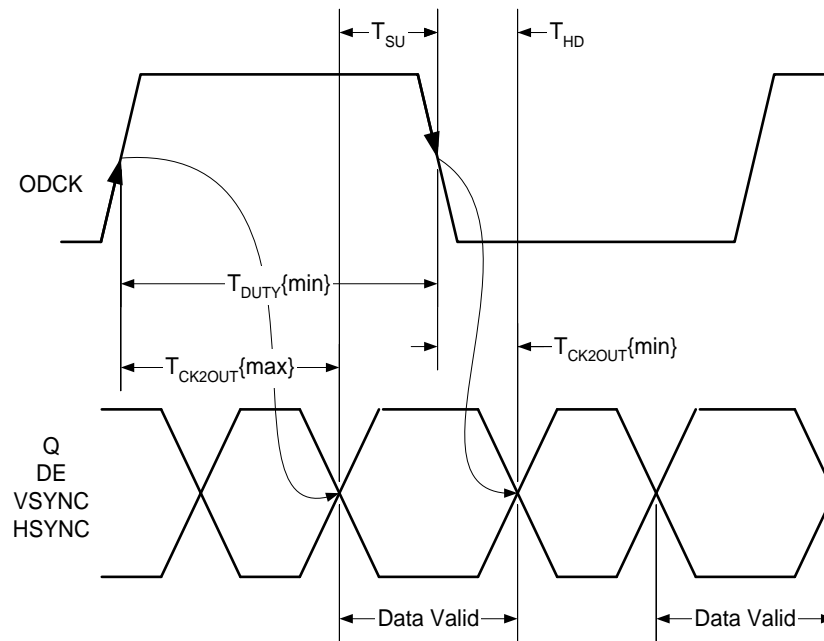
Table 6.1 on the next page shows minimum calculated setup and hold times for commonly used ODCK frequencies. The setup and hold times apply to DE, VSYNC, HSYNC and Data output pins, with output load of 10pF. These are approximations. Hold time is not related to ODCK frequency.

**Table 6.1. Calculation of 24/30/36-Bit Output Setup and Hold Times**

	Symbol	Parameter	T <sub>ODCK</sub>		Min
			27 MHz	74.25 MHz	
24/30/36-Bit Mode	T <sub>SU</sub>	Setup Time to ODCK = T <sub>ODCK</sub> - T <sub>CK2OUT</sub> {max}	37.0 ns	13.5 ns	34.5 ns
	T <sub>HD</sub>	Hold Time from ODCK = T <sub>CK2OUT</sub> {min}	37.0 ns	37.0 ns	0.4 ns

### 6.6.2. 12/15/18-Bit Dual-Edge Mode

Output data is clocked out on each edge of ODCK (both rising and falling), and is then captured downstream using the opposite ODCK edge. This is shown in Figure 6.10. The setup time of data to ODCK is a function of the shortest duty cycle and the longest ODCK to output delay. The hold time does not depend on duty cycle (since every edge is used), and is a function only of the shortest ODCK to output delay.



**Figure 6.10. 12/15/18-Bit Mode Receiver Output Setup and Hold Times**

Table 6.2 shows minimum calculated setup and hold times for commonly used ODCK frequencies, up to the maximum allowed for 12/15/18-bit mode. The setup and hold times apply to DE, VSYNC, HSYNC and Data output pins, with output load of 10 pF. These are approximations. Hold time is not related to ODCK frequency.

**Table 6.2. Calculation of 12/15/18-Bit Output Setup and Hold Times**

	Symbol	Parameter	T <sub>ODCK</sub>		Min
			27 MHz	74.25 MHz	
12/15/18-Bit Mode	T <sub>SU</sub>	Setup Time to ODCK = T <sub>ODCK</sub> • T <sub>DUTY</sub> {min} - T <sub>CK2OUT</sub> {max}	37.0 ns	13.5 ns	12.3 ns
	T <sub>HD</sub>	Hold Time from ODCK = T <sub>CK2OUT</sub> {min}	37.0 ns	37.0 ns	0.4 ns



## 6.7. Calculating Setup and Hold Times for I<sup>2</sup>S Audio Bus

Valid serial data is available at  $T_{\text{sck2sd}}$  after the falling edge of the first SCK cycle, and then captured downstream using the active rising edge of SCK one clock period later. The setup time of data to SCK ( $T_{\text{SU}}$ ) and hold time of SCK to data ( $T_{\text{HD}}$ ) are therefore a function of the worst case SCK-to-output data delay ( $T_{\text{sck2sd}}$ ). Figure 6.6 on page 30 illustrates this timing relationship. Note that the active SCK edge (rising edge) is shown with an arrowhead. For a falling edge sampling clock, the logic is reversed.

Table 6.3 shows the setup and hold time calculation examples for various audio sample frequencies. The formula used in these examples also applies when calculating the setup and hold times for other audio sampling frequencies.

**Table 6.3. I<sup>2</sup>S Setup and Hold Time Calculations**

Symbol	Parameter	FWS (kHz)	FSCLK (MHz)	Ttr	Min
$T_{\text{SU}}$	Setup Time, SCK to SD/WS $= T_{\text{TR}} - ( T_{\text{SCKDUTY\_WORST}} + T_{\text{SCK2SD\_MAX}} )$ $= T_{\text{TR}} - (0.6T_{\text{TR}} + 5\text{ns})$ $= 0.4T_{\text{TR}} - 5\text{ns}$	32 kHz	2.048	488 ns	190 ns
		44.1 kHz	2.822	354 ns	136 ns
		48 kHz	3.072	326 ns	125 ns
		96 kHz	6.144	163 ns	60 ns
		192 kHz	12.288	81 ns	27 ns
$T_{\text{HD}}$	Hold Time, SCK to SD/WS $= ( T_{\text{SCKDUTY\_WORST}} - T_{\text{SCK2SD\_MIN}} )$ $= 0.4T_{\text{TR}} - 5\text{ns}$	32 kHz	2.048	488 ns	190 ns
		44.1 kHz	2.822	354 ns	136 ns
		48 kHz	3.072	326 ns	125 ns
		96 kHz	6.144	163 ns	60 ns
		192 kHz	12.288	81 ns	27 ns

**Note:** The sample calculations shown are based on WS = 64 SCLK rising edges.

## 7. Pin Diagram and Descriptions

### 7.1. Pin Diagram

Figure 7.1 shows the pin assignments of the SiI9233A receiver device. Individual pin functions are described in the [Pin Descriptions](#) section on the next page. The package is a 20 mm × 20 mm 144-pin TQFP with an ePad, which **must** be connected to ground.

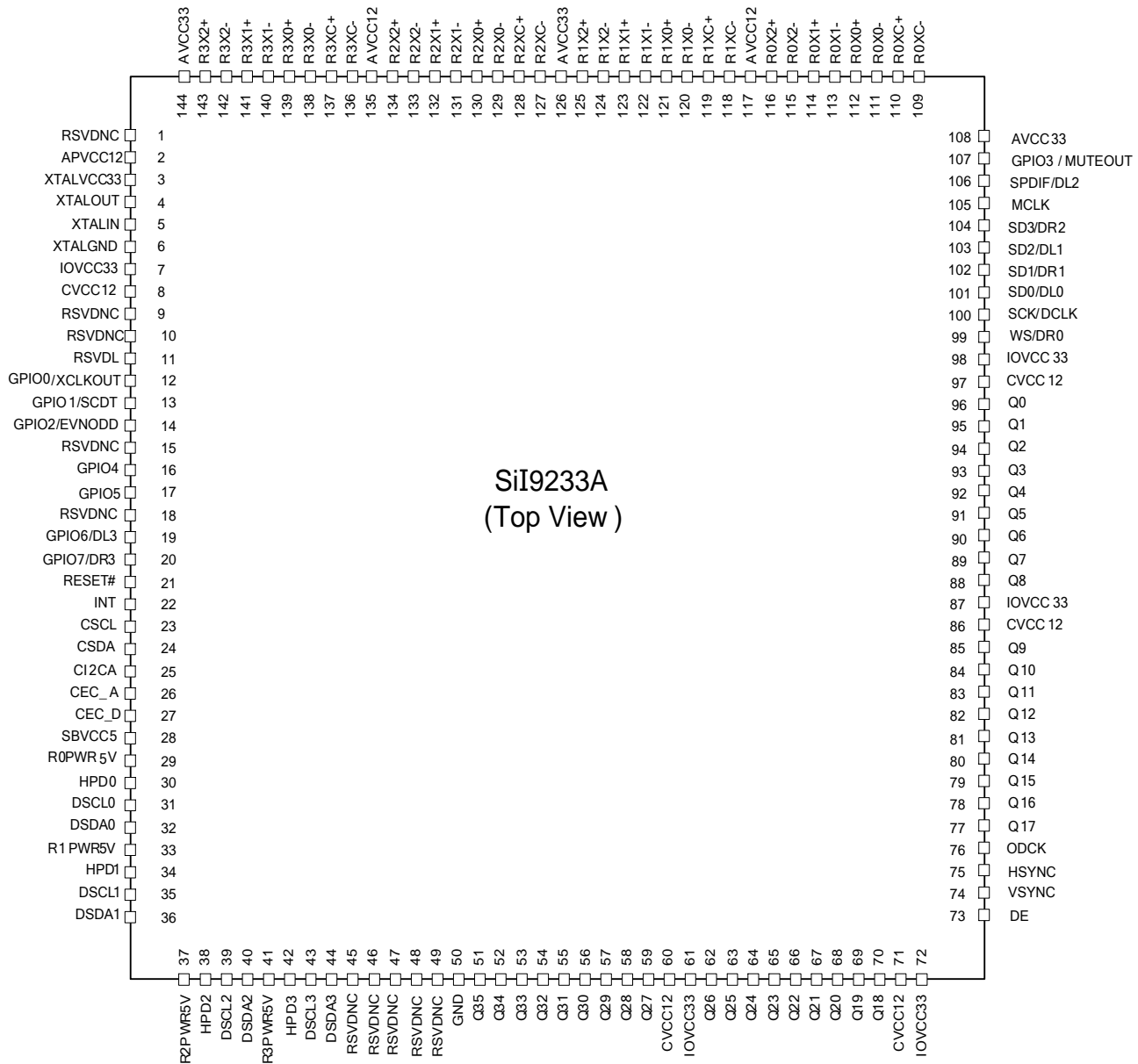


Figure 7.1. Pin Diagram

## 7.2. Pin Descriptions

### 7.2.1. Differential Signal Data Pins

Pin Name	Pin	Type	Dir	Description
R0X0+ R0X0- R0X1+ R0X1- R0X2+ R0X2-	112 111 114 113 116 115	TMDS analog	Input	HDMI Port 0 TMDS input data pairs.
R0XC+ R0XC-	110 109	TMDS analog	Input	HDMI Port 0 TMDS input clock pair.
R1X0+ R1X0- R1X1+ R1X1- R1X2+ R1X2-	121 120 123 122 125 124	TMDS analog	Input	HDMI Port 1 TMDS input data pairs.
R1XC+ R1XC-	119 118	TMDS analog	Input	HDMI Port 1 TMDS input clock pair.
R2X0+ R2X0- R2X1+ R2X1- R2X2+ R2X2-	130 129 132 131 134 133	TMDS analog	Input	HDMI Port 2 TMDS input data pairs.
R2XC+ R2XC-	128 127	TMDS analog	Input	HDMI Port 2 TMDS input clock pair.
R3X0+ R3X0- R3X1+ R3X1- R3X2+ R3X2-	139 138 141 140 143 142	TMDS analog	Input	HDMI Port 3 TMDS input data pairs.
R3XC+ R3XC-	137 136	TMDS analog	Input	HDMI Port 3 TMDS input clock pair.

### 7.2.2. Digital Video Output Data Pins

Pin Name	Pin	Type	Dir	Description
Q0	96	LVTTL 2 mA to 14 mA	Output	36-Bit Output Pixel Data Bus. Q[35:0] is highly configurable using the various video configuration registers. It supports a wide array of output formats, including multiple RGB and YCbCr bus formats. Using the appropriate bits in the PD_SYS2 register, the output drivers can be put into a high impedance state.
Q1	95			
Q2	94			
Q3	93			
Q4	92			
Q5	91			
Q6	90			
Q7	89			
Q8	88			
Q9	85			
Q10	84			
Q11	83			
Q12	82			
Q13	81			
Q14	80			
Q15	79			
Q16	78			
Q17	77			
Q18	70			
Q19	69			
Q20	68			
Q21	67			
Q22	66			
Q23	65			
Q24	64			
Q25	63			
Q26	62			
Q27	59			
Q28	58			
Q29	57			
Q30	56			
Q31	55			
Q32	54			
Q33	53			
Q34	52			
Q35	51			

**Notes:**

1. When transporting video data that uses fewer than 36 bits, the unused bits on the Q[] bus can still carry switching pixel data signals. Unused Q[35:0] bus pins should be unconnected, masked or ignored by downstream devices. For example, carrying YCbCr 4:2:2 data with 16-bit width (see the [YC 4:2:2 Formats with Separate Syncs](#) section on page 47), the bits Q[0] through Q[7] output switching signals.
2. The output data bus, Q[0:35], can be wire-ORed to another device so one device is always in the high-impedance state. However, these pins do not have internal pull-up or pull-down resistors, and so cannot pull the bus HIGH or LOW when all connected devices are in the high impedance state.
3. The drive strength of Q[0:35] can be programmed in 2-mA steps between 2 mA and 14 mA.

### 7.2.3. Digital Video Output Control Pins

Pin Name	Pin	Type	Dir	Description
DE	73	LVTTL 2 mA to 14 mA	Output	Data Enable.
HSYNC	75	LVTTL 2 mA to 14 mA	Output	Horizontal Sync Output.
VSYNC	74	LVTTL 2 mA to 14 mA	Output	Vertical Sync Output.
GPIO2/ EVNODD	14	LVTTL 8 mA	Input	Programmable GPIO2.
GPIO2/ EVNODD			Output	Indicates Even or Odd Field for Interlaced Formats.
ODCK	76	LVTTL 2 mA to 14 mA	Output	Output Data Clock.

#### Notes:

- HSYNC and VSYNC outputs carry sync signals for both embedded and separate sync configurations.
- The drive strength of DE, HSYNC, VSYNC, and ODCK can be programmed in 2-mA steps between 2 mA and 14 mA.

### 7.2.4. HDMI Control Signal Pins

Pin Name	Pin	Type	Dir	Description
DSCL0	31	Schmitt	Input	DDC I <sup>2</sup> C Clock for respective port. HDCP KSV, An, and Ri values are exchanged over an I <sup>2</sup> C port during authentication. True open drain, so does not pull to GND if power is not applied.
DSCL1	35	Open drain		
DSCL2	39	5 V tolerant		
DSCL3	43			
DSDA0	32	Schmitt	Input Output	DDC I <sup>2</sup> C Data for respective port. HDCP KSV, An, and Ri values are exchanged over an I <sup>2</sup> C port during authentication. True open drain, so does not pull to GND if power is not applied.
DSDA1	36	Open drain		
DSDA2	40	5 V tolerant		
DSDA3	44	3 mA		
HPD0	30	LVTTL 4 mA	Input	Hotplug output signal to HDMI connector for respective port
HPD1	34		Output	Indicates EDID is readable..
HPD2	38			
HPD3	42			
R0PWR5V	29	LVTTL 5 V tolerant	Input	5 V power and port detection input for respective port. Used to power internal EDID when device is not powered.
R1PWR5V	33			
R2PWR5V	37			
R3PWR5V	41			
CEC_A	26	CEC compliant 5 V tolerant	Input	HDMI compliant CEC I/O used to interface to CEC devices. This pin connects to the CEC signal of all HDMI connectors in the system. This pin has an internal pull-up resistor.
CEC_D			Output	
CEC_D	27	LVTTL Schmitt	Input Output	CEC interface to local system. True open-drain. An external pull-up is required. This pin typically connects to the local CPU.

### 7.2.5. Digital Audio Output Pins

Pin Name	Pin	Type	Dir	Description
XTALIN	5	5 V tolerant LVTTTL	Input	Crystal Clock Input. Also allows LVTTTL input. Frequency required: 26 MHz – 28.5 MHz.
XTALOUT	4	LVTTTL 4 mA	Output	Crystal Clock Output.
GPIO0/ XCLKOUT	12	LVTTTL 4 mA	Input	Programmable GPIO0.
GPIO0/ XCLKOUT			Output	Additional Clock Output from crystal oscillator circuit.
MCLK	105	LVTTTL 8 mA	Output	Audio Master Clock Output.
SCK/ DCLK	100	LVTTTL 4 mA	Output	I <sup>2</sup> S Serial Clock Output.
SCK/ DCLK				DSD Clock Output.
SD3/DR2 SD2/DL1 SD1/DR1 SD0/DL0	104 103 102 101	LVTTTL 4 mA	Output	I <sup>2</sup> S Serial Data Output.
SD3/DR2 SD2/DL1 SD1/DR1 SD0/DL0	DSD Serial Right Ch2 Data Output. DSD Serial Left Ch1 Data Output. DSD Serial Right Ch1 Data Output. DSD Serial Left Ch0 Data Output.			
WS/ DR0	99	LVTTTL 4 mA	Output	I <sup>2</sup> S Word Select Output.
WS/ DR0				DSD Serial Right Ch0 Data Output.
SPDIF/ DL2	106	LVTTTL 4 mA	Output	S/PDIF Audio Output.
SPDIF/ DL2				DSD Serial Left Channel 2 data output.
GPIO6/ DL3	19	LVTTTL 4 mA	Input/ Output	Programmable GPIO6.
GPIO6/ DL3			Output	DSD Serial Left Channel 3 data output.
GPIO7/ DR3	20	LVTTTL 4 mA	Input/ Output	Programmable GPIO7.
GPIO7/ DR3			Output	DSD Serial Right Channel 3 data output.
GPIO3/ MUTEOUT	107	LVTTTL 4 mA	Input Output	Programmable GPIO3 or Mute Audio Output.
GPIO3/ MUTEOUT			Output	Mute Audio Output. Signal to the external downstream audio device, audio DAC, and so on to mute audio output.

**Note:** The XTALIN pin can either be driven at LVTTTL levels by a clock (leaving XTALOUT unconnected), or connected through a crystal to XTALOUT; see [Figure 9.7](#) on page 67.

### 7.2.6. Configuration/Programming Pins

Pin Name	Pin	Type	Dir	Description
INT	22	LVTTTL 4 mA	Output	Interrupt Output. Configurable polarity and push-pull output. Multiple sources of interrupt can be enabled through the INT_EN register. See note below.
RESET#	21	Schmitt 5 V tolerant	Input	Reset Pin. Active LOW.
C_SCL	23	Schmitt 5 V tolerant	Input	Configuration/Status I <sup>2</sup> C Clock. Chip configuration/status, CEA-861 support and downstream HDCP registers are accessed via this I <sup>2</sup> C port.
C_SDA	24	Schmitt 5 V tolerant 3 mA	Input Output	Configuration/Status I <sup>2</sup> C Data. Chip configuration/status, CEA-861 support and downstream HDCP registers are accessed via this I <sup>2</sup> C port.
CI2CA	25	LVTTTL 5 V tolerant	Input	Local I <sup>2</sup> C Address Select. LOW = Addresses 0x60/0x68 HIGH = Addresses 0x62/0x6A
GPIO1/SCDT	13	LVTTTL 4 mA	Input Output	Programmable GPIO1.
GPIO1/SCDT			Output	Sync Detection Indicator. Indicates Active Video at HDMI Input Port.
GPIO4	16	LVTTTL 4 mA	Input Output	Programmable GPIO4.
GPIO5	17	LVTTTL 4 mA	Input Output	Programmable GPIO5.

**Note:** The INT pin can be programmed to be either a push-pull LVTTTL output or an open-drain output.

### 7.2.7. Power and Ground Pins

Pin Name	Pin	Type	Description	Supply
CVCC12	8, 60, 71, 86, 97	Power	Digital Logic VCC.	1.2 V
IOVCC33	7, 61, 72, 87, 98	Power	Input/Output Pin VCC.	3.3 V
AVCC33	108, 126, 144	Power	TMDS Analog VCC 3.3 V.	3.3 V
AVCC12	117, 135	Power	TMDS Analog VCC 1.2 V.	1.2 V
APVCC12	2	Power	Audio Clock Regeneration PLL Analog VCC. Must be connected to 1.2 V.	1.2 V
XTALVCC33	3	Power	Audio Clock Regeneration PLL crystal oscillator power. Must be connected to 3.3 V.	3.3 V
XTALGND	6	Ground	Audio Clock Regeneration ground.	Ground
SBVCC5	28	Power	Standby power supply. All other supplies can be off with SBVCC5 on.	5 V
GND	50, ePad (bottom of package)	Ground	Ground. The ePad <b>must</b> be soldered to ground.	Ground

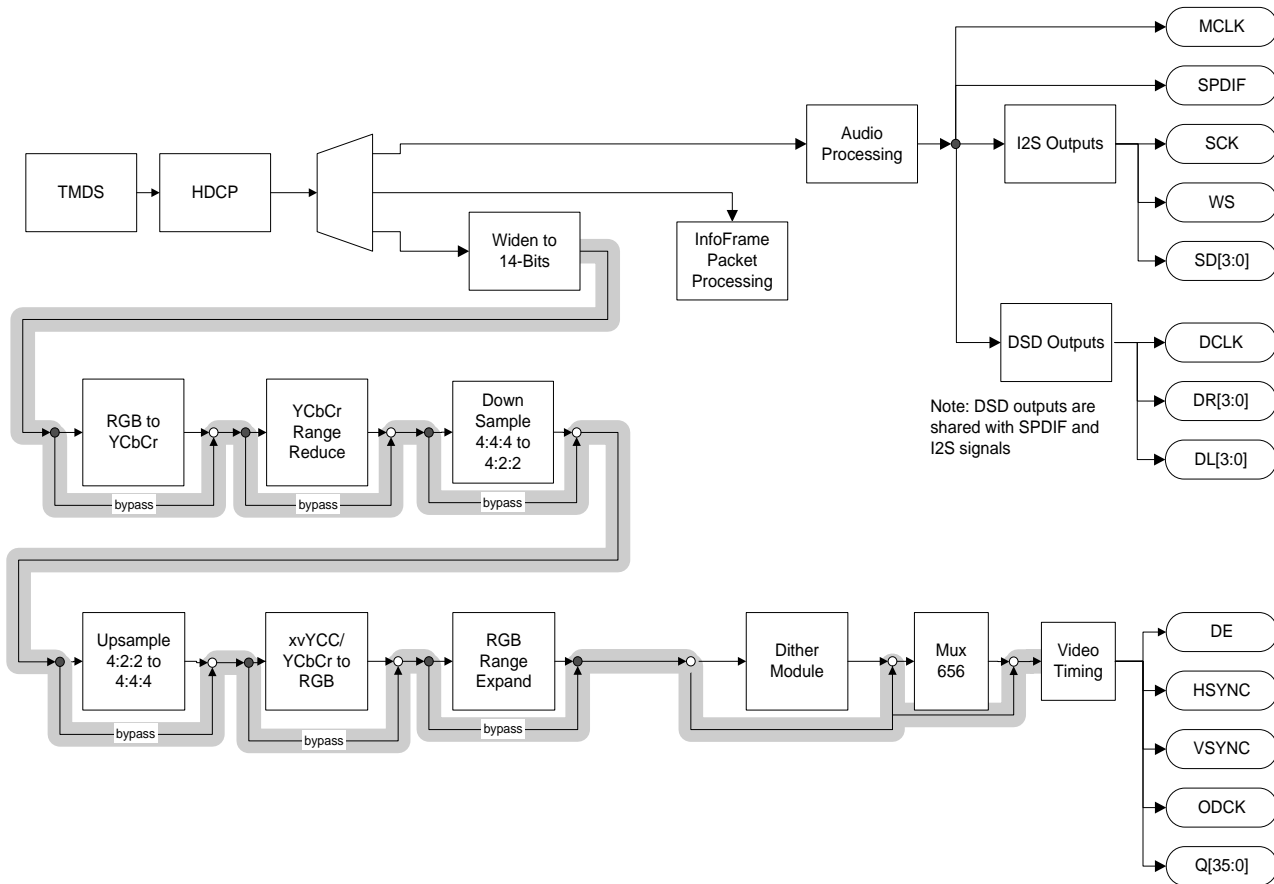
### 7.2.8. Reserved and Not Connected Pins

Pin Name	Pin	Type	Description	Supply
RSVDNC	1, 9, 10, 15, 18, 45–49	Reserved	Reserved, must be left unconnected	No connection
RSVDL	11	Reserved	Reserved, must be tied to ground	Ground

## 8. Feature Information

### 8.1. Video Path

The SiI9233A receiver accepts all valid HDMI input formats and can transform that video in a variety of ways to produce the proper video output format. The following pages describe how to control the video path formatting and how to assign output pins for each video output format. The processing blocks shown in [Figure 8.1](#) correspond to those shown in [Figure 8.2](#) through [Figure 8.4](#) on pages 41 through 43.



**Figure 8.1. Receiver Video and Audio Data Processing Paths**

#### 8.1.1. HDMI Input Modes to SiI9233A Receiver Output Modes

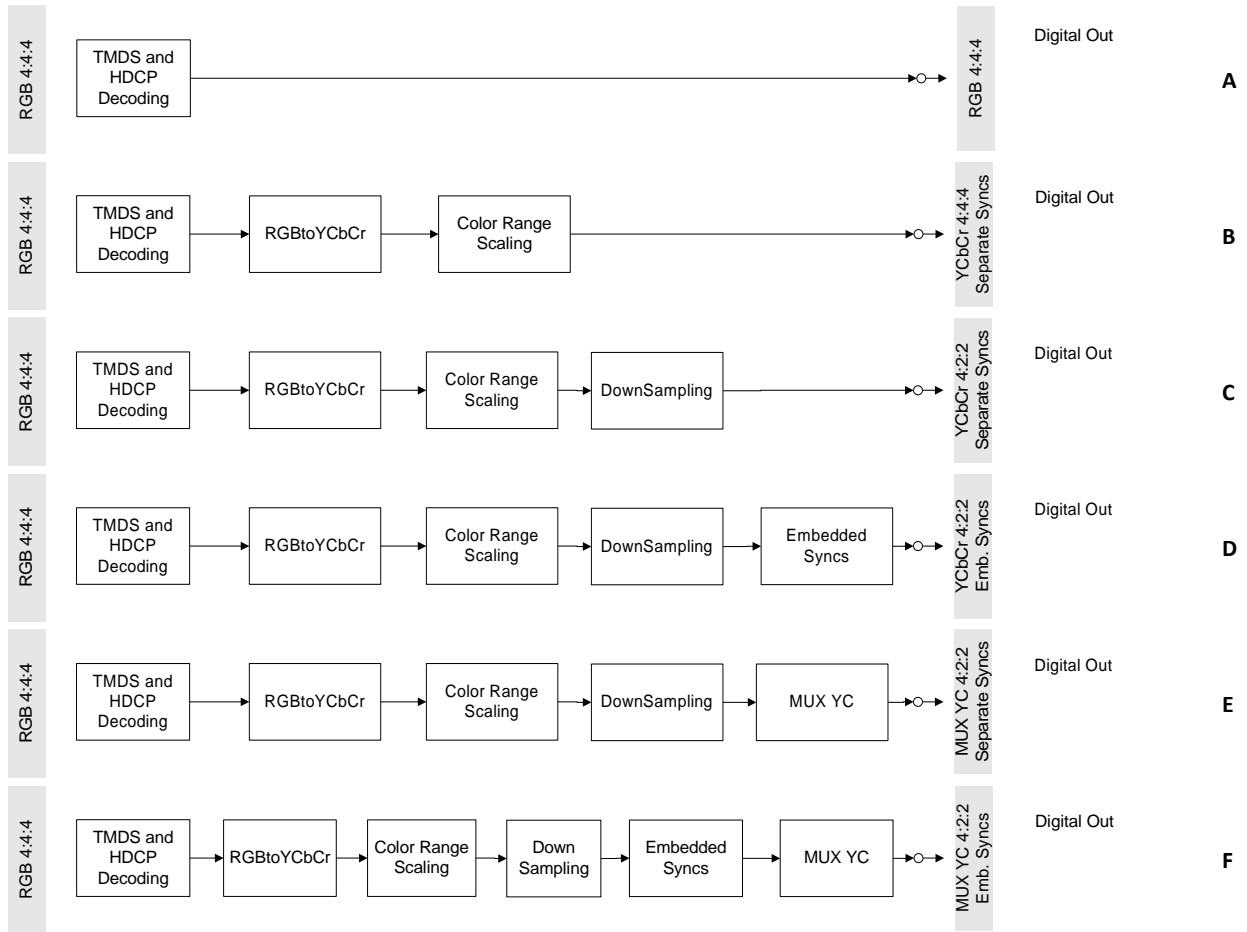
The HDMI link supports transport of video in any of three modes: RGB 4:4:4, YCbCr 4:4:4 or YCbCr 4:2:2. The flexible video path in the SiI9233A receiver allows reformatting of video data to a set of output modes. [Table 8.1](#) lists the supported transformations and points to the figure for each. In every case, the HDMI link itself carries separate syncs.

**Table 8.1. Translating HDMI Formats to Output Formats**

HDMI Input Mode	Digital Output Format					
	RGB 4:4:4 Separate Sync	YCbCr 4:4:4 Separate Sync	YCbCr 4:2:2 Separate Sync	YCbCr 4:2:2 Embedded Sync	YC Mux Separate Sync	YC Mux Embedded Sync
RGB 4:4:4	<a href="#">Figure 8.2A</a>	<a href="#">Figure 8.2B</a>	<a href="#">Figure 8.2C</a>	<a href="#">Figure 8.2D</a>	<a href="#">Figure 8.2E</a>	<a href="#">Figure 8.2F</a>
YCbCr/xvYCC 4:4:4	<a href="#">Figure 8.3A</a>	<a href="#">Figure 8.3B</a>	<a href="#">Figure 8.3C</a>	<a href="#">Figure 8.3D</a>	<a href="#">Figure 8.3E</a>	<a href="#">Figure 8.3F</a>
YCbCr/xvYCC 4:2:2	<a href="#">Figure 8.4A</a>	<a href="#">Figure 8.4B</a>	<a href="#">Figure 8.4C</a>	<a href="#">Figure 8.4D</a>	<a href="#">Figure 8.4E</a>	<a href="#">Figure 8.4F</a>



**8.1.1.1. HDMI RGB 4:4:4 Input Processing**



**Figure 8.2. HDMI RGB 4:4:4 Input to Video Output Transformations**

### 8.1.1.2. HDMI YCbCr/xvYCC 4:4:4 Input Processing

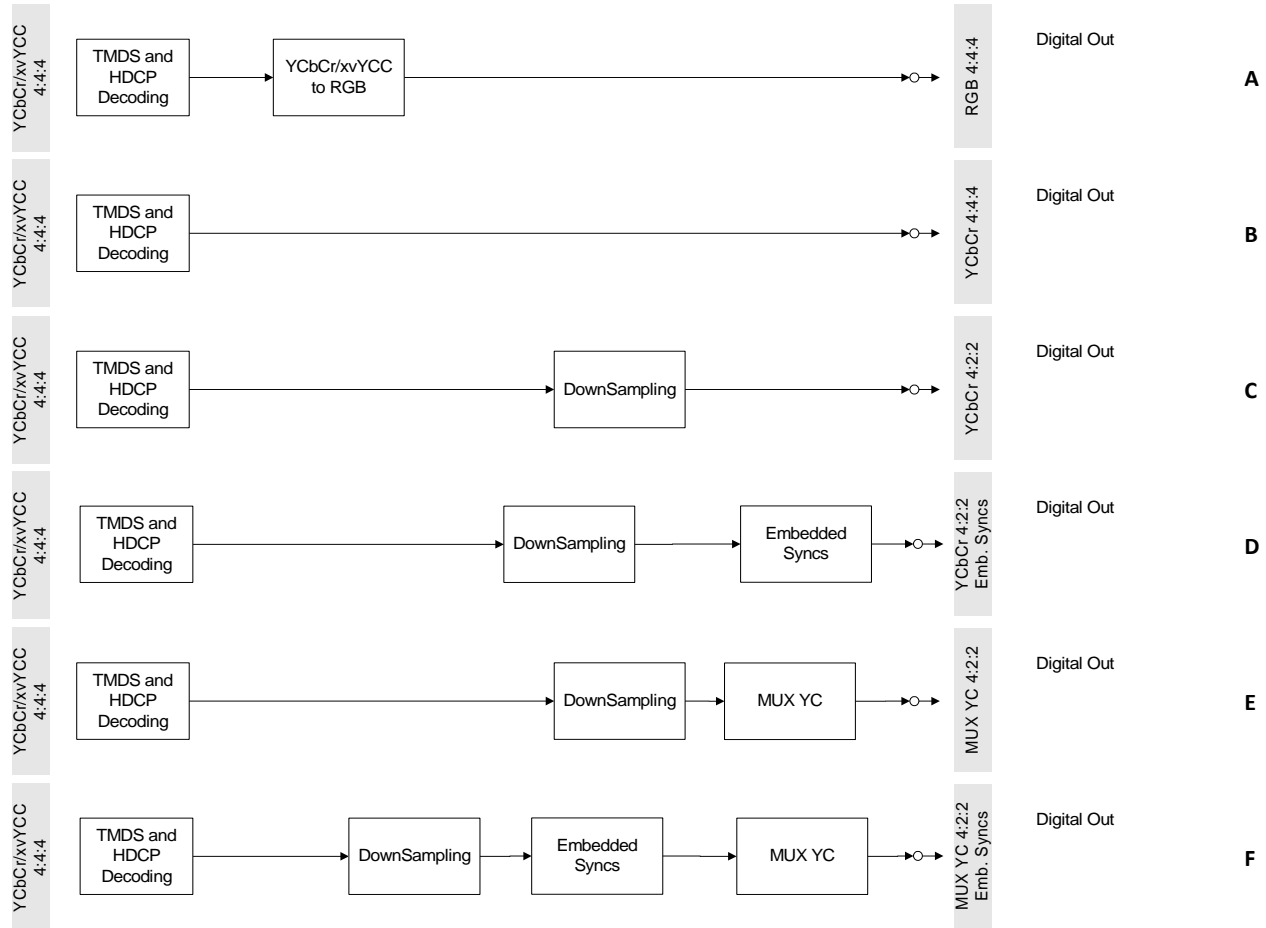
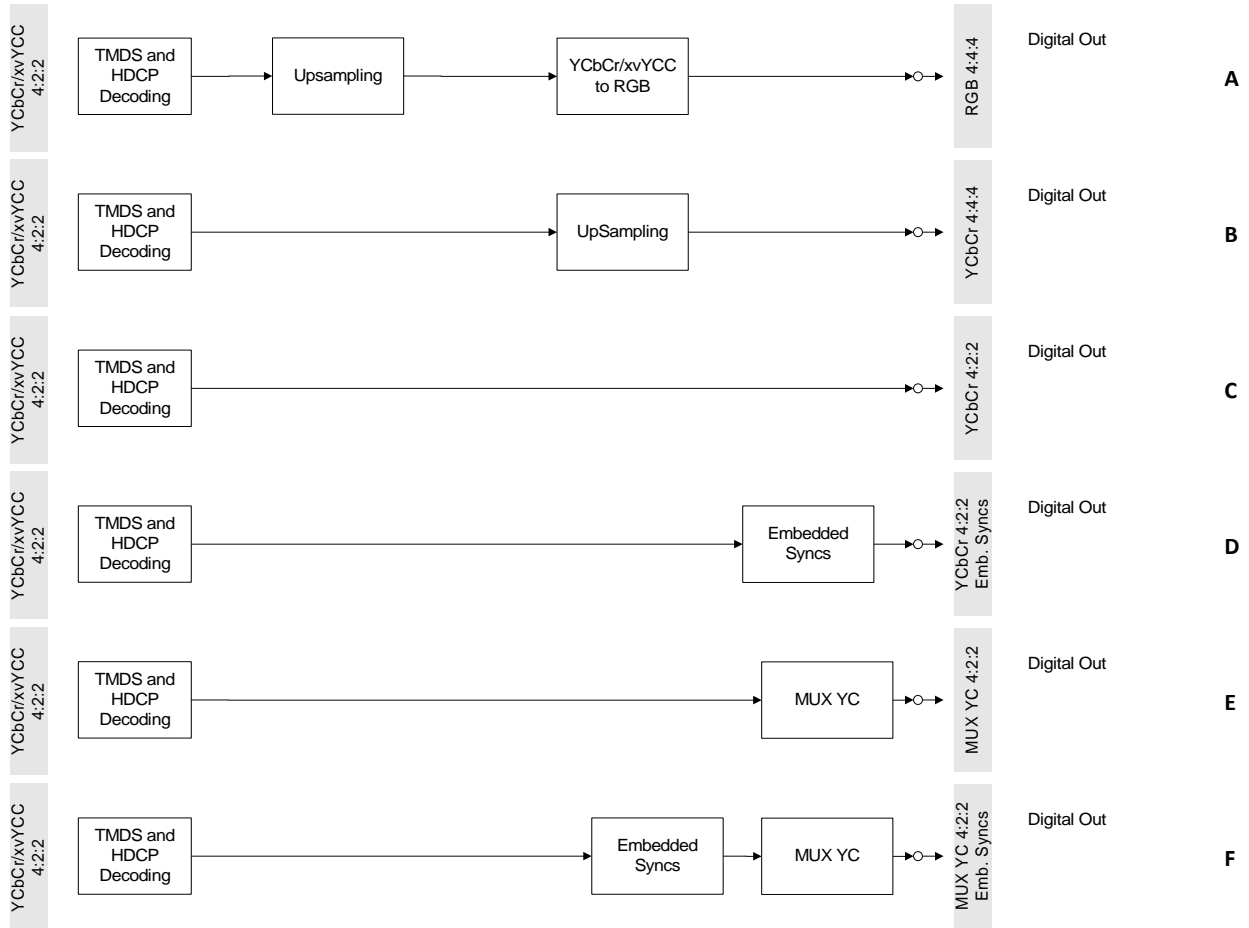


Figure 8.3. HDMI YCbCr/xvYCC 4:4:4 Input to Video Output Transformations

**8.1.1.3. HDMI YCbCr/xvYCC 4:2:2 Input Processing**



**Figure 8.4. HDMI YCbCr/xvYCC 4:2:2 Input to Video Output Transformations**

### 8.1.2. Output Mode Configuration

The SiI9233A receiver supports multiple output data mappings. Some have separate control signals while some have embedded control signals. The selection of data mapping mode should be consistent at the pins and in the corresponding register settings. Refer to the Programmer Reference for more details.

**Table 8.2. Output Video Formats**

Output Mode	Data Widths	Pixel Replication	Syncs	Page	Notes
RGB 4:4:4	24, 30, 36	1x	Separate	45	3, 7
YCbCr 4:4:4	24, 30, 36	1x	Separate	45	1, 3, 7
YC 4:2:2 Sep. Syncs	16, 20, 24	1x	Separate	47	2, 3
YC 4:2:2 Sep. Syncs	16, 20, 24	2x	Separate	47	2, 3, 8
YC 4:2:2 Emb. Syncs	16, 20, 24	1x	Embedded	50	2, 5
YC MUX 4:2:2	8, 10, 12	2x	Separate	53	2, 4, 8
YC MUX 4:2:2 Emb. Syncs	8, 10, 12	2x	Embedded	55	2, 5, 6, 8, 9

**Notes:**

1. YC 4:4:4 data contains one Cr, one Cb and one Y value for every pixel.
2. YC 4:2:2 data contains one Cr and one Cb value for every two pixels; and one Y value for every pixel.
3. These formats can be carried across the HDMI link. Refer to the *HDMI Specification*, Section 6.2.3. The link clock must be within the specified range of the receiver.
4. In YC MUX mode data is sent to one or two 8/10/12-bit channels.
5. YC MUX with embedded SAV/EAV signal.
6. Syncs are embedded using SAV/EAV codes.
7. A 2x clock can also be sent with 4:4:4 data.
8. When sending a 2x clock the HDMI source must also send AVI InfoFrames with an accurate pixel replication field. Refer to *HDMI Spec 1.3*, Section 6.4.
9. 2x clocking does not support YC 4:2:2 embedded Sync timings for 720p or 1080i, as the output clock frequency would exceed the range allowed for the receiver.

The SiI9233A receiver can output video in various formats on its parallel digital output bus. Some transformation of the data received over HDMI is necessary in some modes. Digital output is used with either 4:4:4 or 4:2:2 data.

The diagrams do not include separation of the audio and InfoFrame packets from the HDMI stream, which occurs immediately after the TMDS and (optional) HDCP decoding. The HDMI link always carries separate HSYNC and VSYNC and DE. Therefore the SAV/EAV sync encoder must be used whenever the output mode includes embedded sync.

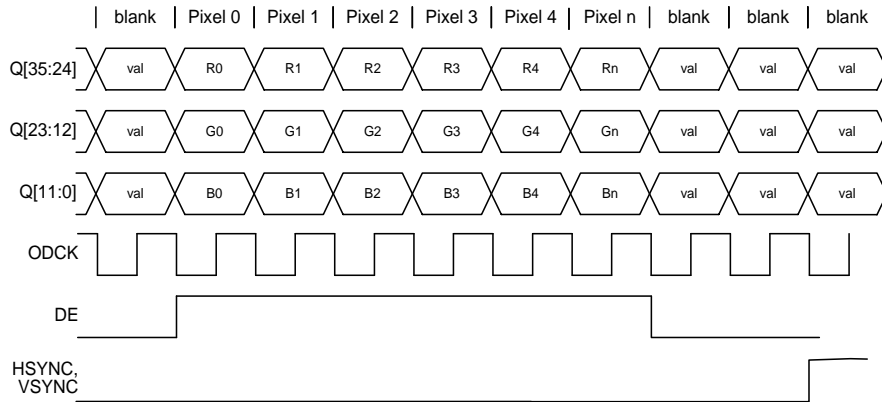
The timing diagrams in [Figure 8.5](#) through [Figure 8.9](#) on pages 46 through 56 show only a representation of the DE, HSYNC and VSYNC timings. These timings are specific to the video resolution, as defined by EIA/CEA-861B and other specs. The number of pixels shown per DE HIGH time is representative, to show the data formatting.

### 8.1.2.1. RGB and YCbCr 4:4:4 Formats with Separate Syncs

The pixel clock runs at the pixel rate and a complete definition of each pixel is output on each clock. Figure 8.5 on the next page shows RGB data. The same timing format is used for YCbCr 4:4:4 as listed in Table 8.3. Figure 8.5 also shows timings with OCLKDIV = 0 and OCKINV = 1.

**Table 8.3. 4:4:4 Mappings**

Pin Name	36-bit	36-bit	30-bit	30-bit	24-bit	24-bit
	RGB	YCbCr	RGB	YCbCr	RGB	YCbCr
Q0	B0	Cb0	NC	NC	NC	NC
Q1	B1	Cb1	NC	NC	NC	NC
Q2	B2	Cb2	B0	Cb0	NC	NC
Q3	B3	Cb3	B1	Cb1	NC	NC
Q4	B4	Cb4	B2	Cb2	B0	Cb0
Q5	B5	Cb5	B3	Cb3	B1	Cb1
Q6	B6	Cb6	B4	Cb4	B2	Cb2
Q7	B7	Cb7	B5	Cb5	B3	Cb3
Q8	B8	Cb8	B6	Cb6	B4	Cb4
Q9	B9	Cb9	B7	Cb7	B5	Cb5
Q10	B10	Cb10	B8	Cb8	B6	Cb6
Q11	B11	Cb11	B9	Cb9	B7	Cb7
Q12	G0	Y0	NC	NC	NC	NC
Q13	G1	Y1	NC	NC	NC	NC
Q14	G2	Y2	G0	Y0	NC	NC
Q15	G3	Y3	G1	Y1	NC	NC
Q16	G4	Y4	G2	Y2	G0	Y0
Q17	G5	Y5	G3	Y3	G1	Y1
Q18	G6	Y6	G4	Y4	G2	Y2
Q19	G7	Y7	G5	Y5	G3	Y3
Q20	G8	Y8	G6	Y6	G4	Y4
Q21	G9	Y9	G7	Y7	G5	Y5
Q22	G10	Y10	G8	Y8	G6	Y6
Q23	G11	Y11	G9	Y9	G7	Y7
Q24	R0	Cr0	NC	NC	NC	NC
Q25	R1	Cr1	NC	NC	NC	NC
Q26	R2	Cr2	R0	Cr0	NC	NC
Q27	R3	Cr3	R1	Cr1	NC	NC
Q28	R4	Cr4	R2	Cr2	R0	Cr0
Q29	R5	Cr5	R3	Cr3	R1	Cr1
Q30	R6	Cr6	R4	Cr4	R2	Cr2
Q31	R7	Cr7	R5	Cr5	R3	Cr3
Q32	R8	Cr8	R6	Cr6	R4	Cr4
Q33	R9	Cr9	R7	Cr7	R5	Cr5
Q34	R10	Cr10	R8	Cr8	R6	Cr6
Q35	R11	Cr11	R9	Cr9	R7	Cr7
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE



**Figure 8.5. 4:4:4 Timing Diagram**

**Note:** The *val* data is defined in various specifications to specific values. These values are controlled by setting the appropriate SiI9233A registers, because no pixel data is carried on HDMI during blanking.

### 8.1.2.2. YC 4:2:2 Formats with Separate Syncs

The YC 4:2:2 formats output one pixel for every pixel clock period. A luminance (Y) value is sent for every pixel, but the chrominance values (Cb and Cr) are sent over two pixels. Pixel data can be 24-bit, 20-bit or 16-bit. HSYNC and VSYNC are output separately on their own pins. The DE HIGH time must contain an even number of pixel clocks. [Figure 8.6](#) on page 49 shows timings with OCLKDIV = 0 and OCKINV = 1.

**Table 8.4. YC 4:2:2 Separate Sync Pin Mappings**

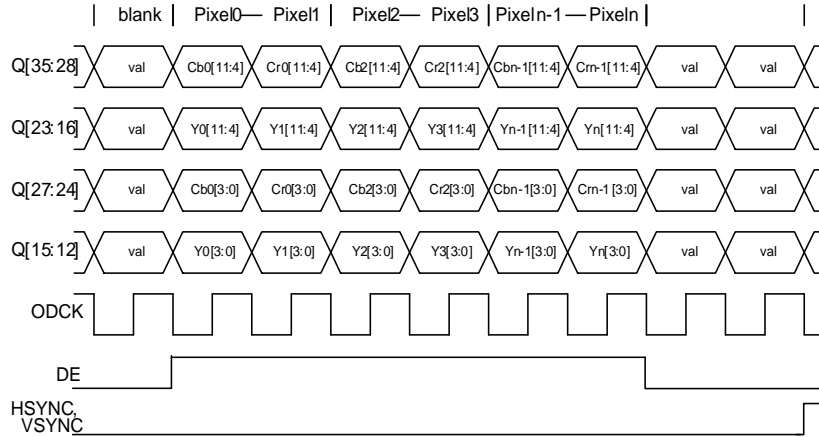
Pin Name	16-bit YC		20-bit YC		24-bit YC	
	Pixel #0	Pixel #1	Pixel #0	Pixel #1	Pixel #0	Pixel #1
Q0	NC	NC	NC	NC	NC	NC
Q1	NC	NC	NC	NC	NC	NC
Q2	NC	NC	NC	NC	NC	NC
Q3	NC	NC	NC	NC	NC	NC
Q4	NC	NC	NC	NC	NC	NC
Q5	NC	NC	NC	NC	NC	NC
Q6	NC	NC	NC	NC	NC	NC
Q7	NC	NC	NC	NC	NC	NC
Q8	NC	NC	NC	NC	NC	NC
Q9	NC	NC	NC	NC	NC	NC
Q10	NC	NC	NC	NC	NC	NC
Q11	NC	NC	NC	NC	NC	NC
Q12	NC	NC	NC	NC	Y0	Y0
Q13	NC	NC	NC	NC	Y1	Y1
Q14	NC	NC	Y0	Y0	Y2	Y2
Q15	NC	NC	Y1	Y1	Y3	Y3
Q16	Y0	Y0	Y2	Y2	Y4	Y4
Q17	Y1	Y1	Y3	Y3	Y5	Y5
Q18	Y2	Y2	Y4	Y4	Y6	Y6
Q19	Y3	Y3	Y5	Y5	Y7	Y7
Q20	Y4	Y4	Y6	Y6	Y8	Y8
Q21	Y5	Y5	Y7	Y7	Y9	Y9
Q22	Y6	Y6	Y8	Y8	Y10	Y10
Q23	Y7	Y7	Y9	Y9	Y11	Y11
Q24	NC	NC	NC	NC	Cb0	Cr0
Q25	NC	NC	NC	NC	Cb1	Cr1
Q26	NC	NC	Cb0	Cr0	Cb2	Cr2
Q27	NC	NC	Cb1	Cr1	Cb3	Cr3
Q28	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4
Q29	Cb1	Cr1	Cb3	Cr3	Cb5	Cr5
Q30	Cb2	Cr2	Cb4	Cr4	Cb6	Cr6
Q31	Cb3	Cr3	Cb5	Cr5	Cb7	Cr7
Q32	Cb4	Cr4	Cb6	Cr6	Cb8	Cr8
Q33	Cb5	Cr5	Cb7	Cr7	Cb9	Cr9
Q34	Cb6	Cr6	Cb8	Cr8	Cb10	Cr10
Q35	Cb7	Cr7	Cb9	Cr9	Cb11	Cr11
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE

**Table 8.5. YC 4:2:2 (Pass Through Only) Separate Sync Pin Mapping**

Pin Name	16-bit YC		20-bit YC		24-bit YC	
	Pixel #0	Pixel #1	Pixel #0	Pixel #1	Pixel #0	Pixel #1
Q0	NC	NC	NC	NC	NC	NC
Q1	NC	NC	NC	NC	NC	NC
Q2	NC	NC	NC	NC	NC	NC
Q3	NC	NC	NC	NC	NC	NC
Q4	NC	NC	NC	NC	Y0	Y0
Q5	NC	NC	NC	NC	Y1	Y1
Q6	NC	NC	Y0	Y0	Y2	Y2
Q7	NC	NC	Y1	Y1	Y3	Y3
Q8	NC	NC	NC	NC	Cb0	Cr0
Q9	NC	NC	NC	NC	Cb1	Cr1
Q10	NC	NC	Cb0	Cr0	Cb2	Cr2
Q11	NC	NC	Cb1	Cr1	Cb3	Cr3
Q12	NC	NC	NC	NC	NC	NC
Q13	NC	NC	NC	NC	NC	NC
Q14	NC	NC	NC	NC	NC	NC
Q15	NC	NC	NC	NC	NC	NC
Q16	Y0	Y0	Y2	Y2	Y4	Y4
Q17	Y1	Y1	Y3	Y3	Y5	Y5
Q18	Y2	Y2	Y4	Y4	Y6	Y6
Q19	Y3	Y3	Y5	Y5	Y7	Y7
Q20	Y4	Y4	Y6	Y6	Y8	Y8
Q21	Y5	Y5	Y7	Y7	Y9	Y9
Q22	Y6	Y6	Y8	Y8	Y10	Y10
Q23	Y7	Y7	Y9	Y9	Y11	Y11
Q24	NC	NC	NC	NC	NC	NC
Q25	NC	NC	NC	NC	NC	NC
Q26	NC	NC	NC	NC	NC	NC
Q27	NC	NC	NC	NC	NC	NC
Q28	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4
Q29	Cb1	Cr1	Cb3	Cr3	Cb5	Cr5
Q30	Cb2	Cr2	Cb4	Cr4	Cb6	Cr6
Q31	Cb3	Cr3	Cb5	Cr5	Cb7	Cr7
Q32	Cb4	Cr4	Cb6	Cr6	Cb8	Cr8
Q33	Cb5	Cr5	Cb7	Cr7	Cb9	Cr9
Q34	Cb6	Cr6	Cb8	Cr8	Cb10	Cr10
Q35	Cb7	Cr7	Cb9	Cr9	Cb11	Cr11
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE

**Note:** This pin mapping is only valid when the input video format is YC 4:2:2 and the output video format is YC 4:2:2 also. No video processing block should be enabled when this pin mapping is used.





**Figure 8.6. YC Timing Diagram**

**Note:** The *val* data is defined in various specifications to specific values. These values are controlled by setting the appropriate SiI9233A registers, because no pixel data is carried on HDMI during blanking.

### 8.1.2.3. YC 4:2:2 Formats with Embedded Syncs

The YC 4:2:2 embedded sync format is identical to the previous format (YC 4:2:2), except that the syncs are embedded and not separate. Pixel data can be 24-bit, 20-bit or 16-bit. DE is always output. Figure 8.7 on page 52 shows the Start of Active Video (SAV) preamble, the End of Active Video” (EAV) suffix, and shows timings with OCLKDIV = 0 and OCKINV = 1.

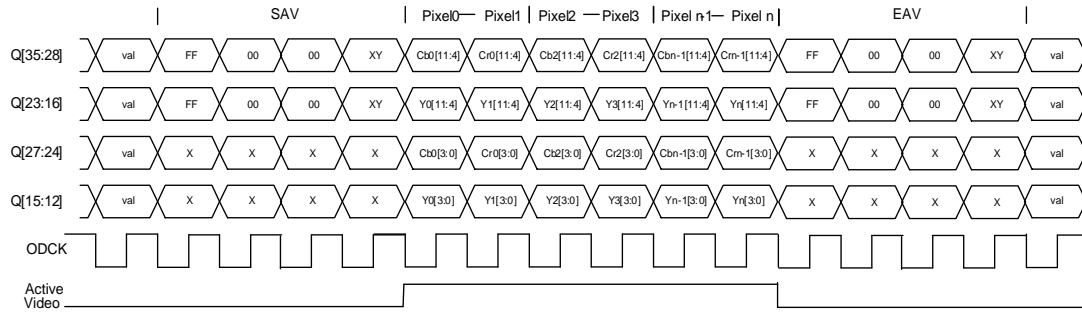
**Table 8.6. YC 4:2:2 Embedded Sync Pin Mappings**

Pin Name	16-bit YC		20-bit YC		24-bit YC	
	Pixel #0	Pixel #1	Pixel #0	Pixel #1	Pixel #0	Pixel #1
Q0	NC	NC	NC	NC	NC	NC
Q1	NC	NC	NC	NC	NC	NC
Q2	NC	NC	NC	NC	NC	NC
Q3	NC	NC	NC	NC	NC	NC
Q4	NC	NC	NC	NC	NC	NC
Q5	NC	NC	NC	NC	NC	NC
Q6	NC	NC	NC	NC	NC	NC
Q7	NC	NC	NC	NC	NC	NC
Q8	NC	NC	NC	NC	NC	NC
Q9	NC	NC	NC	NC	NC	NC
Q10	NC	NC	NC	NC	NC	NC
Q11	NC	NC	NC	NC	NC	NC
Q12	NC	NC	NC	NC	Y0	Y0
Q13	NC	NC	NC	NC	Y1	Y1
Q14	NC	NC	Y0	Y0	Y2	Y2
Q15	NC	NC	Y1	Y1	Y3	Y3
Q16	Y0	Y0	Y2	Y2	Y4	Y4
Q17	Y1	Y1	Y3	Y3	Y5	Y5
Q18	Y2	Y2	Y4	Y4	Y6	Y6
Q19	Y3	Y3	Y5	Y5	Y7	Y7
Q20	Y4	Y4	Y6	Y6	Y8	Y8
Q21	Y5	Y5	Y7	Y7	Y9	Y9
Q22	Y6	Y6	Y8	Y8	Y10	Y10
Q23	Y7	Y7	Y9	Y9	Y11	Y11
Q24	NC	NC	NC	NC	Cb0	Cr0
Q25	NC	NC	NC	NC	Cb1	Cr1
Q26	NC	NC	Cb0	Cr0	Cb2	Cr2
Q27	NC	NC	Cb1	Cr1	Cb3	Cr3
Q28	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4
Q29	Cb1	Cr1	Cb3	Cr3	Cb5	Cr5
Q30	Cb2	Cr2	Cb4	Cr4	Cb6	Cr6
Q31	Cb3	Cr3	Cb5	Cr5	Cb7	Cr7
Q32	Cb4	Cr4	Cb6	Cr6	Cb8	Cr8
Q33	Cb5	Cr5	Cb7	Cr7	Cb9	Cr9
Q34	Cb6	Cr6	Cb8	Cr8	Cb10	Cr10
Q35	Cb7	Cr7	Cb9	Cr9	Cb11	Cr11
HSYNC	Embedded	Embedded	Embedded	Embedded	Embedded	Embedded
VSYNC	Embedded	Embedded	Embedded	Embedded	Embedded	Embedded
DE	Embedded	Embedded	Embedded	Embedded	Embedded	Embedded

**Table 8.7. YC 4:2:2 (Pass Through Only) Embedded Sync Pin Mapping**

Pin Name	16-bit YC		20-bit YC		24-bit YC	
	Pixel #0	Pixel #1	Pixel #0	Pixel #1	Pixel #0	Pixel #1
Q0	NC	NC	NC	NC	NC	NC
Q1	NC	NC	NC	NC	NC	NC
Q2	NC	NC	NC	NC	NC	NC
Q3	NC	NC	NC	NC	NC	NC
Q4	NC	NC	NC	NC	Y0	Y0
Q5	NC	NC	NC	NC	Y1	Y1
Q6	NC	NC	Y0	Y0	Y2	Y2
Q7	NC	NC	Y1	Y1	Y3	Y3
Q8	NC	NC	NC	NC	Cb0	Cr0
Q9	NC	NC	NC	NC	Cb1	Cr1
Q10	NC	NC	Cb0	Cr0	Cb2	Cr2
Q11	NC	NC	Cb1	Cr1	Cb3	Cr3
Q12	NC	NC	NC	NC	NC	NC
Q13	NC	NC	NC	NC	NC	NC
Q14	NC	NC	NC	NC	NC	NC
Q15	NC	NC	NC	NC	NC	NC
Q16	Y0	Y0	Y2	Y2	Y4	Y4
Q17	Y1	Y1	Y3	Y3	Y5	Y5
Q18	Y2	Y2	Y4	Y4	Y6	Y6
Q19	Y3	Y3	Y5	Y5	Y7	Y7
Q20	Y4	Y4	Y6	Y6	Y8	Y8
Q21	Y5	Y5	Y7	Y7	Y9	Y9
Q22	Y6	Y6	Y8	Y8	Y10	Y10
Q23	Y7	Y7	Y9	Y9	Y11	Y11
Q24	NC	NC	NC	NC	NC	NC
Q25	NC	NC	NC	NC	NC	NC
Q26	NC	NC	NC	NC	NC	NC
Q27	NC	NC	NC	NC	NC	NC
Q28	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4
Q29	Cb1	Cr1	Cb3	Cr3	Cb5	Cr5
Q30	Cb2	Cr2	Cb4	Cr4	Cb6	Cr6
Q31	Cb3	Cr3	Cb5	Cr5	Cb7	Cr7
Q32	Cb4	Cr4	Cb6	Cr6	Cb8	Cr8
Q33	Cb5	Cr5	Cb7	Cr7	Cb9	Cr9
Q34	Cb6	Cr6	Cb8	Cr8	Cb10	Cr10
Q35	Cb7	Cr7	Cb9	Cr9	Cb11	Cr11
HSYNC	Embedded	Embedded	Embedded	Embedded	Embedded	Embedded
VSYNC	Embedded	Embedded	Embedded	Embedded	Embedded	Embedded
DE	Embedded	Embedded	Embedded	Embedded	Embedded	Embedded

**Note:** This pin mapping is only valid when the input video format is YC 4:2:2 and the output video format is YC 4:2:2 also. No video processing block should be enabled when this pin mapping is used.



**Figure 8.7. YC 4:2:2 Embedded Sync Timing Diagram**

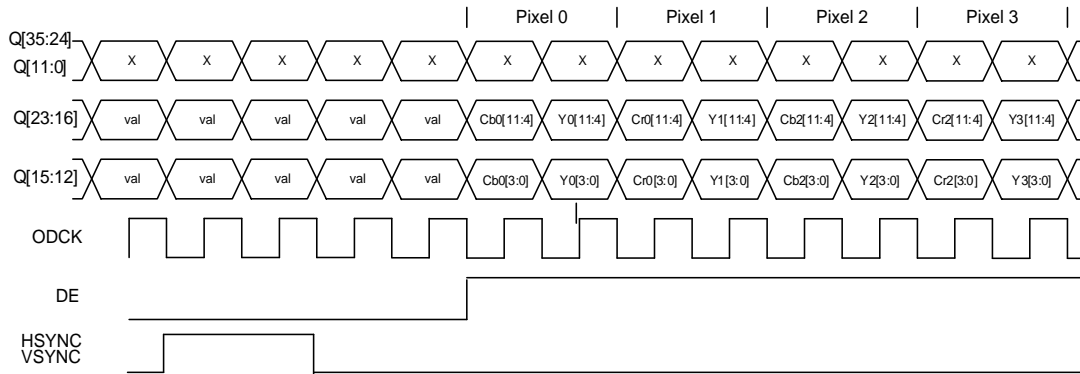
**Note:** The val data is defined in various specifications to specific values. These values are controlled by setting the appropriate SiI9233A registers, because no pixel data is carried on HDMI during blanking. SAV/EAV codes appear as an 8-bit field on both Q[35:28] (per SMPTE) and Q[23:16].

#### 8.1.2.4. YC Mux (4:2:2) Formats with Separate Syncs

The video data is multiplexed onto fewer pins than the mapping in Table 8.8, but complete luminance (Y) and chrominance (Cb and Cr) data is still provided for each pixel because the output pixel clock runs at twice the pixel rate. Figure 8.8 on the next page shows the 24-bit mode. The 16- and 20-bit mappings use fewer output pins for the pixel data. Note the separate syncs. Figure 8.8 also shows OCLKDIV = 0 and OCKINV = 1.

**Table 8.8. YC Mux 4:2:2 Mappings**

Pin Name	8-bit	10-bit	12-bit
	YCbCr	YCbCr	YCbCr
Q0	NC	NC	NC
Q1	NC	NC	NC
Q2	NC	NC	NC
Q3	NC	NC	NC
Q4	NC	NC	NC
Q5	NC	NC	NC
Q6	NC	NC	NC
Q7	NC	NC	NC
Q8	NC	NC	NC
Q9	NC	NC	NC
Q10	NC	NC	NC
Q11	NC	NC	NC
Q12	NC	NC	D0
Q13	NC	NC	D1
Q14	NC	D0	D2
Q15	NC	D1	D3
Q16	D0	D2	D4
Q17	D1	D3	D5
Q18	D2	D4	D6
Q19	D3	D5	D7
Q20	D4	D6	D8
Q21	D5	D7	D9
Q22	D6	D8	D10
Q23	D7	D9	D11
Q24	NC	NC	NC
Q25	NC	NC	NC
Q26	NC	NC	NC
Q27	NC	NC	NC
Q28	NC	NC	NC
Q29	NC	NC	NC
Q30	NC	NC	NC
Q31	NC	NC	NC
Q32	NC	NC	NC
Q33	NC	NC	NC
Q34	NC	NC	NC
Q35	NC	NC	NC
HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE



**Figure 8.8. YC Mux 4:2:2 Timing Diagram**

**Note:** The *val* data is defined in various specifications to specific values. These values are controlled by setting the appropriate SiI9233A registers, because no pixel data is carried on HDMI during blanking.

### 8.1.2.5. YC Mux 4:2:2 Formats with Embedded Syncs

This mode is similar to that shown in [Figure 8.7](#) on page 53, but with embedded syncs. It is similar to YC 4:2:2 with embedded syncs, but also multiplexes the luminance (Y) and chrominance (Cb and Cr) onto the same pins on alternating pixel clock cycles. Normally this mode is used only for 480i, 480p, 576i and 576p modes. Output clock rate is half the pixel clock rate on the link. SAV code is shown before rise of DE. EAV follows the falling edge of DE. See the ITU-R BT.656 Specification. 480p, 54-MHz output can be achieved if the input differential clock is 54 MHz. [Figure 8.9](#) on the next page shows OCLKDIV = 0 and OCKINV = 1.

**Table 8.9. YC Mux 4:2:2 Embedded Sync Pin Mapping**

Pin Name	8-bit	10-bit	12-bit
	YCbCr	YCbCr	YCbCr
Q0	NC	NC	NC
Q1	NC	NC	NC
Q2	NC	NC	NC
Q3	NC	NC	NC
Q4	NC	NC	NC
Q5	NC	NC	NC
Q6	NC	NC	NC
Q7	NC	NC	NC
Q8	NC	NC	NC
Q9	NC	NC	NC
Q10	NC	NC	NC
Q11	NC	NC	NC
Q12	NC	NC	D0
Q13	NC	NC	D1
Q14	NC	D0	D2
Q15	NC	D1	D3
Q16	D0	D2	D4
Q17	D1	D3	D5
Q18	D2	D4	D6
Q19	D3	D5	D7
Q20	D4	D6	D8
Q21	D5	D7	D9
Q22	D6	D8	D10
Q23	D7	D9	D11
Q24	NC	NC	NC
Q25	NC	NC	NC
Q26	NC	NC	NC
Q27	NC	NC	NC
Q28	NC	NC	NC
Q29	NC	NC	NC
Q30	NC	NC	NC
Q31	NC	NC	NC
Q32	NC	NC	NC
Q33	NC	NC	NC
Q34	NC	NC	NC
Q35	NC	NC	NC
HSYNC	Embedded	Embedded	Embedded
VSYNC	Embedded	Embedded	Embedded
DE	Embedded	Embedded	Embedded

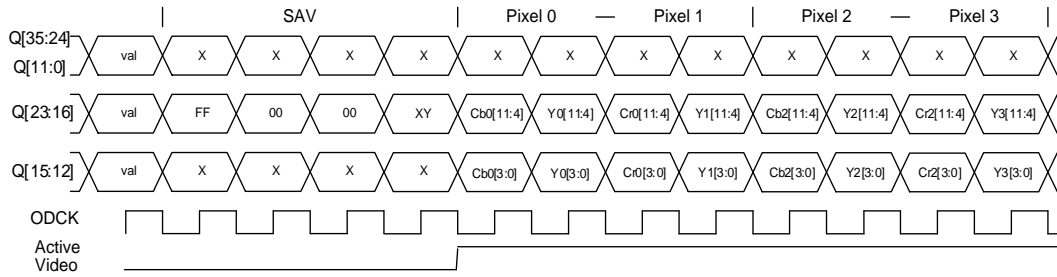


Figure 8.9. YC Mux 4:2:2 Embedded Sync Encoding Timing Diagram

**Note:** The *val* data is defined in various specifications to specific values. These values are controlled by setting the appropriate SiI9233A registers, because no pixel data is carried on HDMI during blanking. Refer to the Programmer Reference for details.

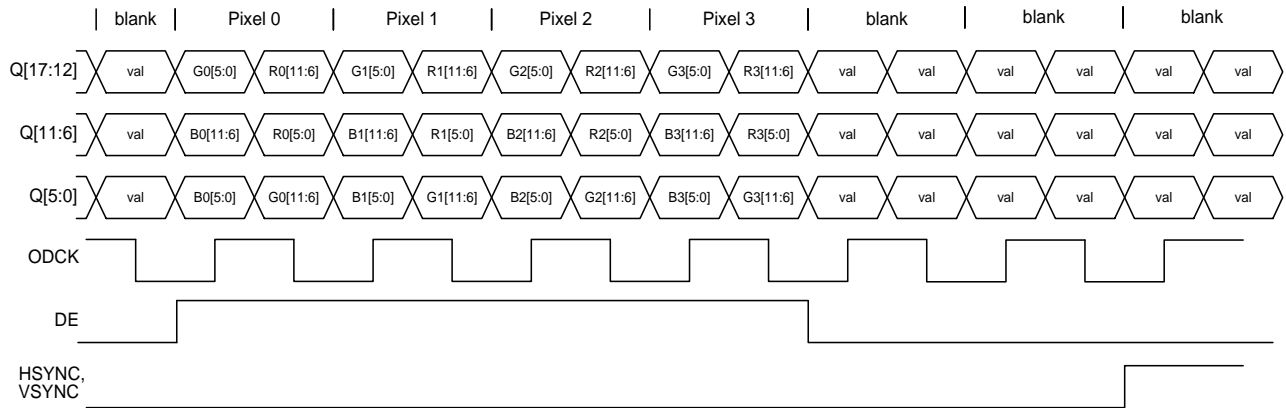
**8.1.2.6. 12/15/18-Bit RGB and YCbCr 4:4:4 Formats with Separate Syncs**

The output clock runs at the pixel rate and a complete definition of each pixel is output on each clock. One clock edge drives out half the pixel data on 12/15/18 pins. The opposite clock edge drives out the remaining half of the pixel data on the same 12/15/18 pins. Figure 8.10 below shows RGB data. The same timing format is used for YCbCr 4:4:4 as listed in the columns of Table 8.10. Control signals (DE, HSYNC and VSYNC) change state with respect to the first edge of ODCK.

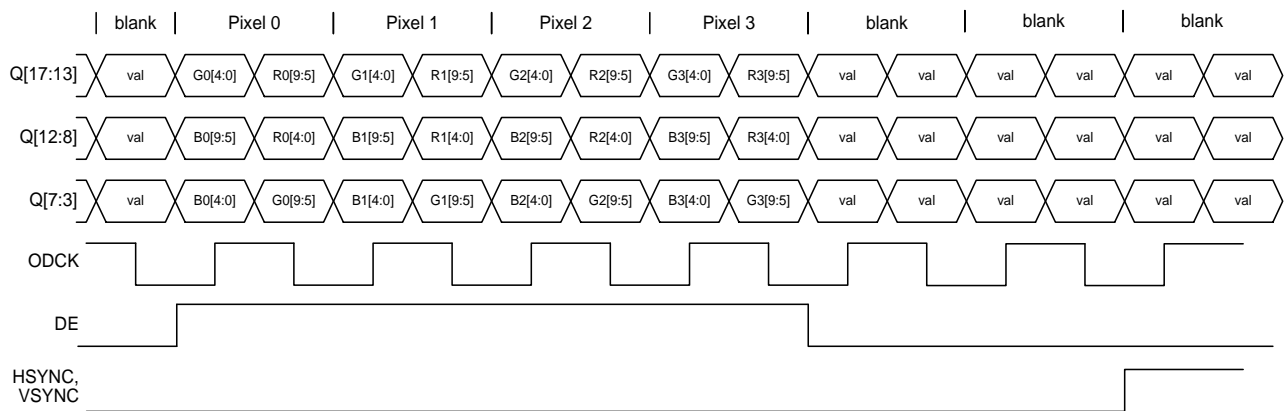
Table 8.10. 12/15/18-Bit Output 4:4:4 Mappings

Pin Name	24-bit				30-bit				36-bit			
	RGB		YCbCr		RGB		YCbCr		RGB		YCbCr	
	First Edge	Second Edge	First Edge	Second Edge	First Edge	Second Edge	First Edge	Second Edge	First Edge	Second Edge	First Edge	Second Edge
Q0	NC	NC	NC	NC	NC	NC	NC	NC	B0	G6	Cb0	Y6
Q1	NC	NC	NC	NC	NC	NC	NC	NC	B1	G7	Cb1	Y7
Q2	NC	NC	NC	NC	NC	NC	NC	NC	B2	G8	Cb2	Y8
Q3	NC	NC	NC	NC	B0	G5	Cb0	Y5	B3	G9	Cb3	Y9
Q4	NC	NC	NC	NC	B1	G6	Cb1	Y6	B4	G10	Cb4	Y10
Q5	NC	NC	NC	NC	B2	G7	Cb2	Y7	B5	G11	Cb5	Y11
Q6	B0	G4	Cb0	Y4	B3	G8	Cb3	Y8	B6	R0	Cb6	Cr0
Q7	B1	G5	Cb1	Y5	B4	G9	Cb4	Y9	B7	R1	Cb7	Cr1
Q8	B2	G6	Cb2	Y6	B5	R0	Cb5	Cr0	B8	R2	Cb8	Cr2
Q9	B3	G7	Cb3	Y7	B6	R1	Cb6	Cr1	B9	R3	Cb9	Cr3
Q10	B4	R0	Cb4	Cr0	B7	R2	Cb7	Cr2	B10	R4	Cb10	Cr4
Q11	B5	R1	Cb5	Cr1	B8	R3	Cb8	Cr3	B11	R5	Cb11	Cr5
Q12	B6	R2	Cb6	Cr2	B9	R4	Cb9	Cr4	G0	R6	Y0	Cr6
Q13	B7	R3	Cb7	Cr3	G0	R5	Y0	Cr5	G1	R7	Y1	Cr7
Q14	G0	R4	Y0	Cr4	G1	R6	Y1	Cr6	G2	R8	Y2	Cr8
Q15	G1	R5	Y1	Cr5	G2	R7	Y2	Cr7	G3	R9	Y3	Cr9
Q16	G2	R6	Y2	Cr6	G3	R8	Y3	Cr8	G4	R10	Y4	Cr10
Q17	G3	R7	Y3	Cr7	G4	R9	Y4	Cr9	G5	R11	Y5	Cr11
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE

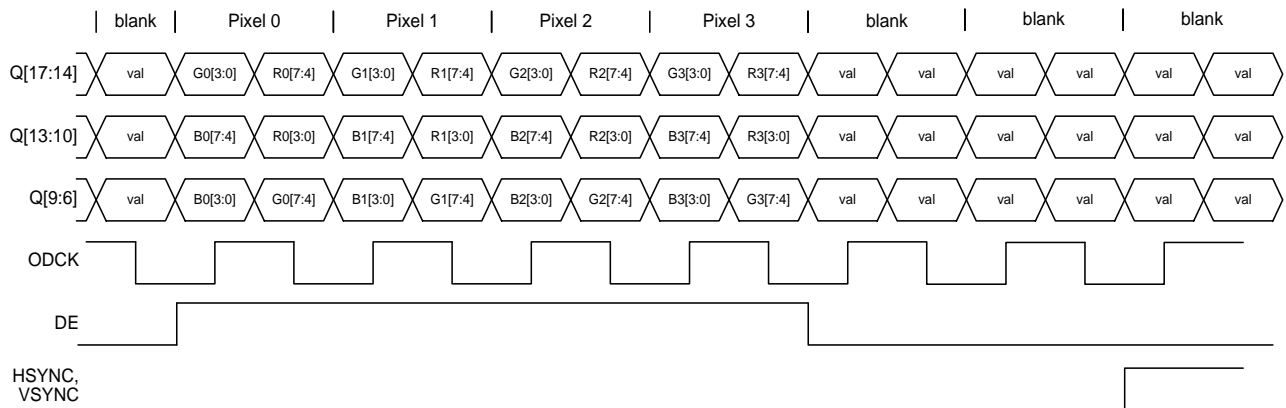




**Figure 8.10. 18-Bit Output 4:4:4 Timing Diagram**



**Figure 8.11. 15-Bit Output 4:4:4 Timing Diagram**



**Figure 8.12. 12-Bit Output 4:4:4 Timing Diagram**

## 8.2. I<sup>2</sup>C Interfaces

### 8.2.1. HDCP E-DDC / I<sup>2</sup>C Interface

The HDCP protocol requires values to be exchanged between the video transmitter and video receiver. These values are exchanged over the DDC channel of the DVI interface. The E-DDC channel follows the I<sup>2</sup>C serial protocol. The SiI9233A device is the video receiver in a system design using an SiI9233A receiver, and it has a connection to the E-DDC bus with a slave address of 0x74. The I<sup>2</sup>C read operation is shown in Figure 8.13, and the write operation in Figure 8.14.

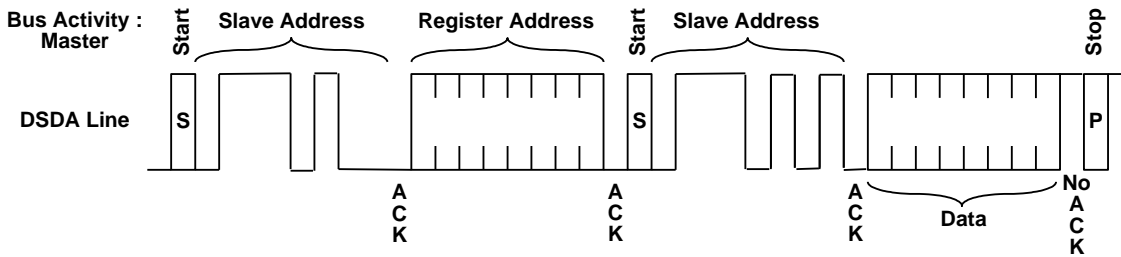


Figure 8.13. I<sup>2</sup>C Byte Read

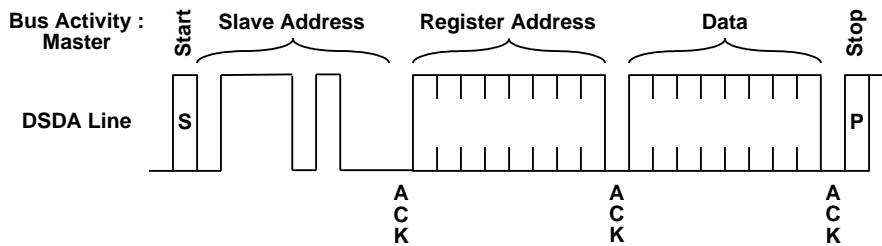


Figure 8.14. I<sup>2</sup>C Byte Write

Multiple bytes can be transferred in each transaction, regardless of whether they are reads or writes. The operations are similar to those in Figure 8.13 and Figure 8.14 except that there is more than one data phase. An ACK follows each byte except the last byte in a read operation. Byte addresses increment, with the least significant byte transferred first, and the most significant byte last. See the I<sup>2</sup>C specification for more information.

There is also a “Short Read” format, designed to improve the efficiency of Ri register reads (which must be done every two seconds while encryption is enabled). This transaction is shown in Figure 8.15. Note that there is no register address phase (only the slave address phase), because the register address is reset to 0x08 (Ri) after a hardware or software reset, and after the STOP condition on any preceding I<sup>2</sup>C transaction.

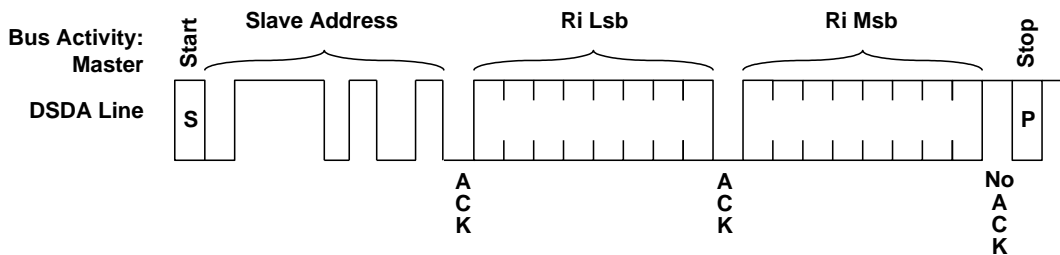


Figure 8.15. Short Read Sequence

### 8.2.2. Local I<sup>2</sup>C Interface

The SiI9233A receiver has a second I<sup>2</sup>C port accessible only to the controller in the display device. It is separate from the E-DDC bus. The SiI9233A receiver is a slave device that responds to six binary I<sup>2</sup>C device addresses of seven bits each. This I<sup>2</sup>C interface only supports the read operation shown in Figure 8.13 on the previous page, and the write operation shown in Figure 8.14 on the previous page. It does not support the short read operation shown in Figure 8.15 on the previous page. Note that the I<sup>2</sup>C data pin for the local I<sup>2</sup>C bus is CSDA, instead of the DSDA pin shown in these figures.

The local I<sup>2</sup>C interface on SiI9233A pins CSCL and CSDA is a slave interface that can run up to 400 kHz. This bus is used to configure and control the receiver by reading/writing to necessary registers.

The local I<sup>2</sup>C interface consists of 5 separate I<sup>2</sup>C slave addresses. Therefore, it appears as 5 separate devices on the I<sup>2</sup>C local bus. The first two of these addresses, used for HDMI Control and general low level register control, are fixed, and can only be set to one of two values by using the CI2CA pin. Table 8.11 shows the address selected for each state of the CI2CA pin at reset. The other 3 addresses (used for CEC, EDID, and xvYCC) have an I<sup>2</sup>C register programmable address mapped into the HDMI Control register space, so the default value can be changed if there is a bus conflict with another device.

**Table 8.11. Control of the Default I<sup>2</sup>C Addresses with the CI2CA Pin**

Register Group	CI2CA = LOW	CI2CA = HIGH
HDMI Control and low level registers (fixed)	0x60 & 0x68	0x62 & 0x6A

The HDMI Control and low level registers are fixed after reset based on CI2CA pin and cannot be changed. The I<sup>2</sup>C slave address for the xvYCC registers, EDID Control registers, and the CEC Control registers each have a register associated with them that allows the address to be changed. See the Programmer Reference for more information.

### 8.2.3. Video Requirement for I<sup>2</sup>C Access

The SiI9233A receiver does not require an active video clock to access its registers from either the E-DDC port or the local I<sup>2</sup>C port. Read-Write registers can be written and then read back. Read-only registers that provide values for an active video or audio stream return indeterminate values if there is no video clock and no active syncs.

Use the SCDT and CKDT register bits to determine when active video is being received by the chip.

### 8.2.4. I<sup>2</sup>C Registers

The register values that are exchanged over the HDMI DDC I<sup>2</sup>C serial interface with the receiver for HDCP are described in the HDCP 1.3 Specification in Section 2.6 – HDCP Port. Refer to the Programmer Reference for details on these and all other SiI9233A registers.

## 9. Design Recommendations

The following information is provided as recommendations that are based on the experience of Lattice Semiconductor engineers and customers. If you choose to deviate from these recommendations for a particular application, Lattice Semiconductor strongly suggests that you contact one of its technical representatives for an evaluation of the change.

### 9.1. Power Control

The low-power standby state feature of the SiI9233A receiver provides a design option of leaving the chip always powered, as opposed to powering it on and off. Leaving the chip powered and using the PD# register bit to put it in a lower power state can result in faster system response time, depending on the system Vcc supply ramp-up delay.

### 9.2. Power-on Sequencing

Due to timing considerations with the power-on reset circuits within the chip, Lattice Semiconductor recommends that 5 V power be available to the device before the 3.3 V and 1.2 V VCC supplies are enabled. If the 3.3 V and 1.2 V supplies reach their operating levels before the 5 V power supply to the power island, the chip may not reset properly.

### 9.3. Power Pin Current Demands

The limits shown in Table 9.1 indicate the current demanded by each group of power pins on the SiI9233A device. These limits were characterized at maximum VCC, 0 °C ambient temperature and for fast-fast silicon. Actual application current demands can be lower than these figures, and varies with video resolution and audio clock frequency.

**Table 9.1. Maximum Power Domain Current versus Video Mode**

Mode	ODCK (MHz)	3.3 V Power Domain Currents (mA)		
		IOVCC33	AVCC33	XTALVCC33
480p	27.0	52	62	2
1080i	74.25	116	62	2
1080p	148.5	226	62	2
1080p@12-bit <sup>1</sup>	225	314	62	2

Mode	ODCK (MHz)	1.2 V Power Domain Currents (mA)		
		AVCC12	CVCC12	APVCC12
480p	27.0	93	53	3
1080i	74.25	91	92	3
1080p	148.5	126	167	3
1080p@12-bit <sup>1</sup>	225	107	210	3

**Notes:**

1. Measured with 12-bits/pixel video data.
2. Measured with 192 kHz, 8-channel audio, except for 480p mode which used 48 kHz, 8-channel audio.
3. Measured with RGB input, vertical black-white/1-pixel stripe (Moire2) pattern, converting to YCbCr output (digital for IOVCC33).
4. Only one core can be selected at a time. The TMDsxSEL register bit turns off the unselected core, except for the termination to AVCC33.

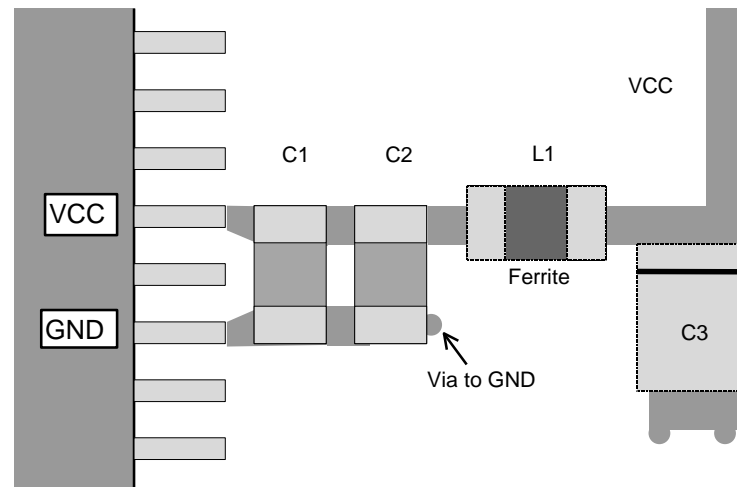
AVCC33 current includes 40 mA for the unselected TMDS core. Only 5 mA of this current is dissipated as power in the receiver; the remainder is dissipated in the HDMI transmitter. The AVCC33 current on the unselected core can be reduced to 5 mA by asserting the corresponding PD\_TERMx# register bit.

## 9.4. HDMI Receiver DDC Bus Protection

The VESA DDC Specification (see the [References](#) section on page 72) defines the DDC I<sup>2</sup>C interconnect bus to be a 5 V signaling path. The I<sup>2</sup>C pins on the SiI9233A chip are 5 V tolerant. And these pins are true open-drain I/O. The pull-up resistors on the DDC bus should be pulled up using the 5 V supply from the HDMI connector. Refer to [Figure 9.9](#) on page 68.

## 9.5. Decoupling Capacitors

Designers should include decoupling and bypass capacitors at each power pin in the layout. These are shown schematically in [Figure 9.4](#) on page 64. Place these components as closely as possible to the SiI9233A pins and avoid routing through vias. [Figure 9.1](#) shows the various types of power pins on the receiver.



**Figure 9.1. Decoupling and Bypass Capacitor Placement**

## 9.6. ESD Protection

The SiI9233A chip is designed to withstand electrostatic discharge to 2 kV. In applications where higher protection levels are required, ESD limiting components can be placed on the differential lines coming into the chip. These components typically have a capacitive effect, reducing the signal quality at higher clock frequencies on the link. Use of the lowest capacitance devices is suggested; in no case should the capacitance value exceed 5 pF.

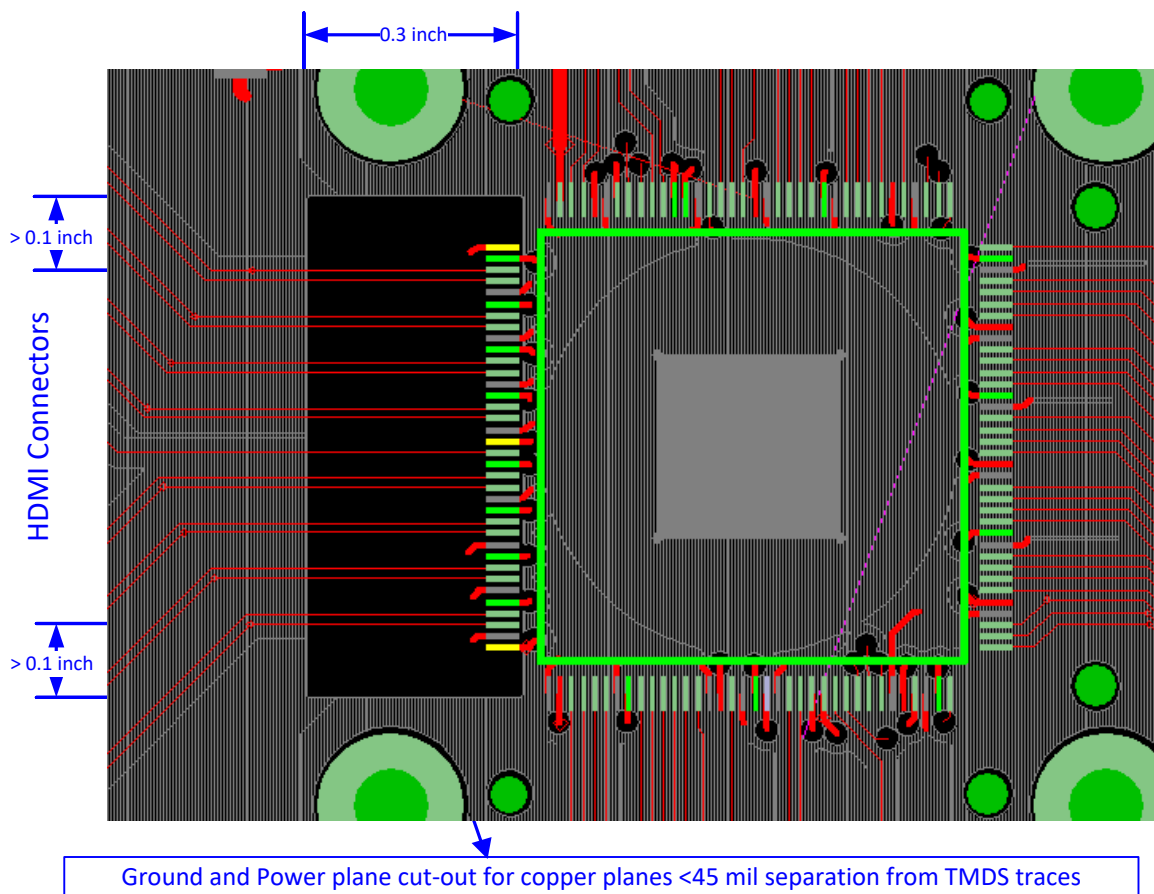
Series resistors can be included on the TMDS lines (see [Figure 9.9](#) on page 68) to counteract the impedance effects of ESD protection diodes. The diodes typically lower the impedance because of their capacitance. The resistors raise the impedance to stay within the HDMI specification centered on a 100-Ω differential.

## 9.7. HDMI Receiver Layout

The SiI9233A chip should be placed as closely as possible to the input connectors that carry the TMDS signals. For a system using industry-standard HDMI connectors (see [Table 10.1](#) on page 71), the differential lines should be routed as directly as possible from connector to receiver. Lattice Semiconductor receivers are tolerant of skews between differential pairs, so spiral skew compensation for path length differences is not required. Each differential pair should be routed together, minimizing the number of vias through which the signal lines are routed. The distance separating the two traces of the differential pair should be kept to a minimum.

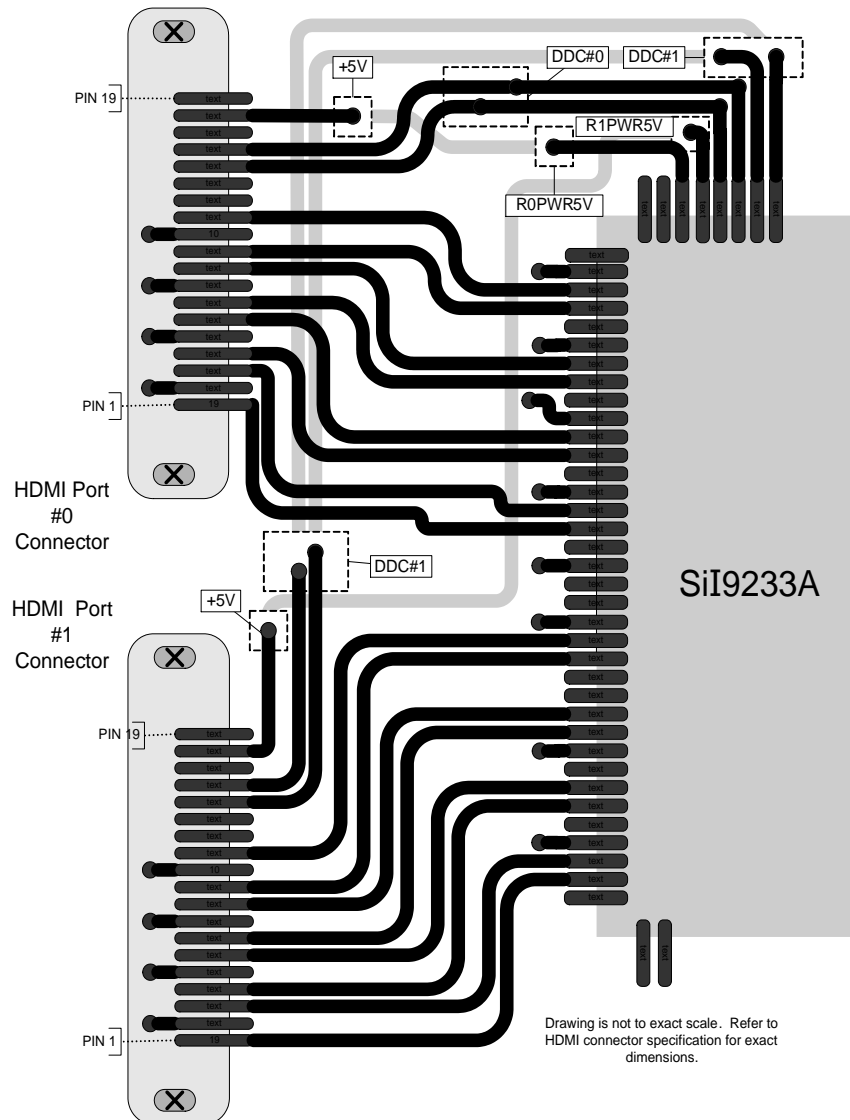
Follow these layout guidelines to achieve the optimal input TMDS signal quality:

1. Lay out all differential pairs with controlled impedance of 100  $\Omega$  differential.
2. Cut out all copper planes (ground and power) that are less than 45 mils underneath the TMDS traces near the receiver with dimensions as shown in [Figure 9.2](#).
3. If ESD suppression devices or common mode chokes are used, place them near the HDMI connector, away from the SiI9233A IC. Do not place them over the ground and power plane cutout near the receiver.



**Figure 9.2. Cut-out Reference Plane Dimensions**

In [Figure 9.3](#) on the next page, which is a representation of a PCB containing HDMI connectors and the receiver, note the sixteen TMDS traces connected directly from the HDMI connectors (left) to the SiI9233A pins (right). Trace impedance should be 100  $\Omega$  differential in each pair and 50  $\Omega$  single-ended if possible. Trace width and pitch depends on the PCB construction. Not all connections are shown; the drawing demonstrates routing of TMDS lines without crossovers, vias, or ESD protection. Refer also to [Figure 9.9](#) on page 68.



**Figure 9.3. HDMI to Receiver Routing – Top View**

## 9.8. EMI Considerations

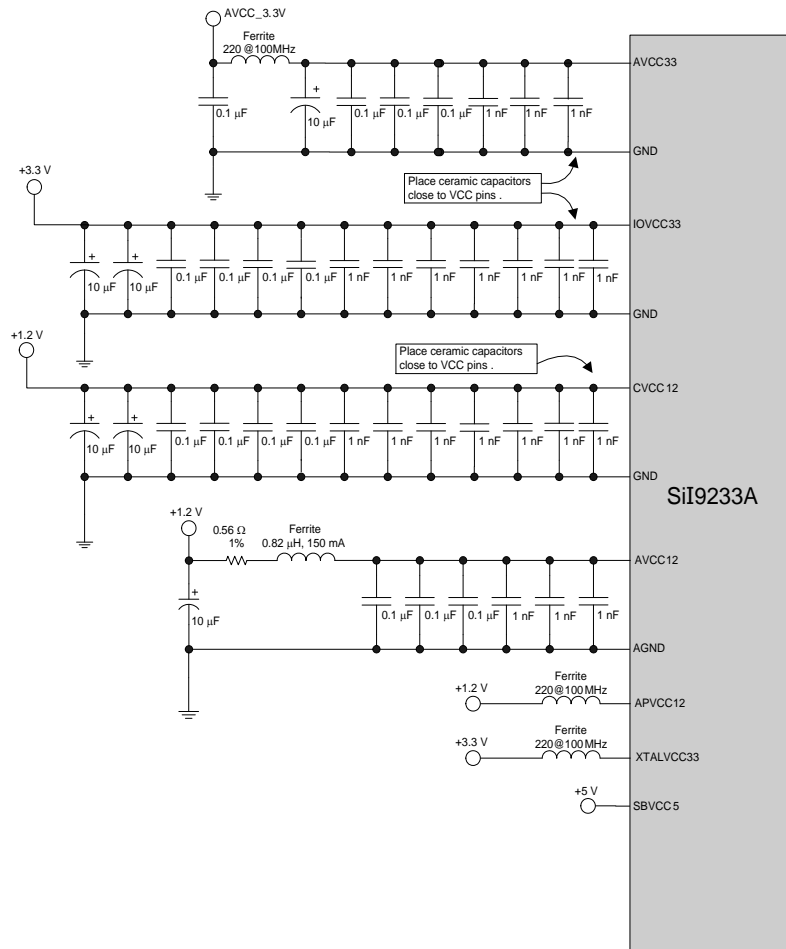
Electromagnetic interference is a function of board layout, shielding, receiver component operating voltage, and frequency of operation, among other factors. When attempting to control emissions, do not place any passive components on the differential signal lines (aside from any essential ESD protection as described earlier). The differential signaling used in HDMI is inherently low in EMI as long as the routing recommendations noted in the Receiver Layout section are followed.

The PCB ground plane should extend unbroken under as much of the SiI9233A chip and associated circuitry as possible, with all ground pins of the chip using a common ground.

## 9.9. Typical Circuit

Representative circuits for application of the SiI9233A chip are shown in [Figure 9.4](#) through [Figure 9.8](#) on pages 64 through 67. For a detailed review of your intended circuit implementation, contact your Lattice Semiconductor representative.

### 9.9.1. Power Supply Decoupling

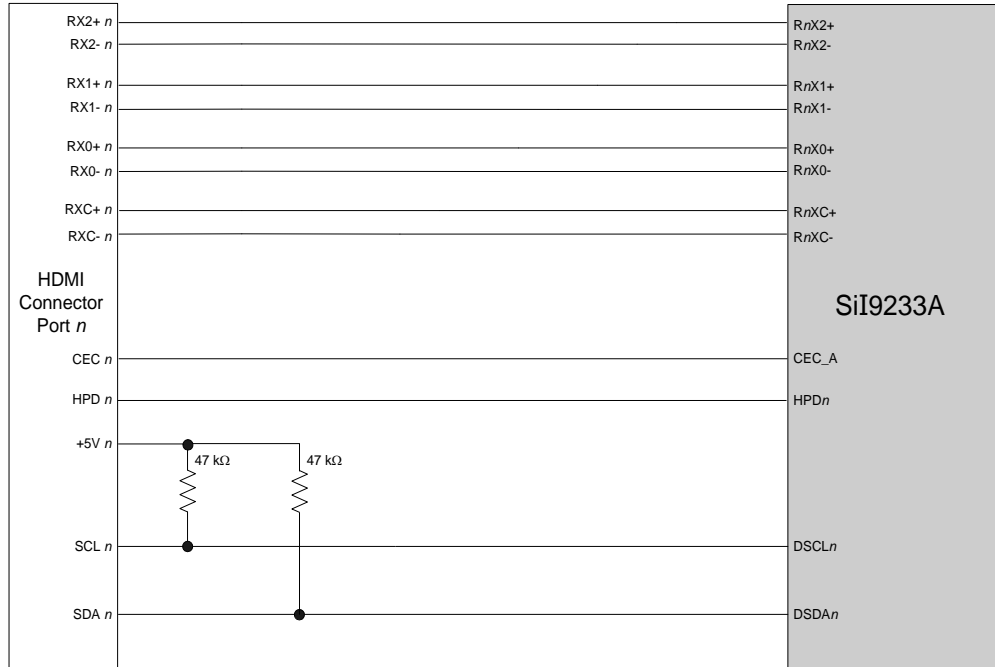


**Figure 9.4. Power Supply Decoupling and PLL Filtering Schematic**

The ferrite on AVCC33 attenuates noise above 10 kHz. A parasitic resistor helps to minimize the peaking. An example of a surface-mount device is the MLF2012 Series SMD inductors from TDK.



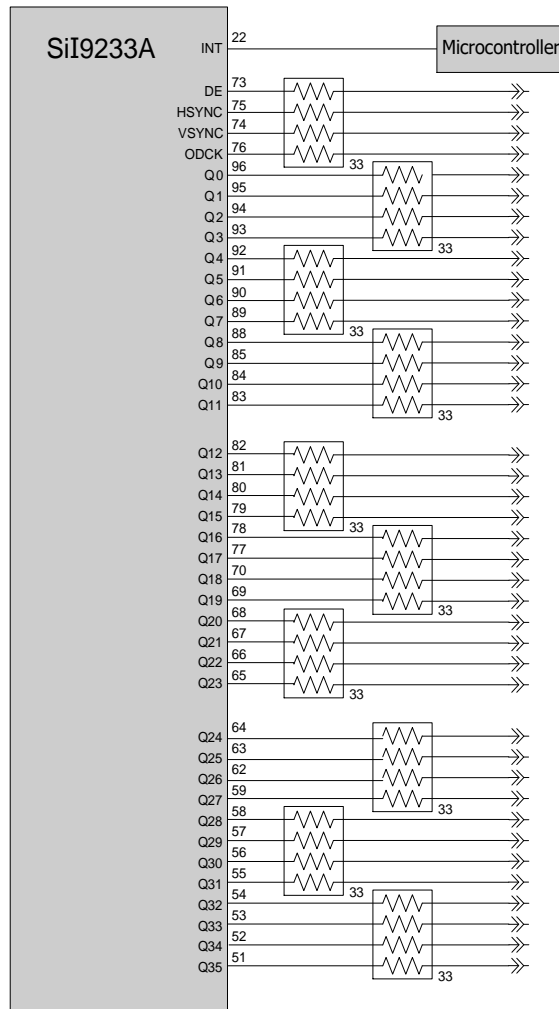
### 9.9.2. HDMI Port Connections



**Figure 9.5. HDMI Port Connections Schematic**

**Note:** Repeat the schematic for each HDMI input port on the SiI9233A receiver.

### 9.9.3. Digital Video Output Connections



**Figure 9.6. Digital Display Schematic**

The 3.3 V to the level-shifters and pull-up resistors should be powered-down whenever the 3.3 V is powered-down on the receiver itself.

The receiver INT output can be connected as an interrupt to the microcontroller, or the microcontroller can poll register 0x70 (INTR\_STATE) to determine if any of the enabled interrupts have occurred. Refer to the Programmer Reference for details. The receiver VSYNC output can be connected to the microcontroller if it is necessary to monitor the vertical refresh rate of the incoming video.

### 9.9.4. Digital Audio Output Connections

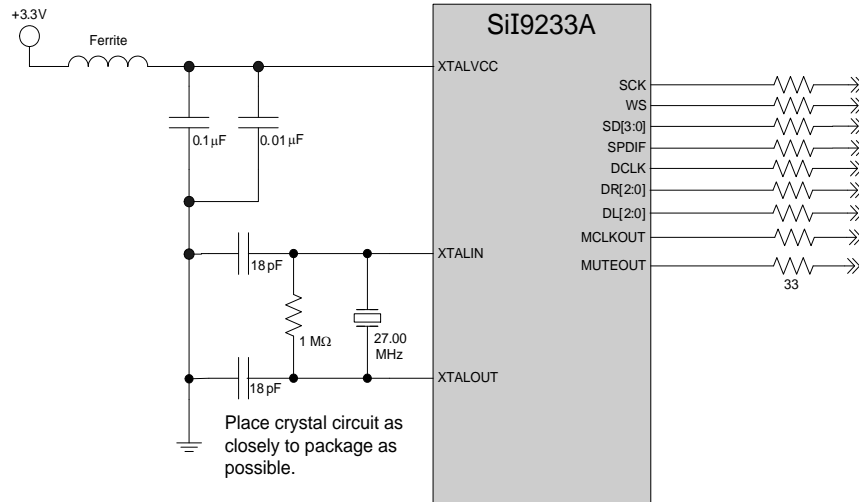


Figure 9.7. Audio Output Schematic

### 9.9.5. Control Signal Connections

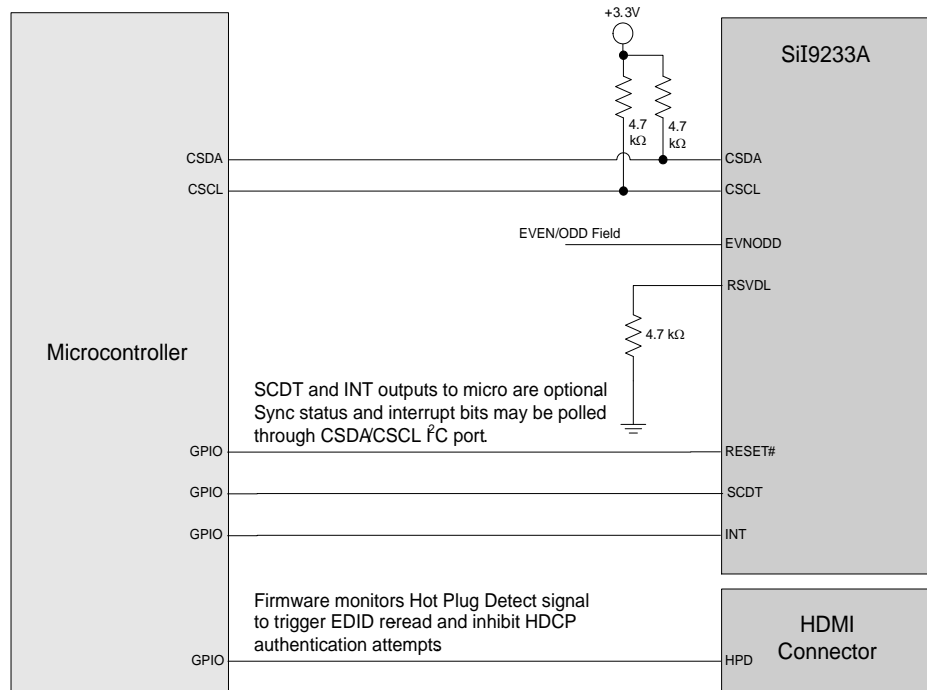


Figure 9.8. Controller Connections Schematic

### 9.10. Layout—TMDS Input Port Connections

Figure 9.9 shows an example of routing TMDS lines between the SiI9233A device and the HDMI connector.

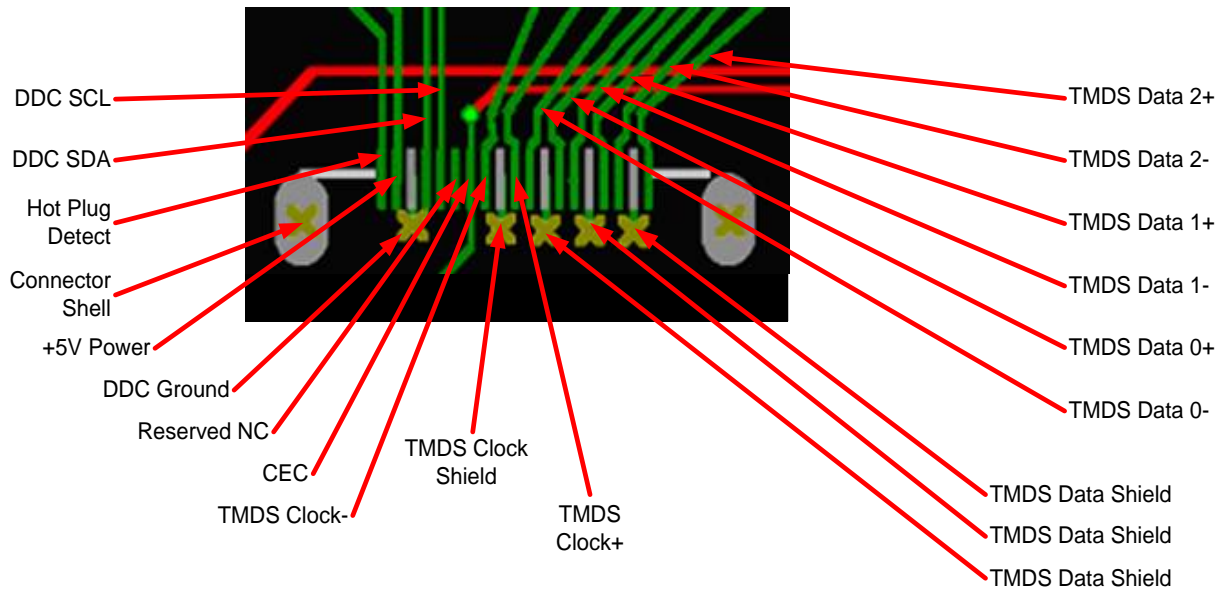


Figure 9.9. TMDS Input Signal Assignments

## 10. Package Information

### 10.1. ePad Requirements

The SiI9233A receiver is packaged in a 144-pin, 20 mm × 20 mm TQFP package with an exposed pad (ePad) that is used for the electrical ground of the device and for improved thermal transfer characteristics. The ePad dimensions are 4.445 mm × 4.0604 mm ±0.15 mm. Soldering the ePad to the ground plane of the PCB is **required** to meet package power dissipation requirements at full speed operation, and to correctly connect the chip circuitry to electrical ground. A clearance of at least 0.25 mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid the possibility of electrical shorts.

The thermal land area on the PCB may use thermal vias to improve heat removal from the package. These thermal vias also double as the ground connections of the chip and must attach internally in the PCB to the ground plane. An array of vias should be designed into the PCB beneath the package. For optimum thermal performance, the via diameter should be 12 mils to 13 mils (0.30 mm to 0.33 mm) and the via barrel should be plated with 1-ounce copper to plug the via. This design helps to avoid any solder wicking inside the via during the soldering process, which may result in voids in solder between the pad and the thermal land. If the copper plating does not plug the vias, the thermal vias can be tented with solder mask on the top surface of the PCB to avoid solder wicking inside the via during assembly. The solder mask diameter should be at least 4 mils (0.1 mm) larger than the via diameter.

Package stand-off when mounting the device also needs to be considered. For a nominal stand-off of approximately 0.1 mm the stencil thickness of 5 mils to 8 mils should provide a good solder joint between the ePad and the thermal land.

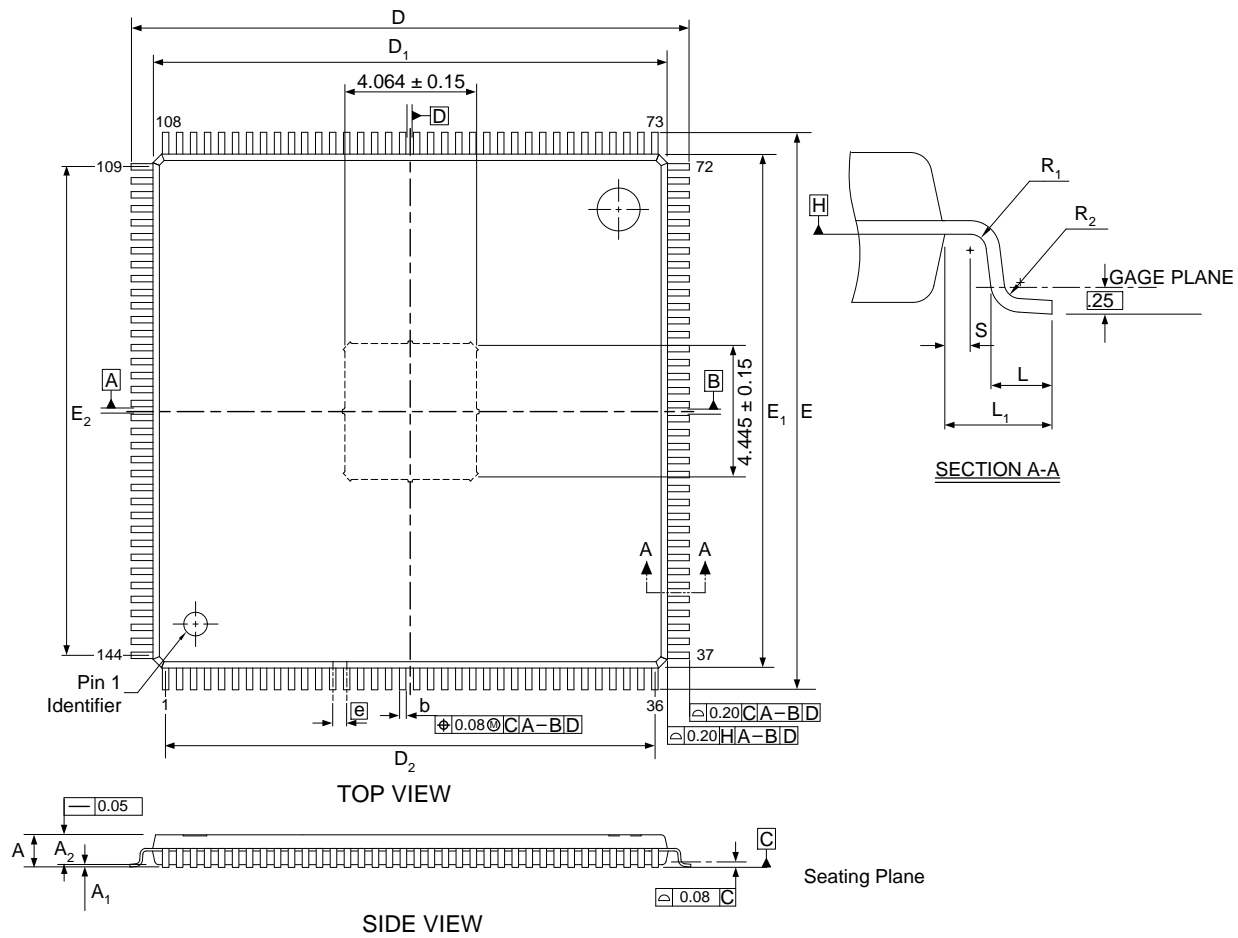
[Figure 10.1](#) on the next page shows the package dimensions of the SiI9233A receiver device.

### 10.2. PCB Layout Guidelines

Refer to Lattice Semiconductor document *PCB Layout Guidelines: Designing with Exposed Pads* (see the [References](#) section on page 72) for basic PCB design guidelines when designing with thermally enhanced packages using the exposed pad. This application note is intended for use by PCB layout designers.

### 10.3. Package Dimensions

These drawings are not to scale.



JEDEC Package Code MS-026-AFB

Item	Description	Min	Typ	Max
A	Thickness	1.00	1.10	1.20
A1	Stand-off	0.05	0.10	0.15
A2	Body thickness	0.95	1.00	1.05
D	Footprint	22.00 BSC		
E	Footprint	22.00 BSC		
D1	Body size	20.00 BSC		
E1	Body size	20.00 BSC		
D2	Lead Row Width	17.5 BSC		
E2	Lead Row Width	17.5 BSC		

Item	Description	Min	Typ	Max
b	Lead width	0.17	0.22	0.27
C	Lead thickness	0.09	—	0.20
e	Lead pitch	0.50 BSC		
L	Lead foot length	0.45	0.60	0.75
L1	Total lead length	1.00 REF		
R1	Lead radius, inside	0.08	—	—
R2	Lead radius, outside	0.08	—	0.20
S	Lead horizontal run	0.20	—	—

Dimensions in millimeters.

Overall thickness A = A1 + A2.

Figure 10.1. 144-Pin TQFP Package Diagram

## 10.4. Marking Diagram

Figure 10.2 shows the markings of the SiI9233A package. Figure 10.1 on the previous page shows the package and dimension details.

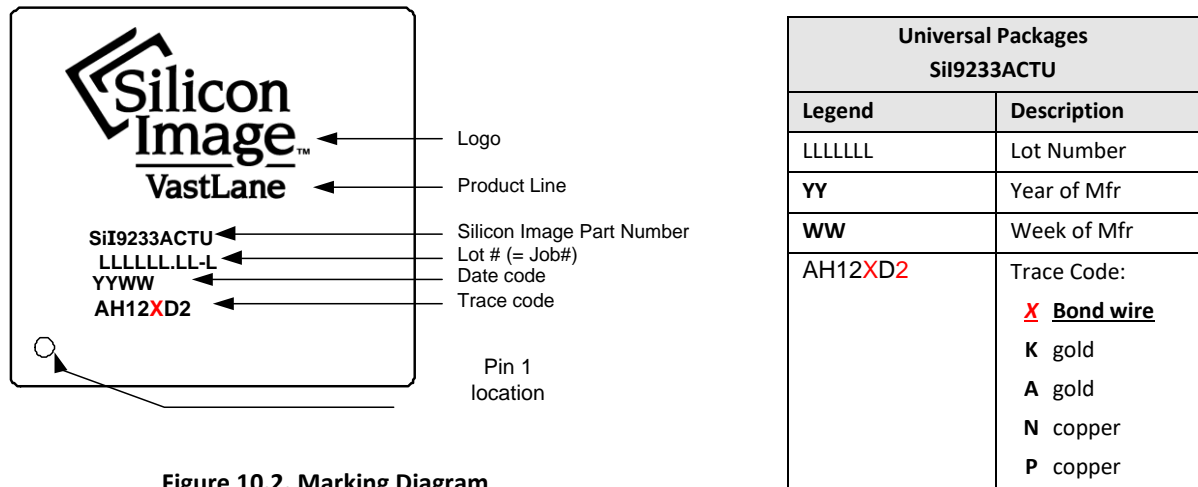


Figure 10.2. Marking Diagram

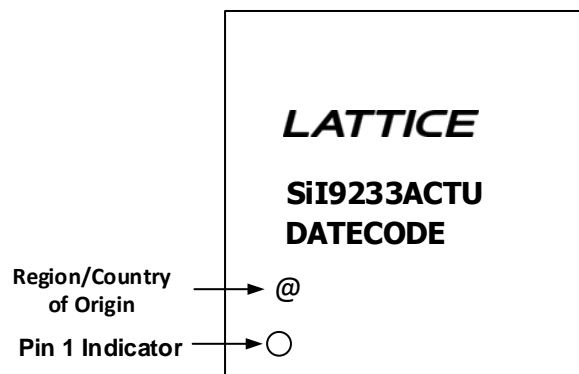


Figure 10.3. Alternate Marking Diagram

## 10.5. Ordering Information

Table 10.1 gives ordering information for the SiI9233A HDMI receiver device.

Table 10.1. SiI9233A HDMI Receiver Device Ordering Information

Part Number	Pixel Clock Range	Interface	Bond Wire	Resolution/Refresh Rate	Package	Temperature Grade
SiI9233ACTU	25 MHz – 225 MHz	HDMI	Gold	1080p/60 Hz	144-pin TQFP ePad	Extended (–30 °C to +85 °C)
SiI9233ACTU-C	25 MHz – 225 MHz	HDMI	Copper	1080p/60 Hz	144-pin TQFP ePad	Extended (–30 °C to +85 °C)

The universal package may be used in lead-free and ordinary process lines.

## References

### Standards Documents

This is a list of the standards abbreviations appearing in this document.

Abbreviation	Standards publication, organization, and date
HDMI	<i>High Definition Multimedia Interface</i> , Revision 1.3, HDMI Consortium; June 2006
HCTS	<i>HDMI Compliance Test Specification</i> , Revision 1.3c, HDMI Consortium; July 2008.
HDCP	<i>High-bandwidth Digital Content Protection</i> , Revision 1.3, Digital-Content Protection, LLC; December 2006.
E-EDID	<i>Enhanced Extended Display Identification Data Standard</i> , Release A Revision 1, VESA; Feb. 2000.
E-DID IG	<i>VESA EDID Implementation Guide</i> , VESA; June 2001.
CEA-861	<i>A DTV Profile for Uncompressed High Speed Digital Interfaces</i> , EIA/CEA; January 2001.
CEA-861-B	<i>A DTV Profile for Uncompressed High Speed Digital Interfaces</i> , Draft 020328, EIA/CEA; March 2002.
CEA-861-D	<i>A DTV Profile for Uncompressed High Speed Digital Interfaces</i> , EIA/CEA; July 2006.
EDDC	<i>Enhanced Display Data Channel Standard</i> , Version 1.1, VESA; March 2004.

For information on the specifications that apply to this document, contact the responsible standards groups appearing on this list.

Standards Group	Web URL
ANSI/EIA/CEA	<a href="http://global.ihs.com">http://global.ihs.com</a>
VESA	<a href="http://www.vesa.org">http://www.vesa.org</a>
DVI	<a href="http://www.ddwg.org">http://www.ddwg.org</a>
HDCP	<a href="http://www.digital-cp.com">http://www.digital-cp.com</a>
HDMI	<a href="http://www.hdmi.org">http://www.hdmi.org</a>

### Lattice Semiconductor Documents

This is a list of the related documents that are available from your Lattice Semiconductor sales representative. *The Programmer's Reference requires an NDA with Lattice Semiconductor.*

Document	Title
SiI-PR-1033	<i>SiI9223A/9233A/9127A HDMI Receivers Programmer Reference</i>
SiI-PR-0041	<i>CEC Programming Interface (CPI) Programmer Reference</i>
SiI-AN-0129	<i>PCB Layout Guidelines: Designing with Exposed Pads</i>

### Technical Support

For assistance, submit a technical support case at [www.latticesemi.com/techsupport](http://www.latticesemi.com/techsupport).



## Revision History

### Revision D, May 2017

Figure 10.3. Alternate Marking Diagram added per PCN13A16.

### Revision C, March 2016

Formatted to latest template.

### Revision C, November 2013

1. Updated Figure 10.2. Marking Diagram to show trace code information.
2. Added Table 10.1. SiI9233A HDMI Receiver Device Ordering Information.
3. Updated layout by repositioning the Revision History section.

### Revision B, December 2012

Added local I<sup>2</sup>C device addresses.

### Revision A07, August 2010

Removed Patent information from DB, rolled the revision.

### Revision A06, April 2010

Update to create Data Brief.

### Revision A05, September 2009

Minor corrections; updated with 3D information.

### Revision A04, June 2009

Update T<sub>CK2OUT</sub> and related values; update additional content.

### Revision A03, February 2009

Removed audio downsampling, output delay control, and video output pull-down information.

### Revision A02, January 2009

Clarify POR requirement; provided RnPW5V power requirement; minor corrections.

### Revision A01, October 2008

Removed references to Mobile HD.

### Revision A, October 2008

Initial production release.



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