Sil9396 superMHL/MHL to HDMI Bridge and superMHL Transmitter with HDCP 2.2 Support

Data Sheet

SiI-DS-1170-B

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Glossary

A glossary of terms used in this document.

Acronym	Definition
CBUS	MHL Link Control Bus
CBUS1	First Generation CBUS
DDC	Display Data Channel
DSC	Display Stream Compression
eCBUS	Enhanced CBUS
eCBUS-S	One-wire, single-ended eCBUS
EDID	Extended Display Identification Data
eMSC	High-throughput CBUS
ESD	Electrostatic Discharge
HDCP	High-bandwidth Digital Content Protection
HDMI	High-Definition Multimedia Interface
HPD	Hot Plug Detect
I²C	Inter-Integrated Circuit
MCU	Microcontroller Unit
MHL	Mobile High-Definition Link
MISO	Master In Slave Out
MOSI	Master Out Slave In
OTP	One Time Programmable
PCM	Pulse Code Modulation
S/PDIF	Sony/Philips Digital Interface Format
SCDC	Status and Control Data Channel
SPI	Serial Peripheral Interface
STB	Set Top Box
TDM	Time-Division Multiplexing
TMDS	Transition Minimized Differential Signaling

1. General Description

The SiI9396 device is a superMHL™ 1.0/MHL® to HDMI 2.0 bridge with HDCP 2.2 repeater support targeted for superMHL and MHL dongle from Lattice Semiconductor. The SiI9396 device is also a superMHL 1.0/HDMI 2.0 transmitter targeted for superMHL source and Set Top Box (STB).

The SiI9396 receiver port can be configured into a superMHL compliant port, an MHL 3 compliant port, or an HDMI 2.0 compliant port.

The SiI9396 device can receive and decompress VESA Display Stream Compression (DSC) 1.1 video signals up to 4K x 2K @ 60 Hz.

As a bridge, the SiI9396 device supports superMHL and MHL input up to 4K x 2K @ 30 Hz with YCbCr 4:2:2.

As a superMHL transmitter, the SiI9396 device supports one output with three-lane superMHL. It also supports audio insertion through S/PDIF or 2-channel I^2S input with downsampling.

As an HDMI transmitter, the SiI9396 device supports one output with HDMI 2.0 up to 18 Gb/s. The SiI9396 device can convert certain types of reduced blank formats such as a 337 MHz Transition Minimized Differential Signaling (TMDS™) input of 10-bit 4K @ 50/60 Hz 4:2:0 into an HDMI 2.0 standard 4K @ 50/60 Hz 4:2:2 10-bit output.

1.1. superMHL Input

- Configurable for one or three data lanes operating at 6 Gb/s per lane
- Three-lane superMHL input supports video resolution up to 4K x 2K @ 60 Hz with YCbCr 4:4:4/RGB
- One-lane superMHL input supports video resolution up to 4K x 2K @ 30 Hz with YCbCr 4:2:2
- One-lane superMHL input via DSC decompression can support up to 4K x 2K @ 60Hz with YCbCr 4:4:4/RGB

1.2. MHL Input

- Supports 6 Gb/s MHL 3 compatible input, backward compatible with MHL 1 and MHL 2

1.3. HDMI Input

- Supports 18 Gb/s HDMI 2.0 compatible input, backward compatible with HDMI 1.4

1.4. superMHL Output

- Supports three-lane superMHL output resolution up to 4K x 2K @ 60 Hz with superMHL connector
- Supports superMHL connector with reversible cable

1.5. HDMI Output

- Supports 18 Gb/s HDMI 2.0 compatible output, backward compatible with HDMI 1.4

1.6. Video Format Conversion

- BT.601/BT.709 color space conversion
- supports xvYCC colorimetry
- Supports 8-bit YCbCr 4:2:2 to YCbCr 4:4:4 chroma upsampling, 8-bit YCbCr 4:4:4 to YCbCr 4:2:2 chroma downsampling
- Supports 8/10-bit YCbCr 4:2:0 to YCbCr 4:2:2, and 8/10-bit YCbCr 4:2:2 to YCbCr 4:2:0 conversion
- Supports pixel reorder with 4K x 2K @ 30 Hz

1.7. DSC Decoder

- Supports 8-bit DSC decoder with YCbCr 4:4:4/RGB
- Supports 8/10-bit DSC decoder with YCbCr 4:2:0

1.8. Audio

- Supports audio insertion through one I^2S input up to two channels or S/PDIF input
- Supports audio extraction up to eight channels through four I^2S outputs or S/PDIF output
- Supports up to 192 kHz PCM and compressed audio formats
- Supports high bitrate (HBR) audio output up to 768 KHz

1.9. HDCP

- Built in HDCP 2.2/HDCP 1.4 decryption engine
- Built in HDCP 2.2/HDCP 1.4 encryption engine
- Supports HDCP 2.2 and HDCP 1.4 repeater

1.10.Host Interface

- Inter-Integrated Circuit (I^2C)
- Serial Peripheral Interface (SPI)

1.11. Microprocessor

- Built-in enhanced microprocessor

1.12.Packaging

- 76-pin QFN (9 mm × 9mm) package
- Standard part covers extended (–20 °C to + 85 °C) temperature range

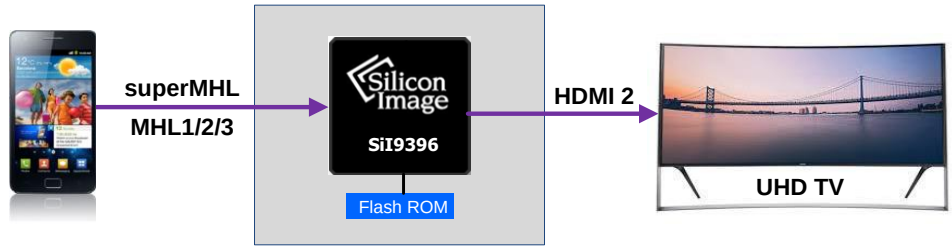


Figure 1.1. Typical Application for the SiI9396 Bridge

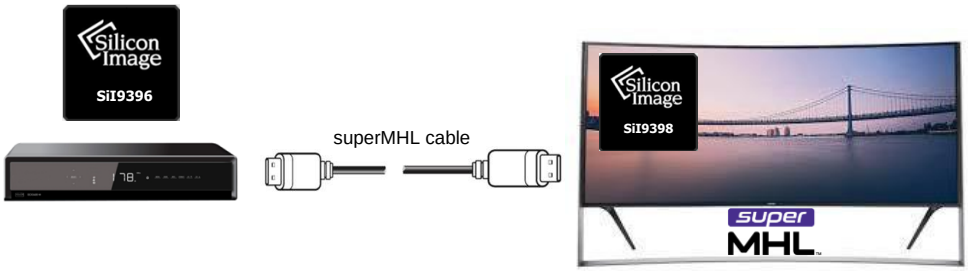


Figure 1.2. Typical Application for the SiI9396 superMHL Transmitter

2. Functional Description

Figure 2.1 shows the functional block diagram of the SiI9396 device.

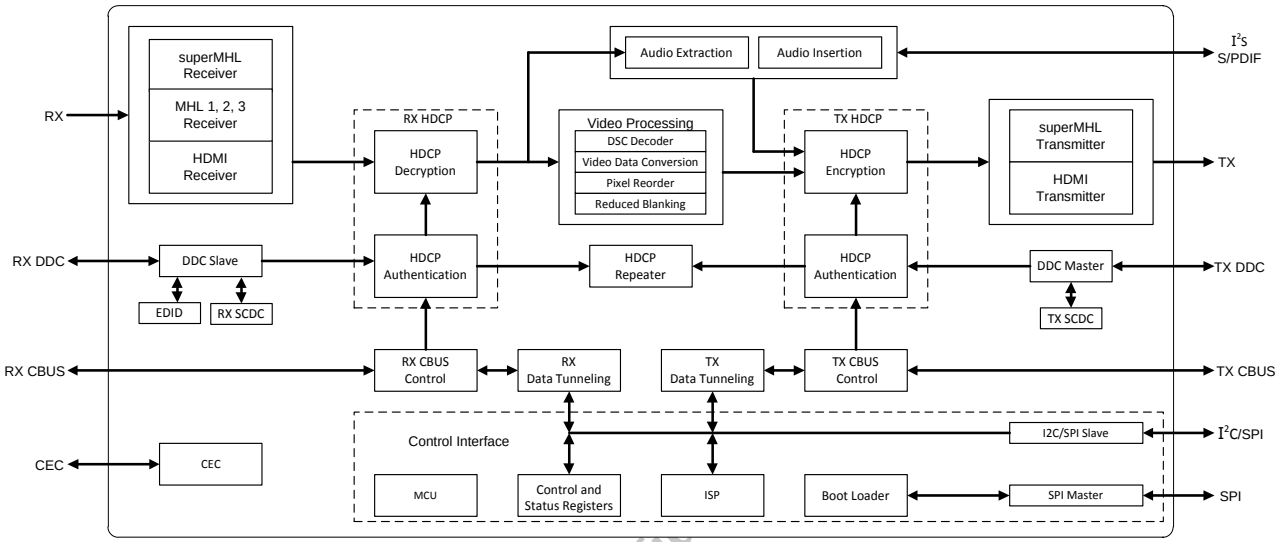


Figure 2.1. Functional Block Diagram

2.1. superMHL Receiver

The superMHL receiver is configurable for one or three data lanes operating at 6 Gb/s per lane. Three-lane superMHL input supports video resolution up to 4K x 2K @ 60 Hz with YCbCr 4:4:4/RGB. One-lane superMHL input supports video resolution up to 4K x 2K @ 30 Hz with YCbCr 4:2:2. With DSC decoder, one-lane superMHL receiver can receive and decompress VESA DSC video up to 4K x 2K @ 60 Hz with YCbCr 4:4:4/RGB. One-lane superMHL receiver supports a Type A connector (Class A).

The superMHL receiver supports Forward Error Correction (FEC). This port supports HDCP 2.2 and HDCP 1.4 decryption.

See the Video Format Support section on page 38 and the 3D Format Support section on page 43 for more information.

2.2. MHL 1, 2, 3 Receiver

The MHL 1, 2, 3 receiver block consists of MHL 1, MHL 2, and MHL 3 interfaces. The working mode of the SiI9396 device depends on the type of source device connected to the input interface. In addition, the status of the discovery pulses on the CBUS is to be considered. Refer to the corresponding section of the MHL Specification for details.

The MHL 1, 2, 3 receiver block receives the TMDS signals and recovers the video, audio, and auxiliary data according to the working mode. With DSC decoder, MHL 3 receiver can receive and decompress VESA DSC video up to 4K x 2K @ 60 Hz with YCbCr 4:4:4/RGB.

See the Video Format Support section on page 38 and the 3D Format Support section on page 43 for more information.

2.3. RX CBUS Control Block

The RX CBUS control block handles the superMHL or MHL control bus interface. The working mode of the CBUS control block is configured based on the input source type. The CBUS control block follows a specific communication and arbitration protocol to exchange EDID, Control, and HDCP information. In superMHL or MHL 3 eCBUS-S mode, the CBUS control block implements the mechanism of Time-Division Multiplexing (TDM) to encode and decode the legacy CBUS commands and eMSC data over the CBUS signal.

2.4. HDMI Receiver

The SiI9396 HDMI receiver features a TMDS core having the capability of receiving data up to 6 Gb/s per channel. The total data bandwidth is 18 Gb/s. This allows the HDMI receiver to input UltraHD 4:4:4 format at 50 or 60 Hz. The HDMI receiver supports HDMI 1.4 and HDMI 2.0 specifications. It also supports HDMI input with HDCP 2.2 or HDCP 1.4 decryption.

See the Video Format Support section on page 38 and the 3D Format Support section on page 43 for more information.

2.5. Receiver DDC Interface

The receiver Display Data Channel (DDC) interface is used as a DDC slave for the HDMI source to read the capabilities programmed in the internal EDID SRAM of the SiI9396 device and exchange the HDCP information. The DDC channel is also used to perform SCDC related transactions by source according to the HDMI 2.0 Specification.

2.6. Data Tunneling Block

The Data Tunneling block implements the mechanism of TDM to transfer the eMSC data and legacy CBUS commands over the CBUS signal between two superMHL or MHL 3 devices. The Data Tunneling blocks include RX data tunneling and TX data tunneling. The total data bandwidth is 75 Mb/s.

The eMSC data on both sides of the receiver and transmitter of the SiI9396 devices can be handled by host processor through the I^2C or SPI interface.

Table 2.1. Typical Bandwidth for eMSC Data Tunneling Block

Data Transfer Channel	Interfaces Used	eCBUS-S	Notes
eMSC	I^2C, SPI	9 Mb/s	1, 2
CBUS1	CBUS	3 Mb/s	—
Reserved	—	63 Mb/s	—
Total	—	75 Mb/s	—

Notes:
1. TDM slot allocation can be adjusted on the eCBUS.
2. Bandwidth may also be limited by the speed used for the I2C or SPI interface.

2.7. superMHL Transmitter

The superMHL transmitter supports three-lane superMHL output with the superMHL Class B connector. This port supports HDCP 2.2 and HDCP 1.4 encryption. The SiI9396 superMHL transmitter features a TMDS core having the capability of receiving data up to 6 Gb/s per channel. The total data bandwidth is 18 Gb/s. This allows receiver to input UltraHD 4:4:4 format at 50 or 60 Hz.

See the Video Format Support section on page 38 for more information.

2.8. TX CBUS Control Block

The TX CBUS Control block handles the superMHL output control bus interface. The CBUS Control block follows a specific communication and arbitration protocol to exchange EDID, Control, and HDCP information. In superMHL eCBUS-S mode, the CBUS Control block implements the mechanism of TDM to encode and decode the legacy CBUS commands and eMSC data over the CBUS signal.

2.9. HDMI Transmitter

The SiI9396 device supports one HDMI transmitter port. The HDMI transmitter features a TMDS core having the capability of transmitting data up to 6 Gb/s per channel. The total data bandwidth is 18 Gb/s. This allows transmitter port to output UltraHD 4:4:4 format at 50 or 60 Hz in HDMI 2.0 mode. A built-in source termination is integrated to minimize reflection and ensure the highest quality of the transmitted signal. This port can support HDCP 2.2 and HDCP 1.4 encryption.

See the Video Format Support section on page 38 for more information.

2.10. Transmitter DDC Interface

The Transmitter DDC Interface is a DDC Master for the HDMI downstream device connection. The DDC master port is used to connect the HDMI cable directly. This feature simplifies the system design and helps to lower its cost. The DDC master is also used to perform Status and Control Data Channel (SCDC) related transactions by source according to the HDMI 2.0 Specification.

2.11. Video Processing

2.11.1. DSC Decoder

The VESA DSC Standard is a specific algorithms used for compressing and decompressing image display streams. The DSC algorithm is designed to enable low-cost hardware implementations of visual lossless video compression over display links. The DSC decoding process includes Substream Demultiplexing, Entropy Decoding, Rate, Line Storage, Prediction and Reconstruction, and Indexed Color History.

The SiI9396 device integrated the 8/10-bit DSC decoder. The input to the block can be 8/10-bit YCbCr 4:2:0 or 8-bit YCbCr 4:4:4/RGB DSC stream. The compression ratio can be 2:1, 2.5:1 or 3:1. The DSC decoder output supports resolution up to 4K x 2K @ 60 Hz 10-bit YCbCr 4:2:0 or 8-bit YCbCr 4:4:4/RGB.

See the DSC Decompression Support section on page 35 for more information.

2.11.2. Video Data Conversion Block

The SiI9396 receiver includes a Video Data Conversion Logic block. Figure 2.2 shows the processing stages for the video data. Each of the processing blocks can be bypassed.

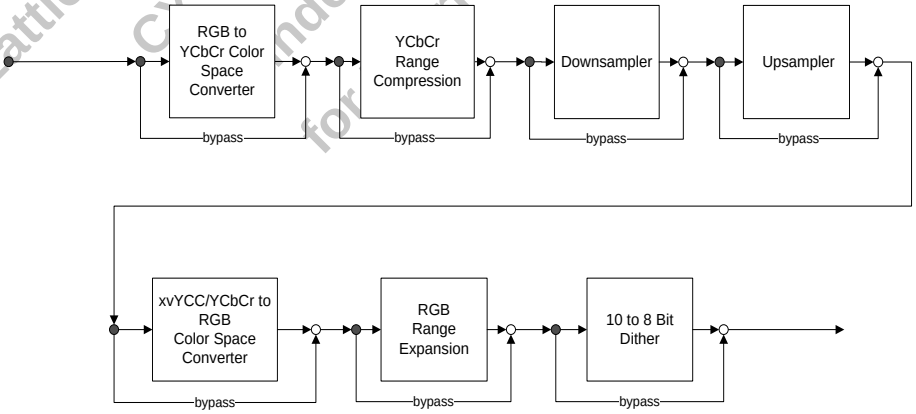


Figure 2.2. Default Video Processing Path

2.11.2.1. Color Space Converter

The Color Space Converter (CSC) converts RGB data to the Standard-Definition (ITU.601), High-Definition (ITU.709) YCbCr formats, and vice-versa. To support the latest extended-gamut xvYCC displays, the SiI9396 device implements CSC blocks to convert RGB data to the extended-gamut Standard-Definition (ITU.601) or High-Definition (ITU.709) xvYCC formats, and vice-versa. The CSC can be adjusted to perform Standard-Definition conversions (ITU.601) or High-Definition conversions (ITU.709) by setting the appropriate registers.

See the RGB to YCbCr Color Space Converter and YCbCr to RGB Color Space Converter sections on page 35 for more information.

2.11.2.2. xvYCC Support

The SiI9396 device adds support to the extended gamut xvYCC color space only in the HDMI mode. This extended format has roughly 1.8 times more colors than the RGB color space. The use of the xvYCC color space is possible because of the availability of LED and laser-based light sources for the next generation displays. This format also makes use of the full range of values in the 8-bit space.

2.11.2.3. YCbCr Range Compression

When enabled by itself, the range compression block compresses 0 – 255 full-range data into 16 – 235 limited-range data for each video channel, and compresses to 16 – 240 for the Cb and Cr channels. The color range scaling is linear.

2.11.2.4. Downsampler

Downsampling reduces the number of chrominance samples in each line by half, converting 4:4:4 sampled video to 4:2:2 video.

2.11.2.5. Upsampler

Chrominance upsampling and downsampling increase or decrease the number of chrominance samples in each line of video. Upsampling doubles the number of chrominance samples in each line, converting 4:2:2 sampled video to 4:4:4 sampled video.

2.11.2.6. RGB Range Expansion

The SiI9396 device can scale the input color from limited-range into full-range using the range expansion block. When enabled by itself, the range expansion block expands 16 – 235 limited-range data into 0 – 255 for each video channel. When the range expansion and the xvYCbCr/YCbCr to RGB color space converter are both enabled, the input conversion range for the Cb and Cr channels is 16 – 240.

2.11.2.7. 10 to 8 Bit Dither

The 10 to 8 Bit Dither block dithers internally processed 10-bit data to 8-bit data for output.

2.11.3. 422 to 420 Conversion

The SiI9396 device supports 8/10-bit YCbCr 4:2:2 to YCbCr 4:2:0 conversion.

2.11.4. 420 to 422 Conversion

The SiI9396 device supports 8/10-bit YCbCr 4:2:0 to YCbCr 4:2:2 conversion.

2.11.5. Pixel Reorder

The SiI9396 device can reorder the pixel of 4K x 2K @ 30 Hz with 8-bit YCbCr 4:2:0 video to reduce bandwidth requirements. For a wirelessHD application, this feature is a must.

2.11.6. Reduced Blanking

The SiI9396 HDMI transmitter can convert some types of reduced blanking formats such as a 337 MHz TMDS input of 4K x 2K @ 50/60 Hz with 10-bit YCbCr 4:2:0 into a standard HDMI 2.0 output. Table 2.2 on the next page describes the detailed timings of the two reduced blanking formats. Other possible reduced blanking formats can also be supported.

Table 2.2. Reduced Blanking Support Timings

Description	4K × 2K @ 60 Hz	4K × 2K @ 50 Hz
Pixel Frequency (MHz)	540	540
Vfreq (Hz)	60	50
Hactive	3840	3840
Hblank	160	960
Hfront	16	16
Hsync	44	44
Hback	100	900
Vactive	2160	2160
Vblank	90	90
Vfront	8	8
Vsync	10	10
Vback	72	72

2.12.Audio Insertion/Extraction

The SiI9396 device supports audio insertion through one I^2S input up to two channels or S/PDIF input. The SiI9396 device also supports audio extraction through four I^2S outputs up to eight channels or S/PDIF output. The SiI9396 device can run either audio insertion or audio extraction, but cannot run both simultaneously. As a superMHL transmitter, the SiI9396 device supports audio insertion. The SiI9396 device supports sampling rates from 32 KHz to 192 KHz. The SiI9396 device also supports High Bitrate (HBR) audio output up to 768 kHz.

Refer to the Audio Input/Output section on page 46 for more information.

2.13.HDCP

The SiI9396 device supports HDCP 2.2 and HDCP 1.4.

2.13.1. Receiver HDCP Authentication Logic Block

The Receiver HDCP Authentication Logic block handles the task of establishing a secure link for receiving protected content from upstream device. This process involves exchanging security information with the source over the CBUS or receiver DDC. The HDCP authentication logic has two parts: one is for HDCP 2.2 authentication, and the other is for HDCP 1.4 authentication. The SiI9396 bridge supports different HDCP modes. Refer to the SiI9396 Bridge Input and Output Matrix with HDCP section on page 46 for more details.

2.13.2. HDCP Decryption Engine Block

The SiI9396 device has two HDCP decryption engines: HDCP 2.2 decryption engine and HDCP 1.4 decryption engine.

The HDCP Decryption Engine block handles the task of decrypt data coming from the superMHL/MHL 1, 2, 3/HDMI receiver blocks. The appropriate decryption key is applied to the HDCP decryption engine block to descramble the video, audio, and auxiliary packets. The decryption mode can be configured by the device. Refer to the SiI9396 Bridge Input and Output Matrix with HDCP section on page 46 for more details.

2.13.3. Transmitter HDCP Authentication Logic

The transmitter HDCP authentication logic block handles the task of establishing a secure link for transmitting protected content to downstream device. It has two parts: one is for HDCP 2.2 authentication, and the other is for HDCP 1.4 authentication. The authentication mode is determined by the device configuration.

Unlike the HDCP 1.4 authentication, the process for HDCP 2.2 involves authentication and key exchange, pairing for downstream device, random number generating, and locality check and session key exchange. The SiI9396 device supports different HDCP modes. Refer to the SiI9396 Bridge Input and Output Matrix with HDCP section on page 46 for details.

2.13.4. HDCP Encryption Engine Block

The HDCP Encryption Engine block contains the necessary logic to encrypt the incoming audio and video data and includes support for HDCP authentication.

The decryption mode is configured by the device. Refer to the SiI9396 Bridge Input and Output Matrix with HDCP section on page 46 for more details.

2.13.5. HDCP Repeater

The SiI9396 bridge supports HDCP 2.2 repeater and HDCP 1.4 repeater.

The HDCP Repeater Block is only used when the device is configured as a repeater, in which MHL receiver and HDMI transmitter connections are cascaded. In this case, each transmitter has to ensure that all downstream receivers are HDCP compliant. To ensure that all receivers in the downstream path are protected by HDCP, the downstream transmitters propagate a ready signal to the final upstream source transmitter.

2.13.6. One Time Programmable (OTP)

The SiI9396 device comes preprogrammed with a set of production HDCP keys stored in an internal ROM. System manufacturers do not need to purchase key sets from the Digital Content Protection LLC. We handle all purchasing, programming, and security for the HDCP keys. The preprogrammed HDCP keys provide the highest level of security because there is no way to read the keys once the devices are programmed. Customers must sign the HDCP license agreement (www.digital-cp.com) or be under a specific NDA with Lattice Semiconductor before receiving samples of the device.

2.14.Control Interface

2.14.1. Internal Microprocessor

The SiI9396 device has an embedded enhanced microprocessor that provides a low-cost system implementation. The internal microprocessor is clocked by internal oscillator. It is used to control the main data flow by register configuration and interrupt handling, as well as handle the initialization at reset, HDCP 1.4/2.2 authentication and encryption and so on.

2.14.2. Boot Loader

This internal microprocessor boots from an external SPI Flash memory through a dedicated SPI master interface. Refer to the SPI Interface Timing section on page 24 for details. The boot sequence is triggered when the standby power is applied to the device.

The SPIM_CLK_BM0, SPIM_DO_BM1, and SPIM_DI_BM2 pins are strapped on hardware reset to select the boot mode, as shown in the following Table 2.3.

Table 2.3. Boot Mode

Pin Name	Value	Mode	Description
BM0	1	Hardware Mode	For internal use only. Do not run the internal microprocessor. The hardware SPI or I²C slave controllers is enabled to allow host processor to access all the registers.
	0	Internal Microprocessor Mode	Attempts to load firmware and run the internal microprocessor if the firmware is loaded successfully.
BM1, BM2	00	I²C Address 0: 0x60	The combination decides the default host control interface for hardware mode and internal microprocessor mode. The I²C Address cannot be adjusted after boot.
	01	I²C Address 1: 0x68	
	10	I²C Address 2: 0x64	
	11	SPI	

Note: 10 kΩ pull-up/down resistors are recommended on the strap pins.

2.14.3. Control and Status Logic Block

Many of the SiI9396 functions are controlled by the Control and Status Registers (CSR).

The Power-On Reset (POR) circuit is also contained in this block. The INT signal interrupts the host processor when certain conditions arise inside the SiI9396 device. The INT output is programmable to be either active HIGH or LOW. The SiI9396 device has six General Purpose I/O (GPIO) pins. Each GPIO pin supports bidirection and can be reconfigured as other functions. Refer to the Control and Configuration Pins section on page 32 for more information.

2.14.4. Local Host Interface

The host controller can communicate with the SiI9396 device either through the local I^2C bus, or through the local SPI slave interface. Refer to the description below for both interfaces.

2.14.4.1. I^2C Slave Controller

The local I^2C Slave Controller provides a communication interface between host processor and SiI9396 device. The controller is capable of running up to 400 kHz. The CSCL and CSDA signals of I^2C are multiplexed with GPIO2 and GPIO3 pins. Refer to Table 2.3 and the Control and Configuration Pins section on page 32 for more information.

The I^2C interface can also be used by the I^2C controller of the internal processor, which can be configured as an I^2C master to control peripherals.

2.14.4.2. SPI Slave Controller

The local SPI Slave Controller provides a faster communication interface between host processor and the SiI9396 device. The CS, SCLK, MISO, and MOSI signals of SPI are multiplexed with GPIO0, GPIO 1, GPIO 2, and GPIO3 pins. Refer to Table 2.3 and the Control and Configuration Pins section on page 32 for more information.

2.14.5. In-System Programming

The SiI9396 device supports In-System Programming (ISP) to update the firmware in SPI Flash memory. The procedure can be performed by host processor through either the I^2C or SPI interface.

2.15.Consumer Electronics Control

The SiI9396 device supports the Consumer Electronics Control (CEC) interface for the HDMI interface. The CEC interface provides CEC compliant signals between CEC devices and a CEC master. The CEC Interface makes CEC control easy and straightforward, removing the burden of requiring the host processor to perform these low-level transactions on the CEC bus and can be configured and controlled by the internal Micro Controller Unit (MCU).

3. Electrical Specifications

3.1. Absolute Maximum Conditions

Table 3.1. Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units	Notes
AVDD10	Analog Core Supply Voltage	–0.3	—	1.25	V	1, 2, 3
VDD10	Digital Core Supply Voltage	–0.3	—	1.25	V	1, 2, 3
FVDD10	Fractional PLL Supply Voltage	–0.3	—	1.25	V	1, 2, 3
MVDD10	Audio PLL Supply Voltage	–0.3	—	1.25	V	1, 2
AVDD_PLL	Transmitter PLL Power Supply Voltage	–0.3	—	1.25	V	1, 2, 3
AVDD_DP	TMDS Transmitter Core Supply Voltage	–0.3	—	1.25	V	1, 2, 3
RX_VDDH	TMDS Receiver Termination Voltage	–0.3	—	4.0	V	1, 2, 3
TX_VDDH	TMDS Transmitter Termination Voltage	–0.3	—	4.0	V	1, 2
VDDIO33	Digital IO Supply Voltage	–0.3	—	4.0	V	1, 2, 3
XTAL_VDD33	Crystal Oscillator Power	–0.3	—	4.0	V	1, 2
SBVCC5	5 V Standby Power Supply Voltage	–0.3	—	5.7	V	1, 2
RPWR5V	5 V Input from Power Pin of HDMI Connector	–0.3	—	5.7	V	1, 2
$V_{5V\text{-}Tolerant}$	Input Voltage on 5 V Tolerant Pins	–0.3	—	5.5	V	1, 2, 3, 4
V_{MHL_CD}	Input Voltage on MHL_CD Pins	–0.3	—	3.6	V	1, 2, 3
V_I	Input Voltage	–0.3	—	VDDIO33 + 0.3	V	1, 2, 3
V_O	Output Voltage	–0.3	—	VDDIO33 + 0.3	V	1, 2, 3
T_J	Junction Temperature	0	—	125	°C	—
T_{STG}	Storage Temperature	–65	—	150	°C	—

Notes:
1. Permanent device damage can occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described under Normal Operating Conditions.
3. Voltage undershoot or overshoot cannot exceed absolute maximum conditions.
4. This is for 5 V tolerant pins, such as TX_HPD, INT, TX_DSCL, and TX_DSDA.

3.2. Normal Operating Conditions

Table 3.2. Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Notes
AVDD10	Analog Core Supply Voltage	0.95	1.0	1.05	V	—
VDD10	Digital Core Supply Voltage	0.95	1.0	1.05	V	—
FVDD10	Fractional PLL Supply Voltage	0.95	1.0	1.05	V	—
MVDD10	Audio PLL Supply Voltage	0.95	1.0	1.05	V	—
AVDD_PLL	Transmitter PLL Power Supply Voltage	0.95	1.0	1.05	V	—
AVDD_DP	TMDS Transmitter Core Supply Voltage	0.95	1.0	1.05	V	—
RX_VDDH	TMDS Receiver Termination Voltage	3.13	3.3	3.47	V	1
TX_VDDH	TMDS Transmitter Termination Voltage	3.13	3.3	3.47	V	1
VDDIO33	Digital IO Supply Voltage	3.13	3.3	3.47	V	—
XTAL_VDD33	Crystal Oscillator Power	3.13	3.3	3.47	V	—
SBVCC5	5 V Standby Power Supply Voltage	4.50	5.0	5.50	V	2
RPWR5V	5 V Input from Power Pin of HDMI Connector	4.50	5.0	5.50	V	—
T_A	Ambient Temperature (with power applied)	–20	+25	+85	°C	3
Θ_{ja}	Ambient Thermal Resistance (Theta JA)	—	22	—	°C/W	3
Θ_{jc}	Junction to Case Resistance (Theta JC)	—	—	8	°C/W	3

Notes:

1. The HDMI Specification requires termination voltage to be controlled to 3.3 V ± 5%.
2. SBVCC5 voltage is measured at SBVCC5TP as shown in Figure 3.1.

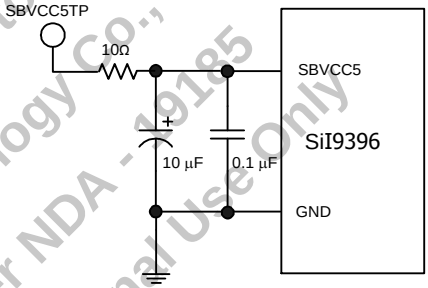


Figure 3.1. Test Point SBVCC5TP for SBVCC5 Measurement

3. Airflow at 0 m/s, 4-layer PCB.

3.3. DC Specification

3.3.1. Digital I/O Specifications

Under normal operating conditions unless otherwise specified.

Table 3.3. DC Digital I/O Specifications

Symbol	Parameter	Pin Type	Conditions	Min	Typ	Max	Units	Notes
V_{IH}	HIGH Level Input Voltage	LVTTL	—	2.0	—	—	V	1
V_{IL}	LOW Level Input Voltage	LVTTL	—	—	—	0.8	V	1
$V_{IH\_MHL\_CD}$	High-level Input Voltage, MHL_CD	LVTTL	—	2.0	—	—	V	1
$V_{IL\_MHL\_CD}$	Low-level Input Voltage, MHL_CD	LVTTL	—	—	—	0.8	V	1
V_{TH+DDC}	LOW to HIGH Threshold, DDC Buses	Schmitt	—	3.0	—	—	V	1, 2
V_{TH-DDC}	HIGH to LOW Threshold, DDC Buses	Schmitt	—	—	—	1.5	V	1, 2
V_{TH+I2C}	LOW-to-HIGH Threshold, I^2C Buses	Schmitt	—	2.0	—	—	V	1, 2
V_{TH-I2C}	HIGH-to-LOW Threshold, I^2C Buses	Schmitt	—	—	—	0.8	V	1, 2
$V_{TH+RESETN}$	LOW to HIGH Threshold, Reset	Schmitt	—	2.0	—	—	V	1, 2
$V_{TH-RESETN}$	HIGH to LOW Threshold, Reset	Schmitt	—	—	—	0.8	V	1, 2
V_{OH}	HIGH Level Output Voltage	LVTTL	—	2.4	—	—	V	1
V_{OL}	LOW Level Output Voltage	LVTTL	—	—	—	0.4	V	1
I_{OL}	Output Leakage Current	—	High impedance	–10	—	10	µA	1
I_{OD4}	4 mA Digital Output Drive	LVTTL	V_{OUT} = 2.4 V	4	—	—	mA	1, 3
			V_{OUT} = 0.4 V	4	—	—	mA	1, 3
$I_{IL\_MHL\_CD}$	Input Leakage Current	LVTTL	High Impedance	—	—	10	µA	1

Notes:

1. Refer to the Pin Descriptions section on page 30 for pin type designations for all package pins.
2. Only these Schmitt trigger input pin thresholds V_{TH+} and V_{TH-} correspond to V_{IH} and V_{IL}.
3. I_{OD} Output applies to all pins defined as LVTTL and LVTTL/Schmitt trigger.

Table 3.4. TMDS Input DC Specifications – HDMI Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{ID}	Differential Mode Input Voltage	—	150	—	1200	mV
V_{ICM}	Common Mode Input Voltage	—	V_{TERM} – 400	—	V_{TERM} – 37.5	mV

Table 3.5. TMDS Input DC Specifications – MHL Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IDC}	Single-ended Input DC Voltage	—	V_{TERM} – 1200	—	V_{TERM} – 300	mV
V_{IDF}	Differential Mode Input Swing Voltage	—	200	—	1000	mV
V_{ICM}	Common Mode Input Swing Voltage	—	170	—	Min (720, 0.85 V_{IDF})	mV

Table 3.6. TMDS Output DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Notes
V_{SWING}	Single-ended Output Swing Voltage	R_{LOAD} = 50 Ω	400	—	600	mV	—
V_H	Single-ended High-level Output Voltage	—	V_{TERM} – 200	—	V_{TERM} + 10	mV	—
V_L	Single-ended Low-level Output Voltage	—	V_{TERM} – 700	—	V_{TERM} – 400	mV	—
$V_{TH+RSEN}$	LOW-to-HIGH Threshold, RSEN	—	0.8	—	1.1	V	1
$V_{TH-RSEN}$	HIGH-to-LOW Threshold, RSEN	—	0.3	—	0.5	V	2

Notes:
1. RSEN deasserted state to asserted state threshold voltage when sink Rx termination transitions from disabled to enabled.
2. RSEN asserted state to deasserted state threshold voltage when sink Rx termination transitions from enabled to disabled.

3.3.2. CBUS I/O Specification

Table 3.7. Digital CBUS I/O Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH_CBUS}	High-level Input Voltage	—	1.0	—	—	V
V_{IL_CBUS}	Low-level Input Voltage	—	—	—	0.6	V
V_{OH_CBUS}	High-level Output Voltage	I_{OH} = 100 µA	1.5	—	1.9	V
V_{OL_CBUS}	Low-level Output Voltage	I_{OL} = –100 µA	—	—	0.2	V
Z_{DSC_CBUS}	Pull-down Resistance – Discovery	—	800	1000	1200	Ω
Z_{ON_CBUS}	Pull-down Resistance – Active	—	90	100	110	kΩ
I_{IL_CBUS}	Input Leakage Current	High Impedance	—	—	1	µA
C_{CBUS}	Capacitance	Power On	—	—	80	pF

3.3.3. CEC DC Specifications

Table 3.8. CEC DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TH+CEC}	LOW to HIGH Threshold	—	2.0	—	—	V
V_{TH-CEC}	HIGH to LOW Threshold	—	—	—	0.8	V
V_{OH_CEC}	HIGH-level Output Voltage	—	2.5	—	—	V
V_{OL_CEC}	LOW-level Output Voltage	—	—	—	0.6	V
I_{IL_CEC}	Input Leakage Current	Power Off; RPWR5V = 0 V	—	—	1.8	µA

3.3.4. DC Power Consumption

Table 3.9. Standby DC Power Consumption

Symbol	Parameter	Video Format	Typical			Maximum			Units
			5 V	3.3 V	1.0 V	5.50 V	3.63 V	1.05 V	
I_{DDSB}	Standby Current	—	3	7	75	3	9	350	mA

Note: All power nets are supplied and no input and output are connected.

Table 3.10. HDMI pass through Mode DC Power Consumption

Symbol	Parameter	Video Format	Typical			Maximum			Units
			5 V	3.3 V	1.0 V	5.50 V	3.63 V	1.05 V	
I_{DDFP}	Full Operation Current	1280 ×720p60	3	53	180	3	54	495	mA
		1920 ×1080p60	3	53	225	3	54	555	mA
		3840 ×2160p30(4:4:4)	3	93	310	3	95	660	mA
		3840 ×2160p60(4:4:4)	3	105	575	3	110	970	mA

Note: Test results will differ depending on TMDS driving current settings of the source.

Table 3.11. DSC with HDMI Pass through Mode DC Power Consumption

Symbol	Parameter	Video Format	Typical			Maximum			Units
			5 V	3.3 V	1.0 V	5.50 V	3.63 V	1.05 V	
I_{DDFP}	Full Operation Current	3840 ×2160p60(4:4:4, 3:1)	3	71	455	3	73	835	mA
		3840 ×2160p60(4:4:4, 2:1)	3	71	500	3	73	885	mA

Table 3.12. MHL to HDMI with DSC Mode DC Power Consumption

Symbol	Parameter	Video Format	Typical			Maximum			Units
			5 V	3.3 V	1.0 V	5.50 V	3.63 V	1.05 V	
I_{DDFP}	Full Operation Current	3840 ×2160p30(4:4:4, 3:1)	4	37	300	5	38	630	mA

Table 3.13. MHL3 to HDMI2 with DSC Mode DC Power Consumption

Symbol	Parameter	Video Format	Typical			Maximum			Units
			5 V	3.3 V	1.0 V	5.50 V	3.63 V	1.05 V	
I_{DDFP}	Full Operation Current	3840 ×2160p60(4:4:4, 3:1)	3	33	570	3	34	975	mA

3.4. AC Specification

3.4.1. TMDS AC Timing Specifications

Table 3.14. TMDS Input Timings – HDMI Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{RXDPS}	Intrapair Differential Input Skew	—	—	—	0.4	T_{BIT}
T_{RXCCS}	Channel-to-Channel Differential Input Skew	—	—	—	$0.2T_{PIXEL}$ + 1.78	ns
F_{RXC}	Differential Input Clock Frequency	—	25	—	300	MHz
T_{RXC}	Differential Input Clock Period	—	3.33	—	40	ns
T_{IJIT}	Differential Input Clock Jitter Tolerance (0.3Tbit)	300 MHz	—	—	100	ps

Table 3.15. TMDS Input Timings – MHL Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{SKEW_DF}	Input Differential Intrapair Skew	—	—	—	93	ps
T_{SKEW_CM}	Input Common-mode Intrapair Skew	—	—	—	93	ps
F_{RXC}	Differential Input Clock Frequency	—	25	—	75	MHz
T_{RXC}	Differential Input Clock Period	—	13.33	—	40	ns
T_{CLOCK_JIT}	Common Mode Clock Jitter Tolerance	—	—	—	$0.3T_{BIT}$ + 266.7	ps
T_{DATA_JIT}	Differential Data Jitter Tolerance	—	—	—	$0.4T_{BIT}$ + 88.88	ps

Table 3.16. TMDS Output Timing AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{TXDPS}	Intrapair Differential Output Skew	—	—	—	0.15	T_{BIT}
T_{TXRT}	Data/Clock Rise Time	20% – 80%	75	—	—	ps
T_{TXFT}	Data/Clock Fall Time	80% – 20%	75	—	—	ps
F_{TXC}	Differential Output Clock Frequency	—	25	—	300	MHz
T_{TXC}	Differential Output Clock Period	—	3.33	—	40	ns
T_{DUTY}	Differential Output Clock Duty Cycle	—	40%	—	60%	T_{TXC}
T_{OJIT}	Differential Output Clock Jitter	—	—	—	0.25	T_{BIT}

3.4.2. CBUS AC Specifications

Table 3.17. CBUS AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{BIT_CBUS}	Bit Time	1 MHz Clock	0.8	—	1.2	µs
T_{BJIT_CBUS}	Bit-to-Bit Jitter	—	–1%	—	+1%	T_{BIT_CBUS}
T_{DUTY_CBUS}	Duty Cycle of 1 Bit	—	40%	—	60%	T_{BIT_CBUS}
T_{R_CBUS}	Rise Time	0.2 V – 1.5 V	5	—	200	ns
T_{F_CBUS}	Fall Time	0.2 V – 1.5 V	5	—	200	ns
ΔT_{RF}	Rise-to-Fall Time Difference	—	—	—	100	ns

3.4.3. Audio Output Specifications

Table 3.18. I²S Output Port AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{TR}	SCK Clock Period (TX)	C_L = 10 pF	1.0	—	—	T_{TR}
T_{HC}	SCK Clock HIGH Time	C_L = 10 pF	0.35	—	—	T_{TR}
T_{LC}	SCK Clock LOW Time	C_L = 10 pF	0.35	—	—	T_{TR}
T_{SU}	Setup Time, SCK to SD/WS	C_L = 10 pF	$0.4T_{TR} – 5$	—	—	ns
T_{HD}	Hold Time, SCK to SD/WS	C_L = 10 pF	$0.4T_{TR} – 5$	—	—	ns
$T_{SCKDUTY}$	SCK Duty Cycle	C_L = 10 pF	40	—	60	% T_{TR}
T_{SCK2SD}	SCK to SD or WS Delay	C_L = 10 pF	–5.0	—	5.0	ns
$T_{MCLKCYC}$	MCLK Cycle Time	C_L = 10 pF	20.0	—	250	ns
F_{MCLK}	MCLK Frequency	C_L = 10 pF	4.0	—	50.0	MHz
$T_{MCLKDUTY}$	MCLK Duty Cycle	C_L = 10 pF	45	—	65	% $T_{MCLKCYC}$

Note: Refer to Figure 4.7 on page 27.

Table 3.19. S/PDIF Output Port AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{SPCYC}	SPDIF Cycle Time	C_L = 10 pF	—	1.0	—	UI[1]
F_{SPDIF}	SPDIF Frequency	—	4.0	—	24.0	MHz
T_{SPDUTY}	SPDIF Duty Cycle	C_L = 10 pF	90.0	—	110.0	% T_{SPCYC}

Notes:
1. Proportional to unit time interval (UI), according to sample rate. Refer to the S/PDIF specification.
2. Refer to Figure 4.8 on page 27 and Figure 4.9 on page 27.

3.4.4. CEC AC Specifications

Table 3.20. CEC AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{R_CEC}	Rise Time	10% – 90%	—	—	250	µs
T_{F_CEC}	Fall Time	90% – 10%	—	—	50	µs

3.4.5. Control Signal AC Timing Specifications

Table 3.21. Control Signal Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Notes
T_{RESET}	RESET# signal LOW time required for reset	—	50	—	—	µs	1, 5
T_{I2CDVD}	SDA Data Valid Delay from SCL falling edge on READ command	CL = 400 pF	—	—	700	ns	2, 6
$t_{SU;DAT}$	I²C data setup time	—	210	—	—	ns	7
T_{HDDAT}	I²C data hold time	0 – 400 kHz	2.0	—	—	ns	3, 6
T_{INT}	Response time for INT output pin from change in input condition (HPD, Receiver Sense, VSYNC change, etc.).	RESET# = HIGH	—	—	100	µs	—
F_{SCL}	Frequency on master DDC SCL signal	—	40	70	100	kHz	4
F_{CSCL}	Frequency on master CSCL signal	—	40	—	400	kHz	—

Notes:

1. Reset on RESET# signal can be LOW as the supply becomes stable (as shown in Figure 4.1), or pulled LOW for at least T_{RESET} (as shown in Figure 4.2).
2. All standard-mode (100 kHz) I²C timing requirements are guaranteed by design. These timings apply to the slave I²C port (pins CSDA and CSCL) and to the master I²C port (pins DSDA and DSCL).
3. This minimum hold time is required by CSCL and CSDA signals as an I²C slave. The device does not include the 300 ns internal delay required by the I²C Specification (Version 2.1, Table 5, note 2).
4. The master DDC block provides an SCL signal for the E-DDC bus. The HDMI Specification limits this to I²C Standard Mode or 100 kHz. Use of the Master DDC block does not require an active IDCK.
5. Not a Schmitt trigger.
6. Operation of I²C pins above 100 kHz is defined by LVTTL levels V_{IH}, V_{IL}, V_{OH}, and V_{OL}. For these levels, I²C speeds up to 400 kHz (fast mode) are supported.
7. In default configuration, operation at 400 kHz does not meet the $t_{SU;DAT}$ data setup time required by the I²C Specification. For advanced configuration information, refer to *SiI9575, SiI9573, and SiI9523 Port Preocess Programmer Reference* (SiI-PR-1054) revision D or later.

3.4.6. SPI Interface Timing

Table 3.22. SPI Control Signal Timing

Symbol	Parameter	Min	Typ	Max	Units	Figure
F_{SPI_CLK}	SPI_CLK Frequency	0.1	8	12	MHz	—
tCSs	SPI_CS_N Setup Time to SPI_CLK	1.05	—	—	ns	Figure 4.5, Figure 4.6
tCSh	SPI_CS_N Hold Time to SPI_CLK	1.25	—	—	ns	
tTXs	SPI_MOSI Setup Time to SPI_CLK	0.45	—	—	ns	
tTXh	SPI_MOSI Hold Time to SPI_CLK	2.0	—	—	ns	
tRXp	SPI_MISO Output Time from SPI_CLK Launch Edge	1.0	—	4.54	ns	Figure 4.6

Note: Under normal operating conditions otherwise specified.

3.4.7. ESD Specifications

Table 3.23. ESD Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes
Latch up	ESD Latch up	±200	—	—	mA	1, 2
HBM	Human Body Model	2000	—	—	V	3
MM	Machine Model	150	—	—	V	4
CDM	Charged Device Model	500	—	—	V	5

Notes:

1. Test is performed at 70 °C.
2. Measured according to JESD78B standard.
3. Measured according to JESD22-A114 standard.
4. Measured according to JESD22-A115 standard.
5. Measured according to JESD22-C101 standard.

4. Timing Diagrams

4.1. Reset Timing Diagrams

Power sequencing is not required for the SiI9396 device. However, to ensure a proper reset, Figure 4.1 and Figure 4.2 must be followed.

VCC must be stable between its limits for Normal Operating Conditions for T_{RESET_VDD} before RESETN goes HIGH, as shown in Figure 4.1. Before accessing registers, RESETN must be pulled LOW for T_{RESET}. This can be done by holding RESETN LOW until T_{RESET_VDD} after stable power, as described above, or by pulling RESETN LOW from a HIGH state for at least T_{RESET}, as shown in Figure 4.2.

Note: VCC can be one of RPWR5V or SBVCC5.

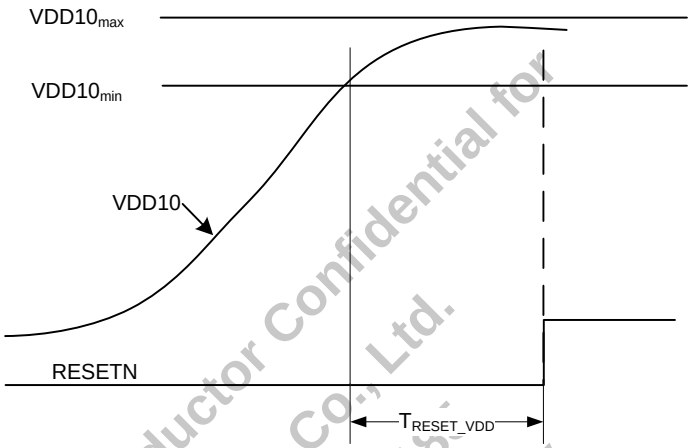


Figure 4.1. Conditions for Use of RESETN

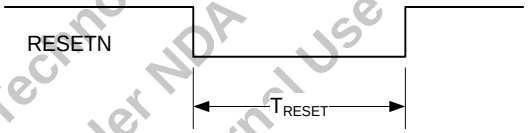


Figure 4.2. RESETN Minimum Timing

4.2. I²C Timing Diagrams

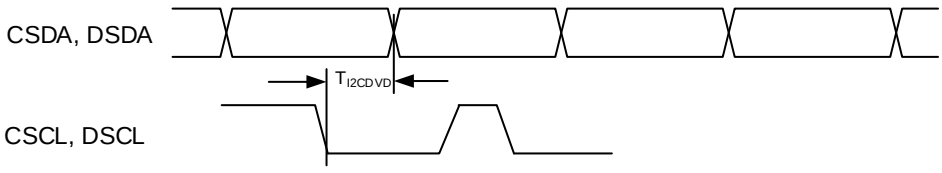


Figure 4.3. I²C Data Valid Delay

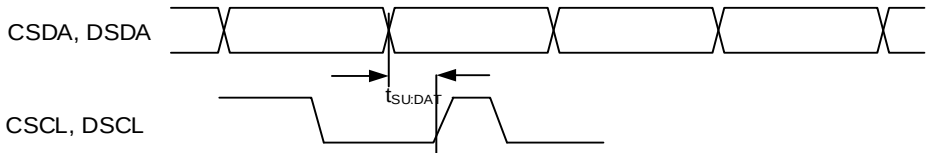


Figure 4.4. I²C Data Setup Timing

4.3. SPI Write/Read Timing

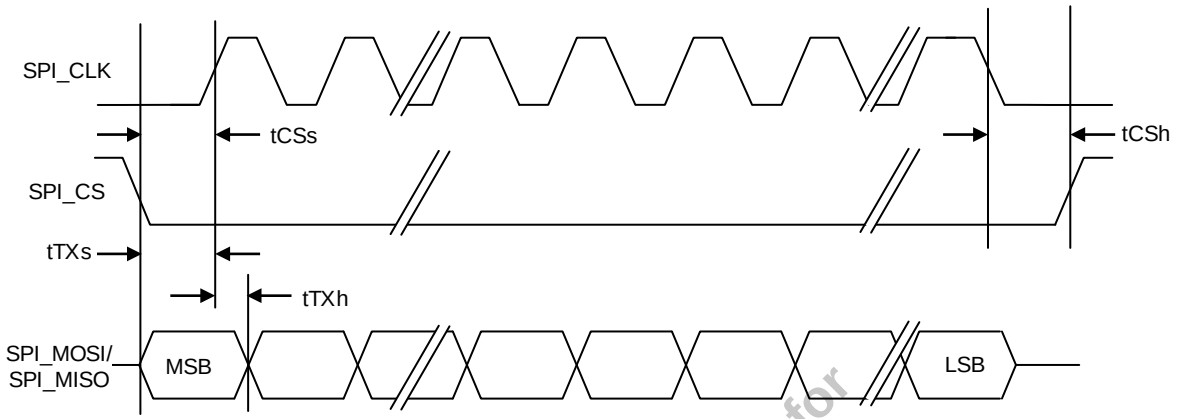


Figure 4.5. SPI Write Setup and Hold Timing

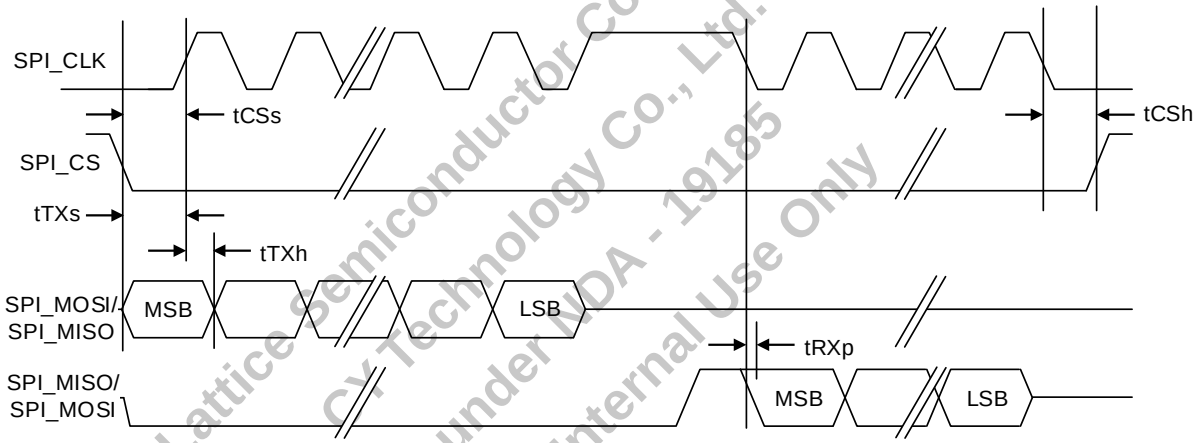


Figure 4.6. SPI Read Setup and Hold Timing

4.4. Digital Audio Output Timing

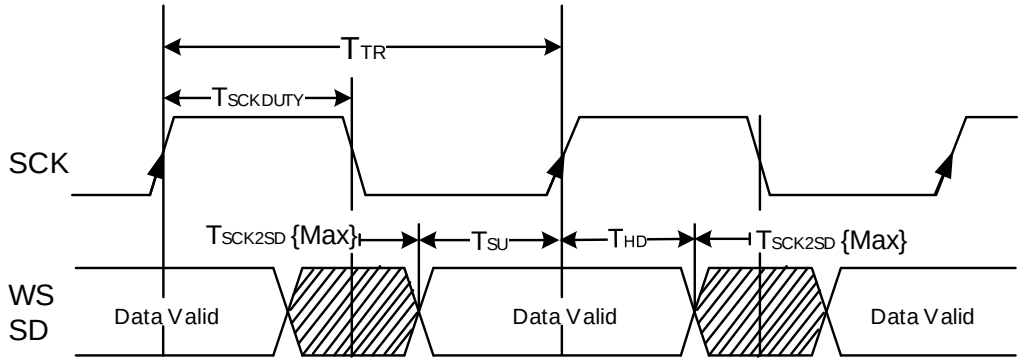


Figure 4.7. I²S Output Timing

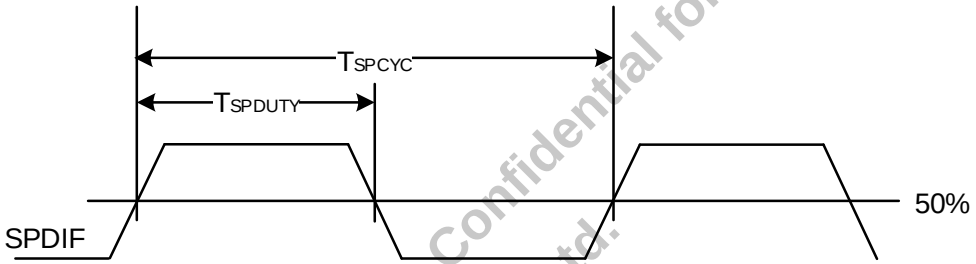


Figure 4.8. S/PDIF Output Timing

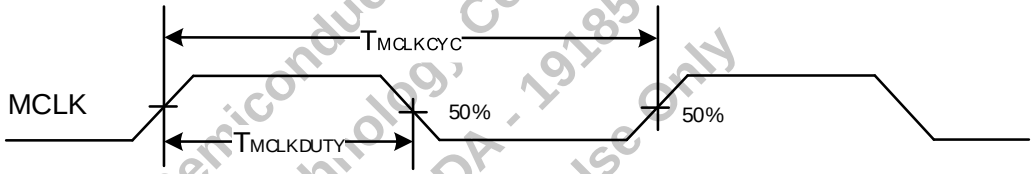


Figure 4.9. MCLK Timing

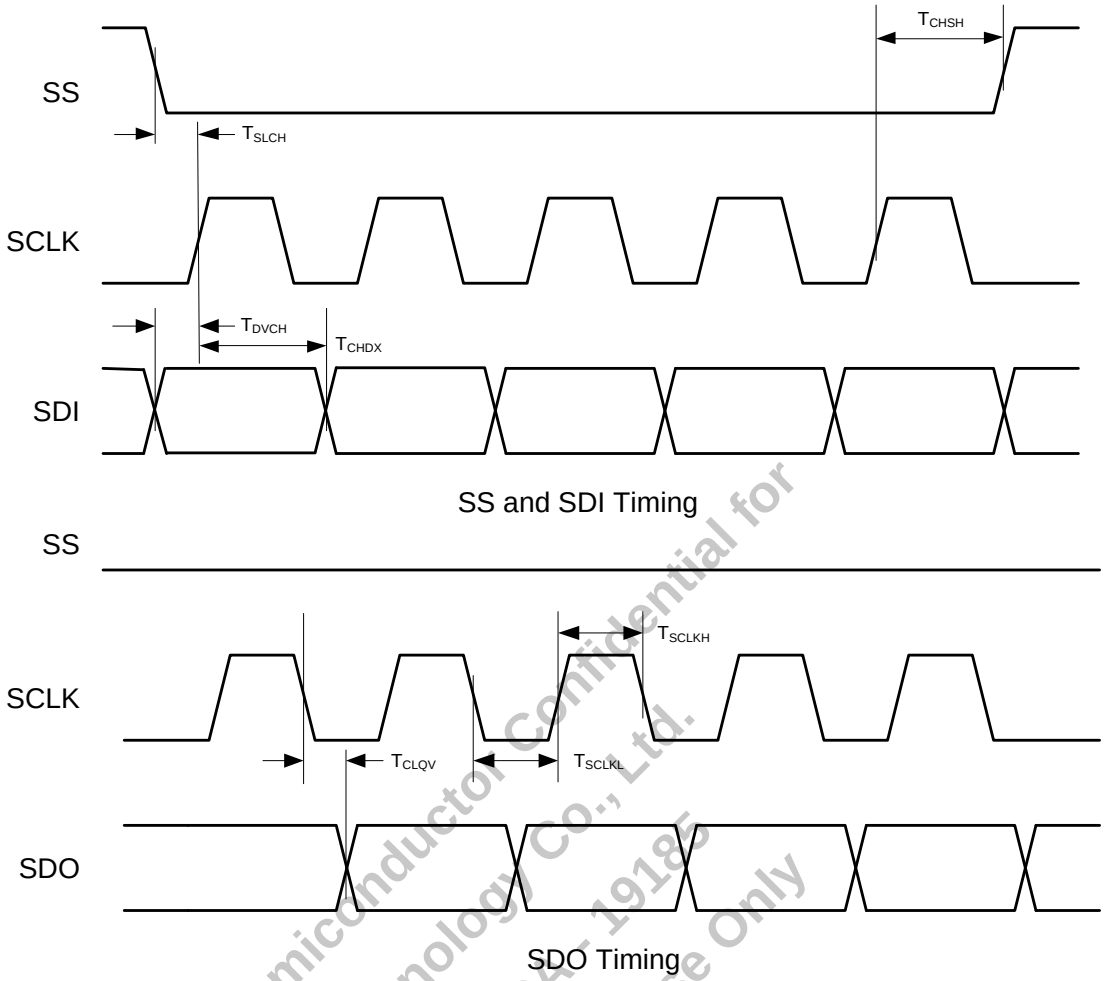


Figure 4.10. SPI Flash Memory Timing

5. Pin Diagram and Descriptions

5.1. Pin Diagram

Figure 5.1 shows the pin diagram of the SiI9396 device. The SiI9396 device is the 76-pin, 9 mm × 9 mm QFN package with an exposed pad (ePad), which must be connected to ground. The Pin Descriptions section describes the functions of each pin.

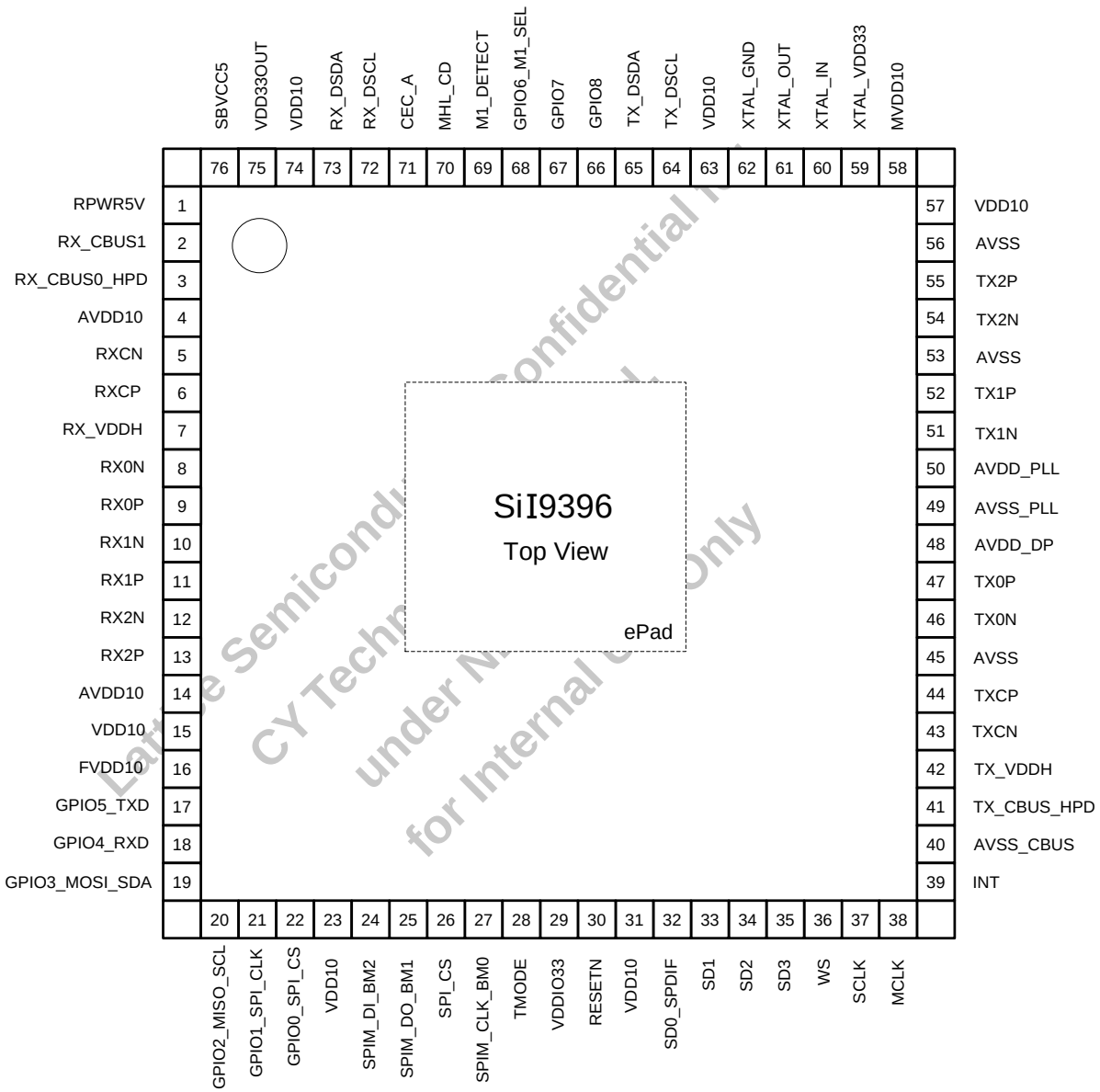


Figure 5.1. SiI9396 Pin Diagram

5.2. Pin Descriptions

5.2.1. SuperMHL/MHL 1, 2, 3/HDMI Receiver Port Pins

Pin Name	Pin	Type	Dir	Description
RX0P	9	TMDS	Input	Receiver Channel 0 TMDS Data Pair
RX0N	8			
RX1P	11			Receiver Channel 1 TMDS Data Pair
RX1N	10			
RX2P	13			Receiver Channel 2 TMDS Data Pair
RX2N	12			
RXCP	6			Receiver TMDS Clock Pair
RXCN	5			
RX_CBUS0_HPD	3	Analog 5 V tolerant	Input/ Output	CBUS0 for superMHL Hot-Plug Detect (HPD) signal output in HDMI mode and CBUS Signal in MHL mode
RX_CBUS1	2	5 V tolerant	Input	CBUS1 for superMHL
M1_DETECT	69	5 V tolerant Open-drain	Output	Detection output for superMHL cable
RX_DSCL	72	LVTTL Schmitt Open-drain 5 V tolerant	Input/ Output	DDC Clock for HDMI receiver
RX_DSDA	73	LVTTL Schmitt Open-drain 5 V tolerant	Input/ Output	DDC Data for HDMI receiver
CEC_A	71	Analog 5 V tolerant, Schmitt triggered, LVTTL	Input/ Output	Interface to CEC devices This pin is compliant with CEC Electrical Specification.
MHL_CD	70	LVTTL Schmitt	Input	MHL cable detect input This pin requires a 300 kΩ pull-down resistor.

Note: When configured as MHL inputs, the RX0P/N pin pair and RXCP/N pin pair carry the respective MHL signals.

5.2.2. HDMI Transmitter Port Pins

Pin Name	Pin	Type	Dir	Description
TXCN	43	TMDS	Output	Transmitter TMDS Clock Pair
TXCP	44			
TX0N	46			Transmitter Channel 0 TMDS Data Pair
TX0P	47			
TX1N	51			Transmitter Channel 1 TMDS Data Pair
TX1P	52			
TX2N	54			Transmitter Channel 2 TMDS Data Pair
TX2P	55			
TX_CBUS_HPD	41	5 V tolerant	Input	Hot Plug Detection Input An external 47 kΩ pull-down resistor is required on this pin.
TX_DSCL	64	LVTTL Schmitt Open-drain 5 V tolerant	Output	DDC clock and data for HDMI transmitter These pins implement true open-drain circuits. External pull-up (1.8 kΩ ± 10% typical) resistors to DDC 5 V are required.
TX_DSDA	65	LVTTL Schmitt Open-drain 5 V tolerant	Input/ Output	

5.2.3. Digital Audio Input/Output Pins

Pin Name	Pin	Type	Dir	Description
MCLK	38	LVTTL	Input/Output	Master clock High Impedance when RESETN is low
SCLK	37	LVTTL	Input/Output	Serial clock High Impedance when RESETN is low
WS	36	LVTTL	Input/Output	I^2S word select or TDM Frame Start (FS) signal High Impedance when RESETN is low
SD3	35	LVTTL	Output	I^2S/TDM serial data output High Impedance when RESETN is low
SD2	34	LVTTL	Output	I^2S/TDM serial data output High Impedance when RESETN is low
SD1	33	LVTTL	Output	I^2S/TDM serial data output High Impedance when RESETN is low
SD0_SPDIF	32	LVTTL	Input/Output	I^2S/TDM serial data or S/PDIF audio output High Impedance when RESETN is low

5.2.4. Control and Configuration Pins

Pin Name	Pin	Type	Dir	Description
RESETN	30	LVTTL Schmitt 5 V tolerant	Input	External Reset Active LOW reset signal to the device. Must be pulled up to PWRMUX_OUT pin. When main power is not provided to the system, the host controller pin that controls the RESETN signal must be in high impedance state.
INT	39	LVTTL 5 V tolerant	Input/Output	Interrupt Input/Output The INT pin can be programmed to be an open-drain output (default) or a push-pull LVTTL output. The polarity can be set to negative (default) or positive asserted. The INT pin is also the interrupt input of internal processor.
SPIM_CLK_BM0	27	LVTTL Schmitt	Output	Function 0: Clock output of SPI master for boot flash Function 1: Strap pin BM0 during reset High Impedance when RESETN is low
SPIM_DI_BM2	24	LVTTL Schmitt	Input	Function 0: Data input of SPI master for boot flash Function 1: Strap pin BM2 during reset
SPIM_DO_BM1	25	LVTTL Schmitt	Output/Input	Function 0: Data output of SPI master for boot flash Function 1: Strap pin BM1 during reset High Impedance when RESETN is low
SPIM_CS	26	LVTTL Schmitt	Output	Chip Select output of SPI master for boot flash External 10 kΩ pull-up resistor is required. High Impedance when RESETN is low
GPIO0_SPI_CS	22	LVTTL Schmitt Open-Drain	Input/Output	Function 0: GPIO0 Function 1: Chip Select input for SPI Slave mode. High Impedance when RESETN is low
GPIO1_SPI_CLK	21	LVTTL Schmitt Open-Drain	Input/Output	Function 0: GPIO1 Function 1: Clock Input/output for SPI High Impedance when RESETN is low
GPIO2_MISO_SCL	20	LVTTL Schmitt Open-Drain	Input/Output	Function 0: GPIO2 Function 1: MISO for SPI Function 2: CSCL for I^2C High Impedance when RESETN is low
GPIO3_MOSI_SDA	19	LVTTL Schmitt Open-Drain	Input/Output	Function 0: GPIO3 Function 1: MOSI for SPI Function 2: CSDA for I^2C High Impedance when RESETN is low
GPIO4_RXD	18	LVTTL Schmitt Open-Drain	Input/Output	Function 0: GPIO 4 Function 1: UART RXD Input of the internal processor High Impedance when RESETN is low
GPIO5_TXD	17	LVTTL Schmitt Open-Drain	Input/Output	Function 0: GPIO 5 Function 1: UART TXD Output of the internal processor High Impendence when RESETN is low
GPIO6_M1_SEL	68	LVTTL Schmitt Open-Drain	Input/Output	Function 0: GPIO 6 Function 1: M1 Cable indication, M1 cable is indicated when the pin is high. Pull up with a 10K resistor for M1 connector, otherwise pull down to ground. High Impendence when RESETN is low
GPIO7	67	LVTTL Schmitt Open-Drain	Input/Output	GPIO 7
GPIO8	66	LVTTL Schmitt Open-Drain	Input/Output	GPIO 8

5.2.5. Crystal Pins

Pin Name	Pin	Type	Dir	Description
XTAL_OUT	61	Analog	Output	Crystal clock output*
XTAL_IN	60	Analog	Input	Crystal clock input*

***Note:** For superMHL (3 Lanes) transmitter use, a 24 MHz crystal or oscillator clock source is required for operation. For audio extraction use, a 27 MHz crystal or oscillator clock source is required for operation. Refer to Figure 5.2.

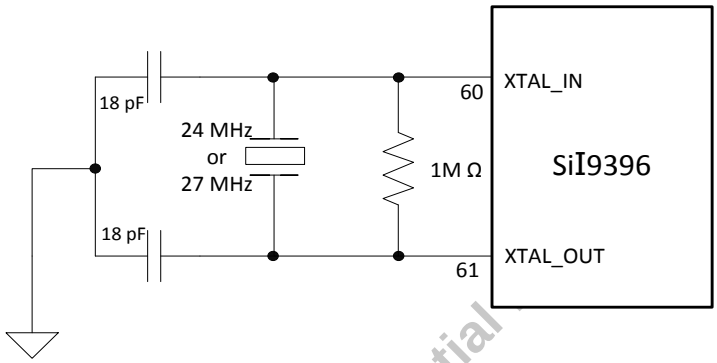


Figure 5.2. Crystal Circuit

5.2.6. Power and Ground Pins

Pin Name	Pin	Type	Description	Supply
SBVCC5	76	Power	Local Power from system. If there is no RPWR5V input, an active 5 V power input of this pin is required. This pin requires a 10 Ω series resistor.	5 V
RPWR5V	1	Power	5 V detection input port for respective HDMI receiver port. Connect to 5 V signal from HDMI input connector. This pin requires a 10 Ω series resistor, a 5.1 kΩ pull down resistor, and at least a 1 µF capacitor to ground.	5 V
RX_VDDH	7	Power	TMDS receiver termination power	3.3 V
TX_VDDH	42	Power	TMDS transmitter termination power	3.3 V
VDDIO33	29	Power	IO power supplies	3.3 V
XTAL_VDD33	59	Power	XTAL power supply	3.3 V
VDD33OUT	75	Power	Internal regulator 3.3 V output This pin requires an external 4.7 µF and 100nF capacitor to ground. Must not be used as any external power supply.	3.3 V
AVDD10	4,14	Power	TMDS receiver core VDD	1.0 V
VDD10	15, 23, 31, 57, 63, 74	Power	Core VDD	1.0 V
FVDD10	16	Power	Fractional PLL power supplies	1.0 V
AVDD_DP	48	Power	TMDS transmitter core power supply	1.0 V
AVDD_PLL	50	Power	Transmitter PLL power supply	1.0 V
MVDD10	58	Power	Audio PLL power supply	1.0 V
AVSS_CBUS	40	Ground	Ground for CBUS TX	Ground
AVSS_PLL	49	Ground	Transmitter PLL Ground	Ground
AVSS	45, 53, 56	Ground	Transmitter Analog Ground	Ground
XTAL_GND	62	Ground	XTAL Ground	Ground
GND	ePad	Ground	The ePad must be soldered to ground, as this is the only ground connection for the device.	GND

5.2.7. Reserved Pins

Pin Name	Pin	Type	Description
TMODE	28	Reserved	Must be connected to the ground.

6. Feature Information

6.1. DSC Decompression Support

The SiI9396 device supports VESA DSC algorithm. This visual lossless compression algorithm only consumes three to four lines of latency for decompression as well as three to four lines of latency for compression.

The SiI9396 bridge supports low latency and visually lossless compression algorithm of VESA DSC which is line based and supports compress ratio up to 2:1, 2.5:1 and 3:1.

The Source device that supports video compression is to acknowledge the SiI9396 bridge for the original video format through the VSIF with compression ratio, algorithm, parameter set, startup conditions and target timing.

Table 6.1 shows the supported DSC video formats.

Table 6.2, Table 6.3 and Table 6.4 list the detailed video timings of the DSC supported formats and their compressed input timings in 2:1, 2.5:1 and 3:1 compression ratios, respectively.

Table 6.1. Supported DSC Video Formats

Video Resolution	Pixel Format	Compression Ratio	Component Depth (bpc)	Frame Rate (Hz)
1920 x 1080	RGB	3:1/2:1	8	50/59.94/60
	YCbCr 4:4:4	3:1/2:1	8	
3840 x 2160	RGB	3:1/2:1	8	23.976/24/25/29.97/30
	YCbCr 4:4:4	3:1/2:1	8	
	YCbCr 4:2:0	2:1	8	
3840 x 2160	RGB	3:1/2:1	8	50/59.94/60
	YCbCr 4:4:4	3:1/2:1	8	
	YCbCr 4:2:0	2:1	8	
		2.5:1	10	

Table 6.2. DSC Decompression – 2:1 Compression Ratio Timing Details (8 bpc)

	Output Timings									Input Timings (2:1 DSC Compression)						
VIC ID	Pixel Format	Frame Rate	Hactive	Hblank	Htotal	Vactive	Vblank	Vtotal	TMDS Clock (MHz)	Hactive	Hblank	Htotal	Vactive	Vblank	Vtotal	TMDS Clock (MHz)
31	RGB/ YCbCr 4:4:4	50	1920	720	2640	1080	45	1125	148.5	960	360	1320	1080	45	1125	74.25
16	RGB/ YCbCr 4:4:4	60	1920	280	2200	1080	45	1125	148.5	960	184	1144	1080	45	1125	77.22
		59.94	1920	280	2200	1080	45	1125	148.351648	960	184	1144	1080	45	1125	77.142857
93	RGB/ YCbCr 4:4:4	24	3840	1660	5500	2160	90	2250	297	1920	830	2750	2160	90	2250	148.5
		23.976	3840	1660	5500	2160	90	2250	296.703296	1920	830	2750	2160	90	2250	148.351648
94	RGB/ YCbCr 4:4:4	25	3840	1440	5280	2160	90	2250	297	1920	720	2640	2160	90	2250	148.5
95	RGB/ YCbCr 4:4:4	30	3840	560	4400	2160	90	2250	297	1920	280	2200	2160	90	2250	148.5
		29.97	3840	560	4400	2160	90	2250	296.703296	1920	280	2200	2160	90	2250	148.351648
96	RGB/ YCbCr 4:4:4	50	3840	1440	5280	2160	90	2250	594	1920	720	2640	2160	90	2250	297
	YCbCr 4:2:0	50	3840	1440	5280	2160	90	2250	297	1920	720	2640	1080	45	1125	148.5
97	RGB/ YCbCr 4:4:4	60	3840	560	4400	2160	90	2250	594	1920	280	2200	2160	90	2250	297
		59.94	3840	560	4400	2160	90	2250	593.406593	1920	280	2200	2160	90	2250	296.703296
	YCbCr 4:2:0	60	3840	560	4400	2160	90	2250	297	1920	280	2200	1080	45	1125	148.5

Table 6.3. DSC Decompression – 2.5:1 Compression Ratio Timing Details (10 bpc)

	Output Timings									Input Timings (2.5:1 DSC Compression)						
VIC ID	Pixel Format	Frame Rate	Hactive	Hblank	Htotal	Vactive	Vblank	Vtotal	TMDS Clock (MHz)	Hactive	Hblank	Htotal	Vactive	Vblank	Vtotal	TMDS Clock (MHz)
96	YCbCr 4:2:0	50	3840	1440	5280	2160	90	2250	371.25	2400	900	3300	864	36	900	148.5
97	YCbCr 4:2:0	60	3840	560	4400	2160	90	2250	371.25	1920	280	2200	1080	45	1125	148.5
		59.94	3840	560	4400	2160	90	2250	370.87912	1920	280	2200	1080	45	1125	148.351648

Table 6.4. DSC Decompression – 3:1 Compression Ratio Timing Details (8 bpc)

	Output Timings									Input Timings (3:1 DSC Compression)						
VIC ID	Pixel Format	Frame Rate	Hactive	Hblank	Htotal	Vactive	Vblank	Vtotal	TMDS Clock (MHz)	Hactive	Hblank	Htotal	Vactive	Vblank	Vtotal	TMDS Clock (MHz)
31	RGB/ YCbCr 4:4:4	50	1920	720	2640	1080	45	1125	148.5	640	240	880	1080	45	1125	49.5
16	RGB/ YCbCr 4:4:4	60	1920	280	2200	1080	45	1125	148.5	640	174	814	1080	45	1125	54.945
		59.94	1920	280	2200	1080	45	1125	148.351648	640	174	814	1080	45	1125	54.8901099
93	RGB/ YCbCr 4:4:4	24	3840	1660	5500	2160	90	2250	297	1280	370	1650	2160	90	2250	89.1
		23.976	3840	1660	5500	2160	90	2250	296.703296	1280	370	1650	2160	90	2250	89.010989
94	RGB/ YCbCr 4:4:4	25	3840	1440	5280	2160	90	2250	297	1280	480	1760	2160	90	2250	99
95	RGB/ YCbCr 4:4:4	30	3840	560	4400	2160	90	2250	297	1280	194	1474	2160	90	2250	99.495
		29.97	3840	560	4400	2160	90	2250	296.703296	1280	194	1474	2160	90	2250	99.395604
96	RGB/ YCbCr 4:4:4	50	3840	1440	5280	2160	90	2250	594	1280	480	1760	2160	90	2250	198
97	RGB/ YCbCr 4:4:4	60	3840	560	4400	2160	90	2250	594	1280	194	1474	2160	90	2250	198.99
		59.94	3840	560	4400	2160	90	2250	593.406593	1280	194	1474	2160	90	2250	198.791209

6.2. Video Format Support

The SiI9396 HDMI receiver features a TMDS core having the capability of receiving data up to 6 Gb/s per channel. The total data bandwidth is 18 Gb/s. The SiI9396 device also supports 6 Gb/s superMHL (1 Lane)/MHL 3 input, backward compatible with MHL 1 and MHL 2.

The SiI9396 HDMI/superMHL (3 Lanes) transmitter features a TMDS core having the capability of transmitting data up to 6 Gb/s per channel. The total data bandwidth is 18 Gb/s.

Following sections show the typical video formats supported by the SiI9396 device. More generally, the device can support any video resolution in HDMI pass through mode provided the total bandwidth for the resolution is less than 18 Gb/s. Other resolution pixel frequency of which is higher than 600 MHz cannot be supported. The accurate pixel frequency can be found on the CEA-861-F.

6.2.1. 2D Format Support

Table 6.5 shows the typical 2D video input formats. Table 6.6 shows the typical 2D video output formats.

Table 6.5. Typical 2D Video Input Formats

Mode	Resolution	Color Space and Pixel Depth	Frame Rate (Hz)
HDMI	480i/p (720 × 480i/p)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 24 bpp	60
	576i/p (720 × 576i/p)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 24 bpp	50
	720p (1280 × 720p)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 24 bpp	50/60
	1080i (1920 × 1080i)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 24 bpp	50/60
	1080p (1920 × 1080p)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 24 bpp	24/30/50/60
	4K x 2K(3840 x 2160)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16 bpp	24/25/30/50/60
	4K × 2K (3840 × 2160)	YCbCr 4:2:0 – 16 bpp	50/60
	4K × 2K (4096 × 2160)	YCbCr 4:2:2 – 16 bpp	24/25/30
	4K x 2K(4096 x 2160)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp	60
	VGA (640 × 480p)	RGB 4:4:4 – 24 bpp	60
	WVGA (800 × 480p)	RGB 4:4:4 – 24 bpp	60
	SVGA (800 × 600p)	RGB 4:4:4 – 24 bpp	60
	XGA (1024 × 768p)	RGB 4:4:4 – 24 bpp	60
	SXGA (1280 × 1024)	RGB 4:4:4 – 24 bpp	60

Table 6.5. Typical 2D Video Input Formats (Continued)

Mode	Resolution	Color Space and Pixel Depth	Frame Rate (Hz)
MHL 1/MHL 2	480i (1440 × 480i)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16 bpp	60
	480p (720 × 480p)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16 bpp	60
	576i (1440 × 576i)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16 bpp	50
	576p (720 × 576p)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16 bpp	50
	720p (1280 × 720p)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16 bpp	50/60
	1080i (1920 × 1080i)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 24 bpp	50/60
	1080p (1920 × 1080p)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16 bpp	24/30
	1080p (1920 × 1080p)	YCbCr 4:2:2 – 16 bpp	50/60
	VGA (640 × 480p)	RGB 4:4:4 – 24 bpp	60
	WVGA (800 × 480p)	RGB 4:4:4 – 24 bpp	60
	SVGA (800 × 600p)	RGB 4:4:4 – 24 bpp	60
	XGA (1024 × 768p)	RGB 4:4:4 – 24 bpp	60

Table 6.5. Typical 2D Video Input Formats (Continued)

Mode	Resolution	Color Space and Pixel Depth	Frame Rate (Hz)
superMHL (1 Lane) /MHL 3	480i (1440 × 480i)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16 bpp	60
	480p (720 × 480p)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16 bpp	60
	576i (1440 × 576i)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16 bpp	50
	576p (720 × 576p)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16 bpp	50
	720p (1280 × 720p)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16 bpp	50/60
	1080i (1920 × 1080i)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16 bpp	50/60
	1080p (1920 × 1080p)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16 bpp	24/30/50/60
	4K x 2K(3840 x 2160)	YCbCr 4:2:2 – 24 bpp	24/25/30
	4K × 2K (4096 × 2160)	YCbCr 4:2:2 – 24 bpp	24/25/30
	VGA (640 × 480p)	RGB 4:4:4 – 24 bpp	60
	WVGA (800 × 480p)	RGB 4:4:4 – 24 bpp	60
	SVGA (800 × 600p)	RGB 4:4:4 – 24 bpp	60
	XGA (1024 × 768p)	RGB 4:4:4 – 24 bpp	60
	SXGA (1280 × 1024)	RGB 4:4:4 – 24 bpp	60

Table 6.6.Typical 2D Video Output Formats

Mode	Resolution	Color Space and Pixel Depth	Frame Rate (Hz)
HDMI	480i/p (720 × 480i/p)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 24 bpp	60
	576i/p (720 × 576i/p)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 24 bpp	50
	720p (1280 × 720p)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16 bpp	50/60
	1080i (1920 × 1080i)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16 bpp	50/60
	1080p (1920 × 1080p)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 24 bpp	24/30/50/60
	4K x 2K(3840 x 2160)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16 bpp	24/25/30/50/60
	4K × 2K (3840 × 2160)	YCbCr 4:2:0 – 12 bpp	50/60
	4K × 2K (4096 × 2160)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16 bpp	24/25/30
	4K x 2K(4096 x 2160)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp	60
	VGA (640 × 480p)	RGB 4:4:4 – 24 bpp	60
	WVGA (800 × 480p)	RGB 4:4:4 – 24 bpp	60
	SVGA (800 × 600p)	RGB 4:4:4 – 24 bpp	60
	XGA (1024 × 768p)	RGB 4:4:4 – 24 bpp	60
	SXGA (1280 × 1024)	RGB 4:4:4 – 24 bpp	60
	UXGA (1600 × 1200)	RGB 4:4:4 – 24 bpp	60
	WUXGA (1900x1200)	RGB 4:4:4 – 24 bpp	60
	QXGA (2048x1536)	RGB 4:4:4 – 24 bpp	60
	WQXGA (2560x1600)	RGB 4:4:4 – 24 bpp	60

Table 6.6.Typical 2D Video Output Formats (Continued)

Mode	Resolution	Color Space and Pixel Depth	Frame Rate (Hz)
superMHL (3 Lanes)	480i/p (720 × 480i/p)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 24 bpp	60
	576i/p (720 × 576i/p)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 24 bpp	50
	720p (1280 × 720p)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16 bpp	50/60
	1080i (1920 × 1080i)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16 bpp	50/60
	1080p (1920 × 1080p)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 24 bpp	24/30/50/60
	4K x 2K(3840 x 2160)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16 bpp	24/25/30/50/60
	4K × 2K (3840 × 2160)	YCbCr 4:2:0 – 12 bpp	50/60
	VGA (640 × 480p)	RGB 4:4:4 – 24 bpp	60
	WVGA (800 × 480p)	RGB 4:4:4 – 24 bpp	60
	SVGA (800 × 600p)	RGB 4:4:4 – 24 bpp	60
	XGA (1024 × 768p)	RGB 4:4:4 – 24 bpp	60
	SXGA (1280 × 1024)	RGB 4:4:4 – 24 bpp	60
	UXGA (1600 × 1200)	RGB 4:4:4 – 24 bpp	60
	WUXGA (1900x1200)	RGB 4:4:4 – 24 bpp	60
	QXGA (2048x1536)	RGB 4:4:4 – 24 bpp	60
	WQXGA (2560x1600)	RGB 4:4:4 – 24 bpp	60

6.2.2. 3D Format Support

Table 6.7 shows the typical 3D video input formats.

Table 6.7. Typical 3D Video Input Formats

Mode	3D Pattern	Resolution	Color Space and Pixel Depth	Frame Rate (Hz)
HDMI	Frame Packing	1080p (1920 × 1080p)	RGB 4:4:4 – 16,18,24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16 bpp	24/48/60
		720p (1280 × 720p)	RGB 4:4:4 – 16,18,24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16 bpp	50/60
	Side-by-Side(Half)	1080i (1920 × 1080i)	RGB 4:4:4 – 16,18,24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16 bpp	50/60
	Top-and-Bottom	1080p (1920 × 1080p)	RGB 4:4:4 – 16,18,24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16 bpp	24
		720p (1280 × 720p)	RGB 4:4:4 – 16,18,24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16 bpp	50/60
superMHL (1 Lane) MHL 1,2,3	Frame Sequential	1080p (1920 × 1080p)	RGB 4:4:4 – 16,18,24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16 bpp	24/48/60
		720p (1280 × 720p)	RGB 4:4:4 – 16,18,24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16 bpp	50/60
	Top-and-Bottom	1080p (1920 × 1080p)	RGB 4:4:4 – 16,18,24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16 bpp	24
		720p (1280 × 720p)	RGB 4:4:4 – 16,18,24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16 bpp	50/60

Table 6.8 shows the typical 3D video output formats.

Table 6.8. Typical 3D Video Output Formats

Mode	3D Pattern	Resolution	Color Space and Pixel Depth	Frame Rate (Hz)
HDMI	Frame Packing	1080p (1920 × 1080p)	RGB 4:4:4 – 16,18,24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16 bpp	24
		720p (1280 × 720p)	RGB 4:4:4 – 16,18,24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16 bpp	50/60
	Top-and-Bottom	1080p (1920 × 1080p)	RGB 4:4:4 – 16,18,24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16 bpp	24
		720p (1280 × 720p)	RGB 4:4:4 – 16,18,24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16 bpp	50/60
superMHL (3 Lanes)	Frame Sequential	1080p (1920 × 1080p)	RGB 4:4:4 – 16,18,24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16 bpp	24/48/60
		720p (1280 × 720p)	RGB 4:4:4 – 16,18,24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16 bpp	50/60
	Top-and-Bottom	1080p (1920 × 1080p)	RGB 4:4:4 – 16,18,24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16 bpp	24
		720p (1280 × 720p)	RGB 4:4:4 – 16,18,24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16 bpp	50/60

6.3. Color Space Conversion

6.3.1. RGB to YCbCr Color Space Converter

The RGB→YCbCr color space converter can convert from video data RGB to standard definition or to high definition YCbCr formats. Table 6.9 shows the conversion formulas that are used. The HDMI AVI packet defines the color space of the incoming video.

Table 6.9. RGB to YCbCr Conversion Formulas

Video Format	Conversion	Formulas
		CE Mode 16 – 235 RGB
VGA	ITU-R BT.601	Y = 0.299R′ + 0.587G′ + 0.114B′ Cb = –0.172R′ – 0.339G′ + 0.511B′ + 128 Cr = 0.511R′ – 0.428G′ – 0.083B′ + 128
WVGA	ITU-R BT.601	
SVGA	ITU-R BT.601	
480p/i	ITU-R BT.601	
576p/i	ITU-R BT.601	
XGA	ITU-R BT.709	Y = 0.213R′ + 0.715G′ + 0.072B′ Cb = –0.117R′ – 0.394G′ + 0.511B′ + 128 Cr = 0.511R′ – 0.464G′ – 0.047B′ + 128
SXGA	ITU-R BT.709	
UXGA	ITU-R BT.709	
WUXGA	ITU-R BT.709	
720p	ITU-R BT.709	
1080i	ITU-R BT.709	
1080p	ITU-R BT.709	

6.3.2. YCbCr to RGB Color Space Converter

The YCbCr→RGB color space converter allows MPEG decoders to interface with RGB-only inputs. The CSC can convert from YCbCr in Standard-Definition (ITU.601) or High-Definition (ITU.709) to RGB. See Table 6.10 for the detailed formulas. Note the difference between RGB range for CE modes and PC modes.

Table 6.10. YCbCr-to-RGB Conversion Formulas

Format Change	Conversion	YCbCr Input Color Range
YCbCr 16-235 Input to RGB 16-235 Output	601*	R′ = Y + 1.371(Cr – 128) G′ = Y – 0.698(Cr – 128) – 0.336(Cb – 128) B′ = Y + 1.732(Cb – 128)
	709	R′ = Y + 1.540(Cr – 128) G′ = Y – 0.459(Cr – 128) – 0.183(Cb – 128) B′ = Y + 1.816(Cb – 128)
YCbCr 16-235 Input to RGB 0-255 Output	601	R′ = 1.164((Y-16) + 1.371(Cr – 128)) G′ = 1.164((Y-16) – 0.698(Cr – 128) – 0.336(Cb – 128)) B′ = 1.164((Y-16) + 1.732(Cb – 128))
	709	R′ = 1.164((Y-16) + 1.540(Cr – 128)) G′ = 1.164((Y-16) – 0.459(Cr – 128) – 0.183(Cb – 128)) B′ = 1.164((Y-16) + 1.816(Cb – 128))

***Note:** No clipping can be done.

6.4. Audio Input/Output

6.4.1. S/PDIF

The S/PDIF stream can carry two-channel uncompressed PCM data (IEC 60958) or a compressed bit stream for multi-channel (IEC 61937) formats. The audio data output logic forms the audio data output stream from the HDMI 1.4 audio packets. The S/PDIF output supports audio sampling rates from 32 to 192 kHz. A separate master clock (MCLK) output, coherent with the S/PDIF output, is provided for time-stamping purpose. Coherent means that the MCLK and S/PDIF are created from the same clock source.

6.4.2. I²S

The I²S bus format is programmable through registers, to allow interfacing with I²S audio DACs or audio DSPs with I²S inputs. Additionally, the audio MCLK frequency is selectable to be an integer multiple of the audio sample rate Fs.

MCLK frequencies support various audio sample rates, as shown in Table 6.11.

Table 6.11. Supported MCLK Frequencies

Multiple Fs	Audio Sample Rate, Fs : I²S and S/PDIF Supported Rates						
	32 kHz	44.1 kHz	48 kHz	88.2 kHz	96 kHz	176.4 kHz	192 kHz
128	4.096 MHz	5.645 MHz	6.144 MHz	11.290 MHz	12.288 MHz	22.579 MHz	24.576 MHz
256	8.192 MHz	11.290 MHz	12.288 MHz	22.579 MHz	24.576 MHz	45.158 MHz	49.152 MHz
384	12.288 MHz	16.934 MHz	18.432 MHz	33.864 MHz	36.864 MHz	—	—
512	16.384 MHz	22.579 MHz	24.576 MHz	45.158 MHz	49.152 MHz	—	—

6.5. SiI9396 Bridge Input and Output Matrix with HDCP

The SiI9396 bridge supports different HDCP modes. See Table 6.12 below for details.

Table 6.12. SiI9396 Input and Output Matrix with HDCP

Device	HDCP Mode	Input			Output	
		HDMI	superMHL (1 Lane)/MHL 3	MHL 1/MHL 2	HDMI	superMHL (3 Lanes)
SiI9396 Bridge	HDCP 1.4	Y	—	Y	Y	—
	HDCP 2.2	Y	Y	N	Y	Y

Notes:

1. Y = Supported, N = Not Supported.
2. The SiI9396 bridge supports two types of HDCP repeater: HDCP 2.2 repeater and HDCP 1.4 repeater.

7. Design Recommendations

The tolerance of all resistors shown in this section is ± 5% unless otherwise noted.

7.1. Power Supplies Decoupling

We recommend that designers include decoupling and bypass capacitors at each power pin in the layout. These are shown schematically in Figure 7.1. Place these components as close as possible to the pins of the SiI9396 device, and avoid routing traces through vias if possible. An example of this layout configuration is shown in Figure 7.2. Connections in one group (such as VDD) can share C2, the ferrite, and C3, with each pin having a separate C1 placed as close to the pin as possible.

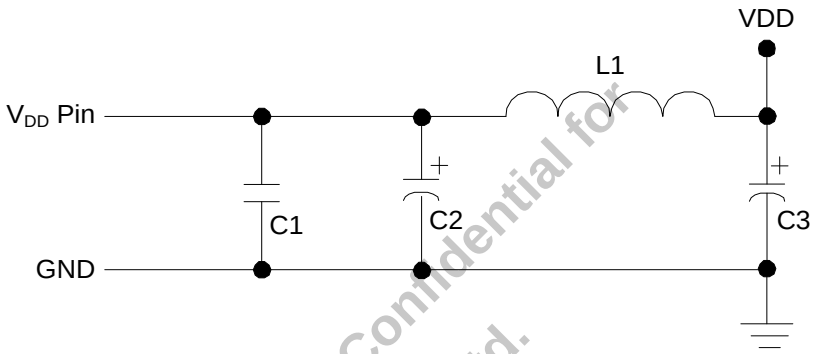


Figure 7.1. Decoupling and Bypass Schematic

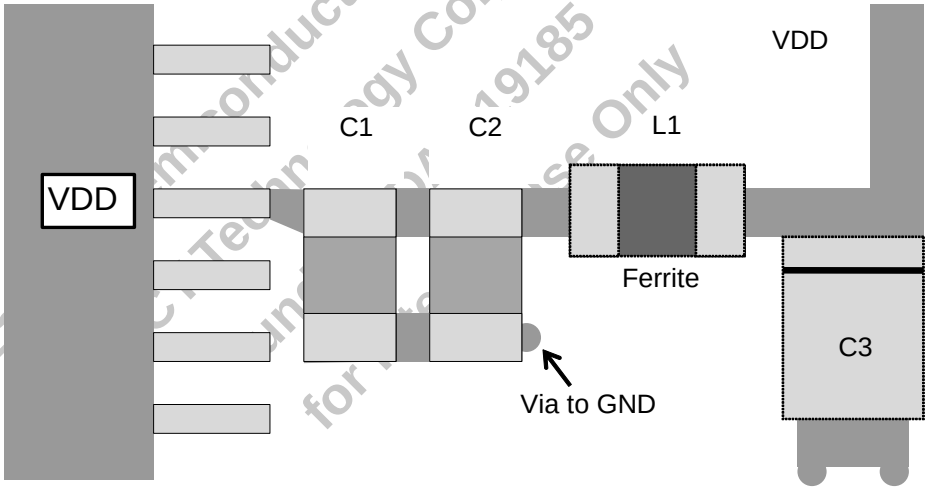


Figure 7.2. Decoupling and Bypass Capacitor Placement

7.2. High-speed TMDS Signals

7.2.1. Layout Guidelines

The layout guidelines below help to ensure signal integrity. We strongly encourage the board designer to follow these guidelines.

- Place the input and output connectors that carry the TMDS signals as close as possible to the device.
- Route the differential lines as directly as possible from the connector to the device when using industry-standard HDMI connectors.
- Route the two traces of each differential pair together.
- Minimize the number of vias through which the signal lines are routed.
- Lay out the MHL input pin traces with a controlled differential impedance of 100 Ω and a common mode impedance of 30 Ω. The differential impedance of the HDMI output pins must be designed within ± 15% of 100 Ω.
- Serpentine traces are not recommended to compensate for inter-pair trace skew.

7.2.2. Electrostatic Discharges Protection

The SiI9396 device can withstand electrostatic discharges (ESD) due to handling during manufacture. In applications where higher protection levels are required, ESD-limiting components can be placed on the differential lines of the device. These components typically have a capacitive effect that reduces the signal quality at higher clock frequencies. Use the lowest capacitance devices possible. ESD components must be placed after the receiver series termination resistors and as close as possible to the input or output connector. In no case can the capacitance value of these components exceed 1 pF.

7.3. Electromagnetic Interference Considerations

Electromagnetic interference (EMI) is a function of board layout, shielding, receiver component operating voltage, frequency of operation, and other factors. When attempting to control emissions, it is important not to place any passive components on the differential signal lines, except the common-mode chokes and ESD protection described earlier. The differential signaling used in HDMI is inherently low in EMI if the routing recommendations noted in the Layout Guidelines section are followed.

For the SiI9396 device, to pass the HDMI CTS test, common mode choke is required by TMDS signals of transmitter side for performance improvement. We recommend using the component: DLW21SN670HQ2L.

The PCB ground plane should extend unbroken under as much of the transmitter device and associated circuitry as possible, with all ground pins of the device using a common ground.

8. Packaging

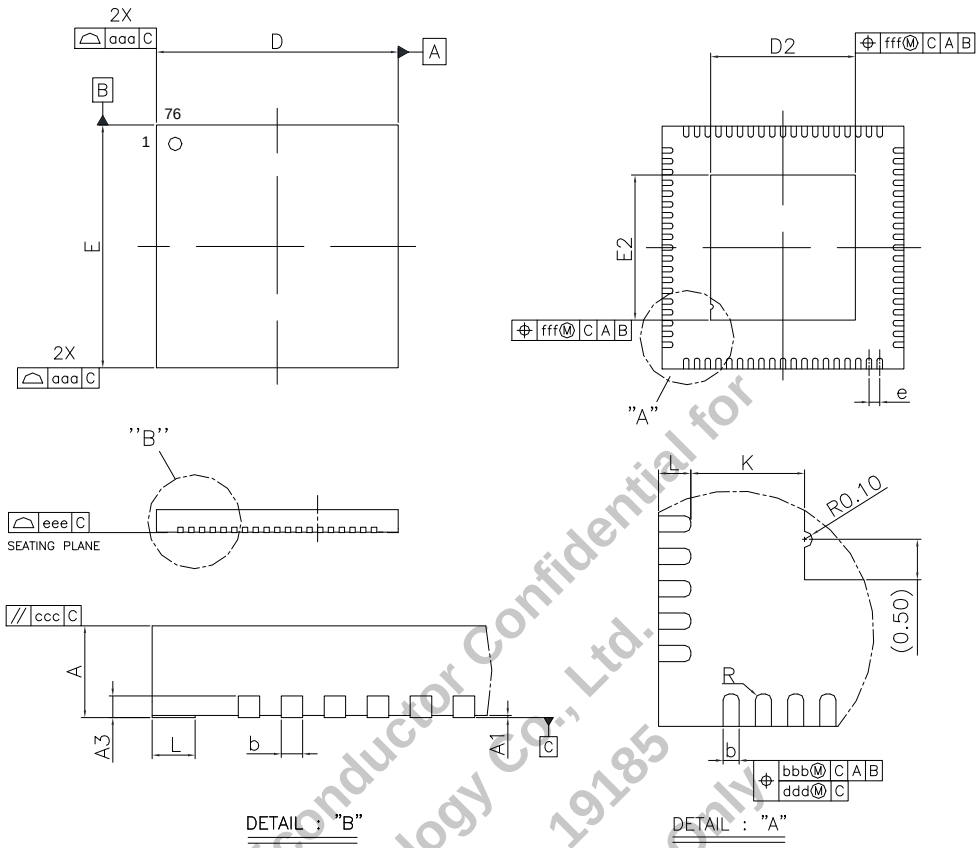
8.1. ePad Requirements

The SiI9396 device is packaged in a 76-pin, 9 mm × 9 mm QFN package with an exposed pad (ePad) that is used for electrical ground of the device and for improving thermal transfer characteristics.

The ePad dimensions are 6.3 mm × 6.3 mm. Soldering the ePad to the ground plane of the PCB is required to meet package power dissipation requirements at full speed operation, and to correctly connect the device circuitry to electrical ground. As a general guideline, a clearance of at least 0.25 mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid the possibility of electrical short circuit. Figure 8.1 on page 50 shows the package dimensions of the SiI9396 device.

8.2. Package Dimensions

Package drawings are not to scale.



JEDEC Package Code MO-220

Symbol	Description	Min	Typ	Max
A	Thickness	0.80	0.85	0.90
A1	Stand-off	0.00	0.02	0.05
A_3	Base thickness		0.20 REF	
D / E	Body size	8.90	9.00	9.10
D2 / E2	ePad size	6.15	6.30	6.45
b	Plated lead width	0.15	0.20	0.25
e	Lead pitch		0.40 BSC	
L	Lead foot length	0.30	0.40	0.50
R	Lead tip radius	0.075	—	—
K	Lead to ePad clearance	0.20	—	—
aaa	—		0.10	
bbb	—		0.07	
ccc	—		0.10	
ddd	—		0.05	
eee	—		0.08	
fff	—		0.10	

All dimensions are in millimeters.

Figure 8.1. 76-pin QFN Package Diagram

8.3. Marking Specification

Marking drawing is not to scale. Figure 8.2 shows the marking diagram of the SiI9396 bridge.

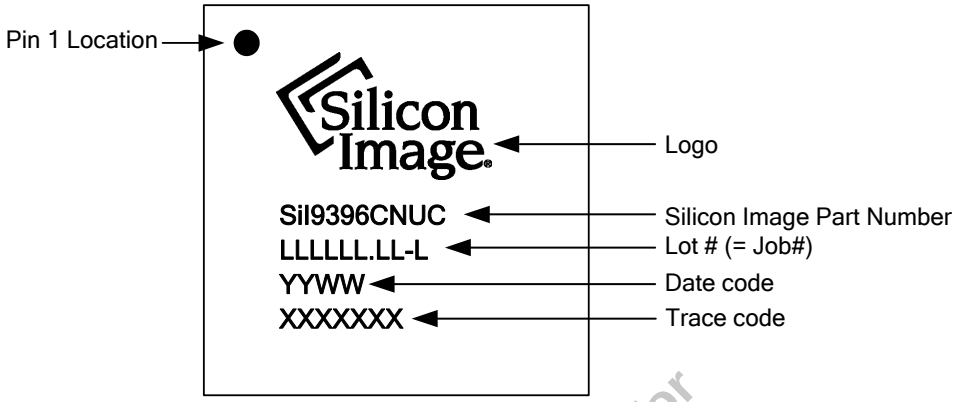


Figure 8.2. Marking Diagram

8.4. Ordering Information

Production Part Numbers:

Part Number	Device
SiI9396 CNUC	SiI9396 superMHL/MHL to HDMI Bridge and superMHL Transmitter with HDCP 2.2 Support

The universal package can be used in lead-free and ordinary process lines.

References

Standards Documents

This is a list of the standards abbreviations appearing in this document.

Abbreviation	Standards publication, organization, and date
CEA-861-F	A DTV Profile for Uncompressed High Speed Digital Interfaces, EIA/CEA, May 2013
DVI	Digital Visual Interface, Revision 1.0, Digital Display Working Group, April 1999
EDDC	Enhanced Display Data Channel Standard, Version 1.1, VESA, March 2004
E-EDID	Enhanced Extended Display Identification Data Standard, Release A Revision 1, VESA, February 2000
E-DID IG	VESA EDID Implementation Guide, VESA, March 2001
HCTS	HDMI Compliance Test Specification, Revision 1.4b, HDMI Consortium, October 2011
HDCP	*High-bandwidth Digital Content Protection*, Revision 2.2, Digital Content Protection, LLC; February 2013 *High-bandwidth Digital Content Protection,* Revision 1.4, Digital Content Protection, LLC, July 2009
HDMI	*High Definition Multimedia Interface*, Revision 2.0, HDMI Consortium, September 2013 *High Definition Multimedia Interface*, Revision 1.4a, HDMI Licensing, LLC, March 2011
MHL	*MHL (Mobile High-Definition Link) Specification*, Version 3.0, MHL, LLC, September 2013 *MHL (Mobile High-definition Link) Specification,* Version 2.0, MHL, LLC, February 2012
superMHL	superMHL Specification, Version 1.0, MHL, LLC, January 2015

For information on the specifications that apply to this document, contact the responsible standards groups appearing on this list.

Standards Group	Web URL
ANSI/EIA/CEA	http://global.ihs.com
DVI	http://www.ddwg.org
HDCP	http://www.digital-cp.com
HDMI	http://www.hdmi.org
MHL	http://www.mhlconsortium.org
VESA	http://www.vesa.org

Lattice Semiconductor Documents

This is a list of the related documents that are available from your Lattice Semiconductor sales representative.

Document	Title
SiI-AR-02006	*SiI9396 Receiver Driver API Reference*

Revision History

Revision B, November 2016

- Changed HBR I^2S extraction support from 384 KHz to 768 KHz in the Audio and Audio Insertion/Extraction sections.
- In Table 2.3. Boot Mode, changed I^2C address from 0x62 to 0x68 when BM1, BM2 = 01.
- Removed S/PDIF Output Port DC Specification table.
- In the DC Power Consumption section, changed maximum value from 1.10 V to 1.05 V.
- Removed 192 Fs MCLK option from the Table 6.11. Supported MCLK Frequencies.
- Updated description in the Power Supplies Decoupling section.

Revision A, June 2016

First production release.

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