Single Channel 10A Isolated Gate Driver

GENERAL DESCRIPTION

The SiLM5350-AQ family is a single channel, isolated gate driver for IGBTs, MOSFETs with 10A source and 10A sink peak output current. The SiLM5350S/R/H-AQ provides a split output that controls the rise and fall times individually. The SiLM5350M/F/P-AQ has internal clamp to prevent false turn-on caused by Miller current.

The SiLM5350-AQ family have 5000 V_{RMS} isolation in SOP8W and 3000 V_{RMS} isolation in SOP8 package per UL1577.

The SiLM5350-AQ family brings significant performance and reliability upgrades over standard optocoupler based gate drivers. Performance highlights include high common mode transient immunity (CMTI), low propagation delay, small pulse width distortion and higher operating temperature.

The high performance and reliability of SiLM5350-AQ makes it ideal for use in all types of motor drives, solar inverters, industrial power supplies, and appliances.

APPLICATION

- AC and brushless DC motor drives
- Renewable energy inverters
- High voltage DC-DC converters
- Industrial power supplies

FEATURES

- AEC-Q100 qualified for automotive application
  - Temperature grade 1: –40°C to +125°C, T_A
- Split outputs (SiLM5350S/R/H-AQ)
- Internal clamping (SiLM5350M/F/P-AQ)
- 10A source output current
- 10A sink output current
- 10A active miller clamp current
- 80ns (Typ) propagation delay
- 40ns (Max) part-to-part delay matching
- 40ns (Max) pulse width distortion
- 150kV/us (Min) common mode transient immunity (CMTI)
- Input side supply range from 3V to 18V
- Driver side supply range from 4V to 30V
  - 12.5V, 8.5V, 5.5V and 3.5V UVLO Options
- TTL Inputs and negative 5V handing capability on Input Pins
- Junction temperature, T_J: –40°C to +150°C
- Safety certifications
  - 5000V_{RMS} SOP8W and 3000V_{RMS} SOP8 isolation for 1 minute per UL 1577
  - CQC certification per GB4943.1-2022
  - DIN VDE 0884-17: 2021-10 (Pending)

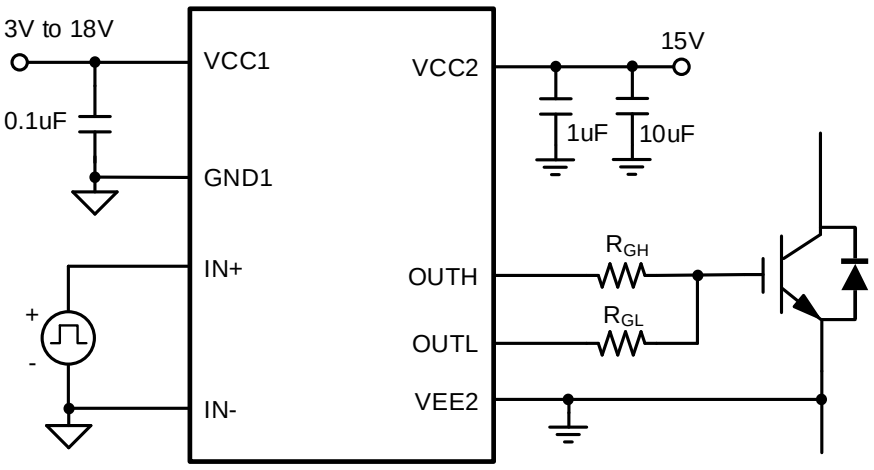
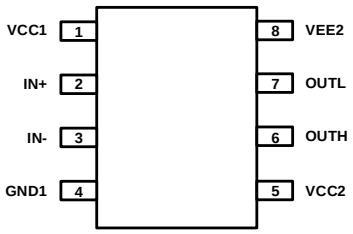
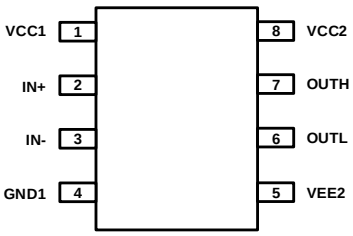
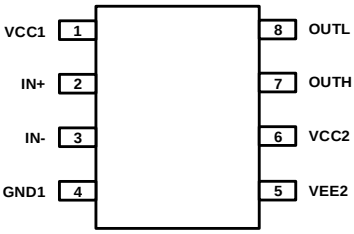
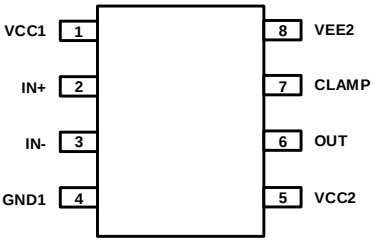
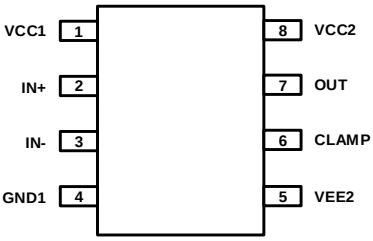
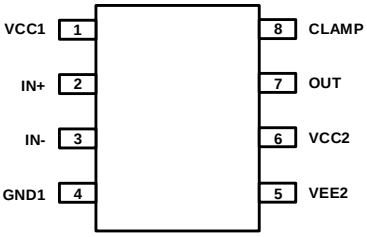


Figure 1. SiLM5350S-AQ Application Circuit

Table of Contents

PIN CONFIGURATION

Part Name	Pin Configuration (Top View)
SiLM5350S-AQ	
SiLM5350R-AQ	
SiLM5350H-AQ	
SiLM5350M-AQ	
SiLM5350F-AQ	
SiLM5350P-AQ	

PIN DESCRIPTION

Table 1. SiLM5350S-AQ Pin Description

No.	Pin	Description
1	VCC1	Input supply voltage
2	IN+	Noninverting voltage control input. This pin is pulled low internally if left open
3	IN-	Inverting voltage control input. This pin is pulled high internally if left open
4	GND1	Input ground
5	VCC2	Positive output supply voltage
6	OUTH	Gate driver pullup output
7	OUTL	Gate driver pulldown output
8	VEE2	Negative output supply voltage

Table 2. SiLM5350R-AQ Pin Description

No.	Pin	Description
1	VCC1	Input supply voltage
2	IN+	Noninverting voltage control input. This pin is pulled low internally if left open
3	IN-	Inverting voltage control input. This pin is pulled high internally if left open
4	GND1	Input ground
5	VEE2	Negative output supply voltage
6	OUTL	Gate driver pulldown output
7	OUTH	Gate driver pullup output
8	VCC2	Positive output supply voltage

Table 3. SiLM5350H-AQ Pin Description

No.	Pin	Description
1	VCC1	Input supply voltage
2	IN+	Noninverting voltage control input. This pin is pulled low internally if left open
3	IN-	Inverting voltage control input. This pin is pulled high internally if left open
4	GND1	Input ground
5	VEE2	Negative output supply voltage
6	VCC2	Positive output supply voltage
7	OUTH	Gate driver pullup output
8	OUTL	Gate driver pulldown output

Table 4. SiLM5350M-AQ Pin Description

No.	Pin	Description
1	VCC1	Input supply voltage
2	IN+	Noninverting voltage control input. This pin is pulled low internally if left open
3	IN-	Inverting voltage control input. This pin is pulled high internally if left open
4	GND1	Input ground
5	VCC2	Positive output supply voltage
6	OUT	Gate driver output

No.	Pin	Description
7	CLAMP	Active Miller clamp input used to prevent false turn-on of the power switches
8	VEE2	Negative output supply voltage

Table 5. SiLM5350F-AQ Pin Description

No.	Pin	Description
1	VCC1	Input supply voltage
2	IN+	Noninverting voltage control input. This pin is pulled low internally if left open
3	IN-	Inverting voltage control input. This pin is pulled high internally if left open
4	GND1	Input ground
5	VEE2	Negative output supply voltage
6	CLAMP	Active Miller clamp input used to prevent false turn-on of the power switches
7	OUT	Gate driver output
8	VCC2	Positive output supply voltage

Table 6. SiLM5350P-AQ Pin Description

No.	Pin	Description
1	VCC1	Input supply voltage
2	IN+	Noninverting voltage control input. This pin is pulled low internally if left open
3	IN-	Inverting voltage control input. This pin is pulled high internally if left open
4	GND1	Input ground
5	VEE2	Negative output supply voltage
6	VCC2	Positive output supply voltage
7	OUT	Gate driver output
8	CLAMP	Active Miller clamp input used to prevent false turn-on of the power switches

FUNCTIONAL BLOCK DIAGRAM

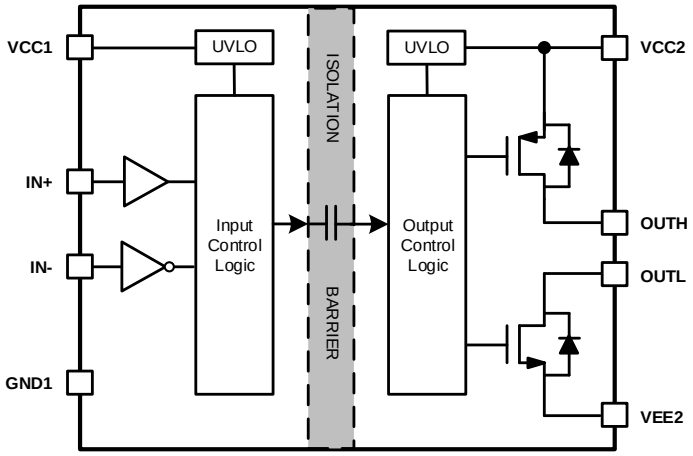


Figure 2. SiLM5350S/R/H-AQ Functional Block Diagram

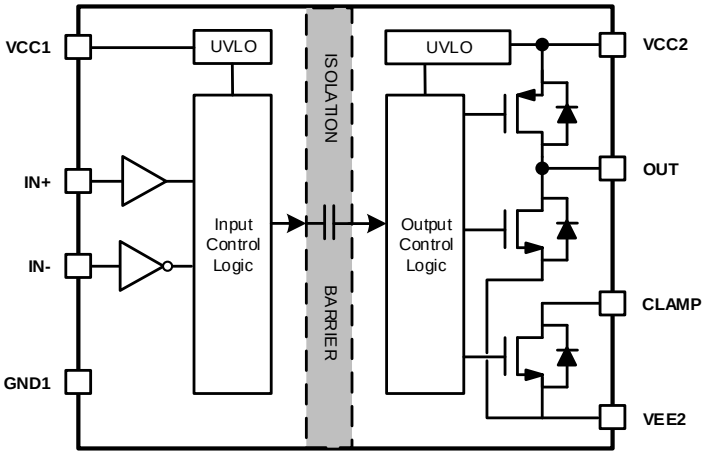


Figure 3. SiLM5350M/F/P-AQ Functional Block Diagram

ORDERING INFORMATION

Order Part No.	Pin Configuration	VCC2 UVLO	Isolation Rating	Package	QTY
SiLM5350SDDCM-AQ	Split Output	12.5V/11.5V	5 kV_{RMS}	SOP8W	1000
SiLM5350SBDCM-AQ	Split Output	8.5V/7.5V	5 kV_{RMS}	SOP8W	1000
SiLM5350SADCM-AQ	Split Output	5.5V/5V	5 kV_{RMS}	SOP8W	1000
SiLM5350SGDCM-AQ	Split Output	3.5V/3V	5 kV_{RMS}	SOP8W	1000
SiLM5350SDBCA-AQ	Split Output	12.5V/11.5V	3 kV_{RMS}	SOP8	2500
SiLM5350SBBCA-AQ	Split Output	8.5V/7.5V	3 kV_{RMS}	SOP8	2500
SiLM5350SABCA-AQ	Split Output	5.5V/5V	3 kV_{RMS}	SOP8	2500
SiLM5350SGBCA-AQ	Split Output	3.5V/3V	3 kV_{RMS}	SOP8	2500
SiLM5350RDDCM-AQ	Split Output	12.5V/11.5V	5 kV_{RMS}	SOP8W	1000
SiLM5350RBDCM-AQ	Split Output	8.5V/7.5V	5 kV_{RMS}	SOP8W	1000
SiLM5350RADCM-AQ	Split Output	5.5V/5V	5 kV_{RMS}	SOP8W	1000
SiLM5350RGDCM-AQ	Split Output	3.5V/3V	5 kV_{RMS}	SOP8W	1000
SiLM5350RDBCA-AQ	Split Output	12.5V/11.5V	3 kV_{RMS}	SOP8	2500
SiLM5350RBBCA-AQ	Split Output	8.5V/7.5V	3 kV_{RMS}	SOP8	2500
SiLM5350RABCA-AQ	Split Output	5.5V/5V	3 kV_{RMS}	SOP8	2500
SiLM5350RGBCA-AQ	Split Output	3.5V/3V	3 kV_{RMS}	SOP8	2500
SiLM5350HDDCM-AQ	Split Output	12.5V/11.5V	5 kV_{RMS}	SOP8W	1000
SiLM5350HBDCM-AQ	Split Output	8.5V/7.5V	5 kV_{RMS}	SOP8W	1000
SiLM5350HADCM-AQ	Split Output	5.5V/5V	5 kV_{RMS}	SOP8W	1000
SiLM5350HGDCM-AQ	Split Output	3.5V/3V	5 kV_{RMS}	SOP8W	1000
SiLM5350HDBCA-AQ	Split Output	12.5V/11.5V	3 kV_{RMS}	SOP8	2500
SiLM5350HBBCA-AQ	Split Output	8.5V/7.5V	3 kV_{RMS}	SOP8	2500
SiLM5350HABCA-AQ	Split Output	5.5V/5V	3 kV_{RMS}	SOP8	2500
SiLM5350HGBCA-AQ	Split Output	3.5V/3V	3 kV_{RMS}	SOP8	2500
SiLM5350MDDCM-AQ	Internal Clamping	12.5V/11.5V	5 kV_{RMS}	SOP8W	1000
SiLM5350MBDCM-AQ	Internal Clamping	8.5V/7.5V	5 kV_{RMS}	SOP8W	1000
SiLM5350MADCM-AQ	Internal Clamping	5.5V/5V	5 kV_{RMS}	SOP8W	1000
SiLM5350MGDCM-AQ	Internal Clamping	3.5V/3V	5 kV_{RMS}	SOP8W	1000
SiLM5350MDBCA-AQ	Internal Clamping	12.5V/11.5V	3 kV_{RMS}	SOP8	2500

Order Part No.	Pin Configuration	VCC2 UVLO	Isolation Rating	Package	QTY
SiLM5350MBBCA-AQ	Internal Clamping	8.5V/7.5V	3 kV_{RMS}	SOP8	2500
SiLM5350MABCA-AQ	Internal Clamping	5.5V/5V	3 kV_{RMS}	SOP8	2500
SiLM5350MGBCA-AQ	Internal Clamping	3.5V/3V	3 kV_{RMS}	SOP8	2500
SiLM5350FDDCM-AQ	Internal Clamping	12.5V/11.5V	5 kV_{RMS}	SOP8W	1000
SiLM5350FBDCM-AQ	Internal Clamping	8.5V/7.5V	5 kV_{RMS}	SOP8W	1000
SiLM5350FADCM-AQ	Internal Clamping	5.5V/5V	5 kV_{RMS}	SOP8W	1000
SiLM5350FGDCM-AQ	Internal Clamping	3.5V/3V	5 kV_{RMS}	SOP8W	1000
SiLM5350FDBCA-AQ	Internal Clamping	12.5V/11.5V	3 kV_{RMS}	SOP8	2500
SiLM5350FBBCA-AQ	Internal Clamping	8.5V/7.5V	3 kV_{RMS}	SOP8	2500
SiLM5350FABCA-AQ	Internal Clamping	5.5V/5V	3 kV_{RMS}	SOP8	2500
SiLM5350FGBCA-AQ	Internal Clamping	3.5V/3V	3 kV_{RMS}	SOP8	2500
SiLM5350PDDCM-AQ	Internal Clamping	12.5V/11.5V	5 kV_{RMS}	SOP8W	1000
SiLM5350PBDCM-AQ	Internal Clamping	8.5V/7.5V	5 kV_{RMS}	SOP8W	1000
SiLM5350PADCM-AQ	Internal Clamping	5.5V/5V	5 kV_{RMS}	SOP8W	1000
SiLM5350PGDCM-AQ	Internal Clamping	3.5V/3V	5 kV_{RMS}	SOP8W	1000
SiLM5350PDBCA-AQ	Internal Clamping	12.5V/11.5V	3 kV_{RMS}	SOP8	2500
SiLM5350PBBCA-AQ	Internal Clamping	8.5V/7.5V	3 kV_{RMS}	SOP8	2500
SiLM5350PABCA-AQ	Internal Clamping	5.5V/5V	3 kV_{RMS}	SOP8	2500
SiLM5350PGBCA-AQ	Internal Clamping	3.5V/3V	3 kV_{RMS}	SOP8	2500

Note1: The R, F, H, P suffixes version are in preview status which means the device has been announced but is not in production. Sample may or may not available. For more information, please contacts Sillumin local sales.

ABSOLUTE MAXIMUM RATINGS

Symbol	Definition	Min	Max	Units
VCC1	Input Supply Voltage	-0.3	20	V
V_{IN+} ,V_{IN-}	Input Signal Voltage	-7	20	V
VCC2-VEE2	Driver supply voltage	-0.3	35	V
CLAMP-VEE2	Internal clamping voltage	VEE2-0.3	VCC2+0.3	V
OUT/OUTH-VEE2	Output signal voltage	VEE2-0.3	VCC2+0.3	V
T_J	Junction temperature	-40	150	°C
T_S	Storage temperature	-55	150	°C

RECOMMENDED OPERATION CONDITIONS

Symbol	Definition	Min	Max	Units
VCC1	Input Supply Voltage	3	18	V
V_{IN+} ,V_{IN-}	Input Signal Voltage	-5	18	V
VCC2-VEE2	Driver supply voltage (12.5V UVLO option)	13.5	30	V
VCC2-VEE2	Driver supply voltage (8.5V UVLO option)	9	30	V
VCC2-VEE2	Driver supply voltage (5.5V UVLO option)	6	30	V
VCC2-VEE2	Driver supply voltage (3.5V UVLO option)	4	30	V
T_A	Ambient temperature	-40	125	°C

ESD RATINGS

Symbol	Definition	Value	Units
V_{ESD}	HBM	±4000	V
	CDM	±1500	V

THERMAL INFORMATION

Symbol	Definition	Value		Unit
		SOP8	SOP8W	
$R_{\theta JA}$	Junction to ambient thermal resistance	108.7	109.6	°C/W
$R_{\theta JC}$	Junction to case (top) thermal resistance	43.1	64.1	°C/W

PACKAGE SPECIFICATIONS

Symbol	Definition	Min	Typ	Max	Units
R_{IO}	Resistance (Input Side to Output Side)		10^{12}		Ω
C_{IO}	Capacitance (Input Side to Output Side)		0.8		pF

INSULATION SPECIFICATIONS

Symbol	Definition	Test Condition	Value		Units
			SOP8	SOP8W	
CLR	External clearance	Shortest terminal to terminal distance through air	>4	>8	mm
CPG	External creepage	Shortest terminal to terminal distance across the package surface	>4	>8	mm
DTI	Distance through the insulation	Minimum internal gap	>16	>16	um
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11), IEC 60112	>600	>600	V
	Material Group		I	I	
	Overvoltage category	Rated mains voltages ≤150V_{RMS}	I-IV	I-IV	
		Rated mains voltages ≤300V_{RMS}	I-III	I-IV	
		Rated mains voltages ≤600V_{RMS}	I-II	I-III	
		Rated mains voltages ≤1000V_{RMS}	I-I	I-II	
DIN V VDE 0884-11(1)					
V_{IORM}	Maximum repetitive peak isolation voltage		1000	1500	V_{PK}
V_{IOWM}	Maximum isolation working voltage		707	1060	V_{RMS}
V_{IOTM}	Maximum transient isolation voltage	60s	4242	7000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage	Test method per IEC62368, 1.2/50us waveform, V_{TEST}=1.3 x V_{IOSM} for SOP8, V_{TEST}=1.6 x V_{IOSM} for SOP8W	6000	6250	V_{PK}
q_{pd}	Apparent charge	Method b2: $V_{pd(m)}$=1.875 x V_{IORM}, tm=1 s	≤5	≤5	pC
	Climatic Category		40/125/21	40/125/21	
	Pollution Degree		2	2	
UL1577(1)					
V_{ISO}	Isolation Voltage	V_{TEST}=V_{ISO}, t=60s (qualification), V_{TEST}=1.2 x V_{ISO}, t=1s (100% production)	3000	5000	V_{RMS}

1. Certification pending

SAFETY RELATED CERTIFICATIONS FOR SOP8

VDE	UL	CQC
DIN VDE 0884-17: 2021-10	UL 1577 component recognition program	Certified according to GB4943.1-2022
Basic Insulation, V_{IORM}=1000V_{PK}, V_{IOTM}=4242V_{PK}	Single protection, 3000 V_{RMS}	Basic insulation, Altitude≤ 5000m
Certification Pending	File number: E521801	File number: CQC23001373092

SAFETY LIMITING VALUES FOR SOP8

Symbol	Parameter	Condition	Value	Unit
I_S	Safety output supply current	$R_{\theta JA}$=108.7°C/W, V_{CC2} = 15V, T_J=150°C, T_A =25°C	73	mA
		$R_{\theta JA}$=108.7°C/W, V_{CC2} = 25V, T_J=150°C, T_A =25°C	44	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$=108.7°C/W, T_J =150°C, T_A =25°C	1150	mW
T_S	Maximum safety temperature		150	°C

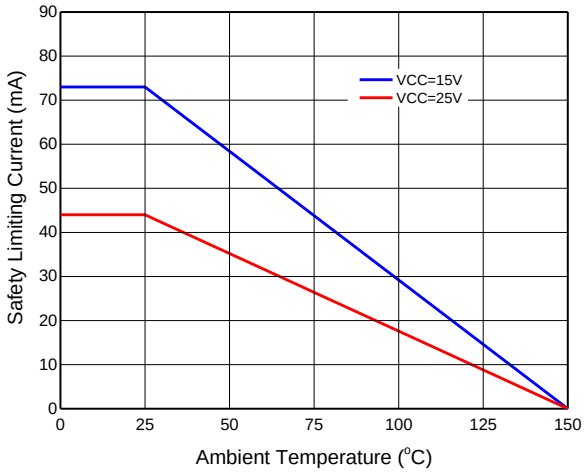


Figure 4. Thermal Derating Curve for Limiting Current per VDE for SOP8 Package

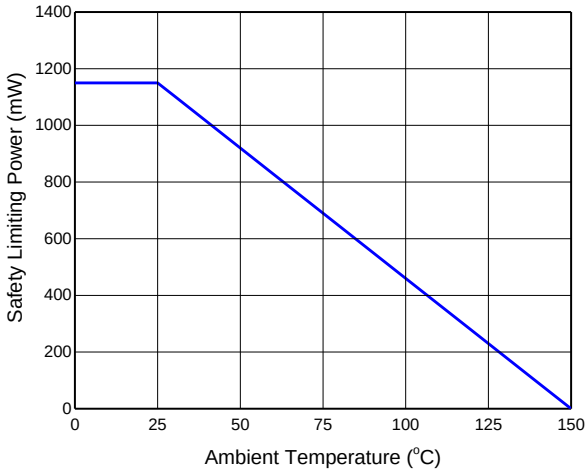


Figure 5. Thermal Derating Curve for Limiting Power per VDE for SOP8 Package

SAFETY RELATED CERTIFICATIONS FOR SOP8W

VDE	UL	CQC
DIN VDE 0884-17: 2021-10	UL 1577 component recognition program	Certified according to GB4943.1-2022
Reinforced Insulation	Single protection, 5000 V_{RMS}	Reinforced insulation Altitude≤ 5000m
Certification Pending	File number: E521801	File number: CQC23001376521

SAFETY LIMITING VALUES FOR SOP8W

Symbol	Parameter	Condition	Value	Unit
I_S	Safety output supply current	$R_{\theta JA}$=109.6°C/W, V_{CC2} = 15V, T_J=150°C, T_A =25°C	72.7	mA
		$R_{\theta JA}$=109.6°C/W, V_{CC2} = 25V, T_J=150°C, T_A =25°C	43.6	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$=109.6°C/W, T_J =150°C, T_A =25°C	1140	mW
T_S	Maximum safety temperature		150	°C

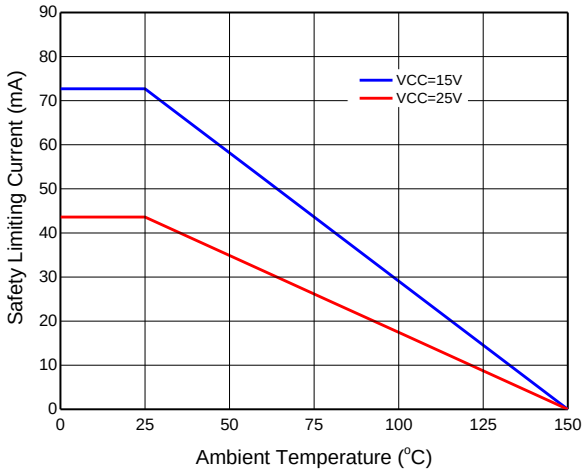


Figure 6. Thermal Derating Curve for Limiting Current per VDE for SOP8W Package

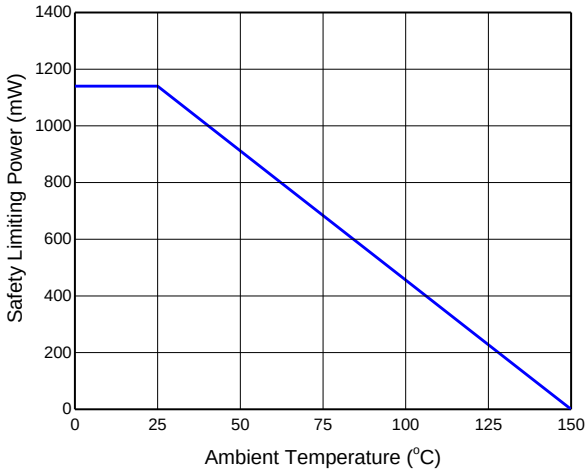


Figure 7. Thermal Derating Curve for Limiting Power per VDE for SOP8W Package

ELECTRICAL CHARACTERISTICS (DC)

VCC1 = 5V, VCC2 = 15V, GND1 = VEE2 = 0V, and T_A = 25°C unless otherwise specified. All min and max specifications are at T_A = -40°C to 125°C

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Input Power Supply						
V_{CC1}	Input Supply Voltage		3		18	V
$V_{UVLO\_VCC1\_R}$	VCC1 UVLO Rising		2.55	2.7	2.85	V
$V_{UVLO\_VCC1\_F}$	VCC1 UVLO Falling		2.35	2.5	2.65	V
$V_{UVLO\_VCC1\_HYS}$	VCC1 UVLO Hysteresis			0.2		V
I_{CC1}	Quiescent Current	V_{IN+} = 0V, V_{IN-} = VCC1		2.0	2.5	mA
	Operation Current	C_{LOAD}=1nF, f_{sw}= 50kHz, (50% Duty Cycle)		2.6	3.3	mA
Logic Interface						
V_{IH}	High Level Input Threshold Voltage at IN+ and IN-		2			V
V_{IL}	Low Level Input Threshold Voltage at IN+ and IN-				0.8	V
R_{PD}	Pull down Resistance on IN+			180		kΩ
R_{PU}	Pull up Resistance on IN-			180		kΩ
Driver Power Supply						
$V_{UVLO\_VCC2\_R}$	VCC2 UVLO Rising VCC2-VEE2	3.5V UVLO Version	3.2	3.5	3.8	V
		5.5V UVLO Version	5.1	5.5	5.9	V
		8.5V UVLO Version	8	8.5	9	V
		12.5V UVLO Version	11.5	12.5	13.5	V
$V_{UVLO\_VCC2\_F}$	VCC2 UVLO Falling VCC2-VEE2	3.5V UVLO Version	2.7	3	3.3	V
		5.5V UVLO Version	4.6	5	5.4	V
		8.5V UVLO Version	7	7.5	8	V
		12.5V UVLO Version	10.5	11.5	12.5	V
$V_{UVLO\_VCC2\_HYS}$	VCC2 UVLO Hysteresis VCC2-VEE2	3.5V UVLO Version		0.5		V
		5.5V UVLO Version		0.5		V
		8.5V UVLO Version		1		V
		12.5V UVLO Version		1		V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{CC2}	Quiescent Current	V_{IN+} = 0V, V_{IN-} = VCC1		1.4	2.1	mA
	Operation Current	C_{LOAD}=1nF, f_{sw}= 50kHz, (50% Duty Cycle)		2.7	3.5	mA
OUTPUT						
I_{OH}	Peak Source Current			10		A
I_{OL}	Peak Sink Current			10		A
I_{OH}	Peak Source Current	VCC2=5V, only for 3.5V UVLO version		5.8		A
I_{OL}	Peak Sink Current	VCC2=5V, only for 3.5V UVLO version		8.0		A
V_{OH}	High Level Output Voltage	I_O=-20mA		8	15	mV
V_{OL}	Low Level Output Voltage	I_O=20mA		8	15	mV
V_{OUTSD}	Active pulldown voltage on OUT	I_{OUT}=1A, VCC2 Open		1.8	2.5	V
Active Miller Clamp						
I_{CLAMP}	Clamp low level current			10		A
V_{CLAMP}	Clamp low level voltage	I_{CLAMP}=20mA		7	13	mV
$V_{CLAMP-TH}$	Clamp threshold voltage		1.8	2	2.2	V

SWITCHING CHARACTERISTICS (AC)

VCC1 = 5V, VCC2 = 15V, GND1 = VEE2 = 0V, and T_A = 25°C unless otherwise specified. All min and max specifications are at T_A = -40°C to 125°C

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{PLH}	Propagation delay, Low to High	C_{LOAD}=1nF, f_{sw}=20kHz, (50% Duty Cycle)		80	130	ns
t_{PHL}	Propagation delay, High to Low			80	130	ns
t_{PWD}	Pulse Width Distortion				40	ns
t_{PDD}	Propagation Delay Difference Between Any Two Parts				40	ns
t_r	Turn on rise time	C_{LOAD}=1nF			15	ns
t_f	Turn off fall time	C_{LOAD}=1nF			15	ns
t_{UVLO_REC1}	VCC1 UVLO Recovery Delay	V_{CC1} Rising from 0V to 5V		12		us
t_{UVLO_REC2}	VCC2 UVLO Recovery Delay	V_{CC2} Rising from 0V to 15V		20		us
$CMTI_H$	Output High Level Common Mode Transient Immunity	V_{CM}=1000V, V_{CC}=15V, T_A=25°C	150	200		kV/us
$CMTI_L$	Output Low Level Common Mode Transient Immunity	V_{CM}=1000V, V_{CC}=15V, T_A=25°C	150	200		kV/us

PARAMETER MEASUREMENT INFORMATION

Propagation Delay, Rise Time and Fall Time

Figure 8 shows the propagation delay, rise and fall times for noninverting configuration. Figure 9 shows the propagation delay, rise and fall times for inverting configuration.

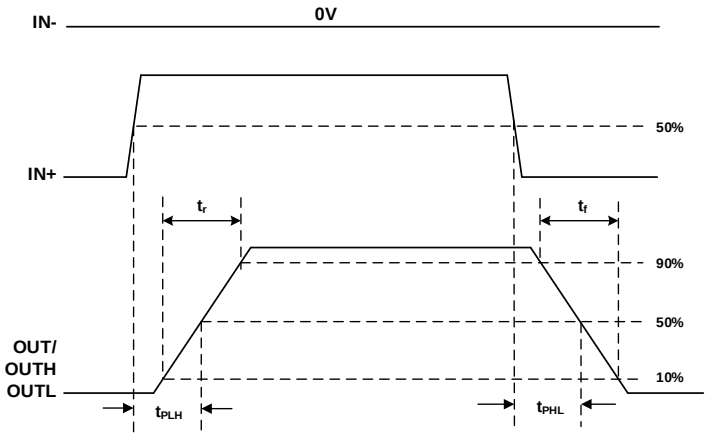


Figure 8. Propagation Delay, Rise Time and Fall Time in Noninverting Configuration

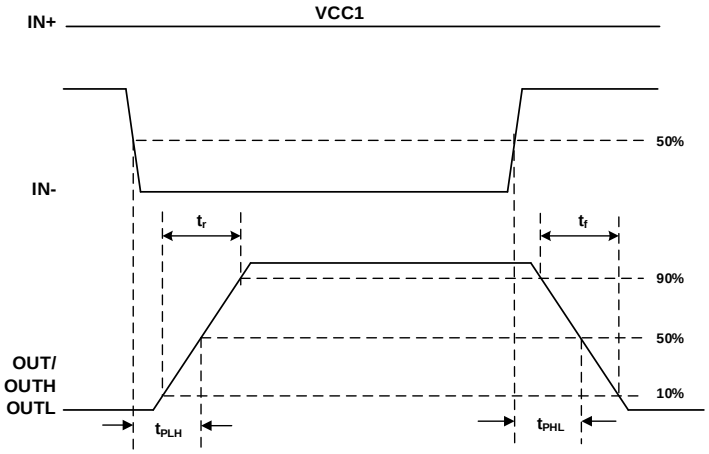


Figure 9. Propagation Delay, Rise Time and Fall Time in Inverting Configuration

CMTI Testing

Figure 10 and Figure 11 show the simplified diagram of the CMTI testing.

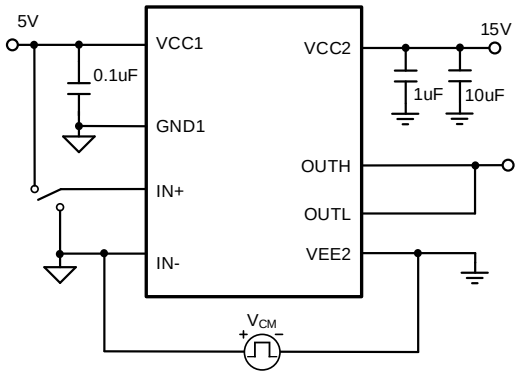


Figure 10. CMTI Test for SiLM5350S/R/H-AQ

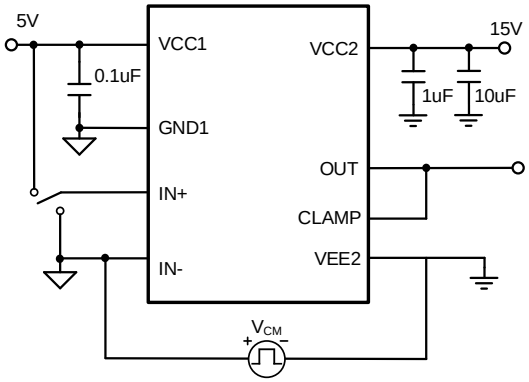


Figure 11. CMTI Test for SiLM5350M/F/P-AQ

TYPICAL PERFORMANCE CHARACTERISTICS

T_A=25°C, VCC1=5V, VCC2=15V, C_{LOAD}=1nF, unless otherwise specified

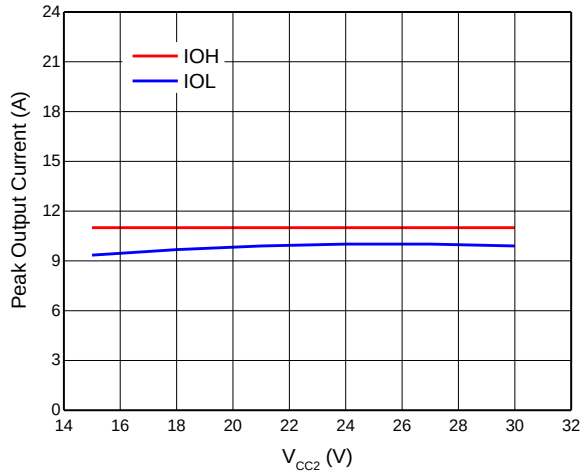


Figure 12. Output Drive Current vs Output Voltage

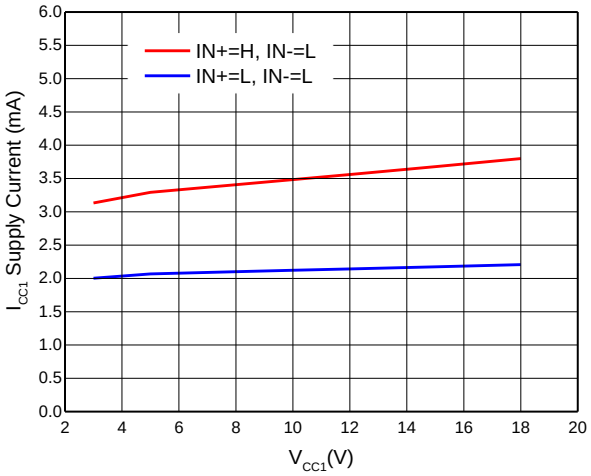


Figure 13. I_{CC1} Supply Current vs V_{CC1} Voltage

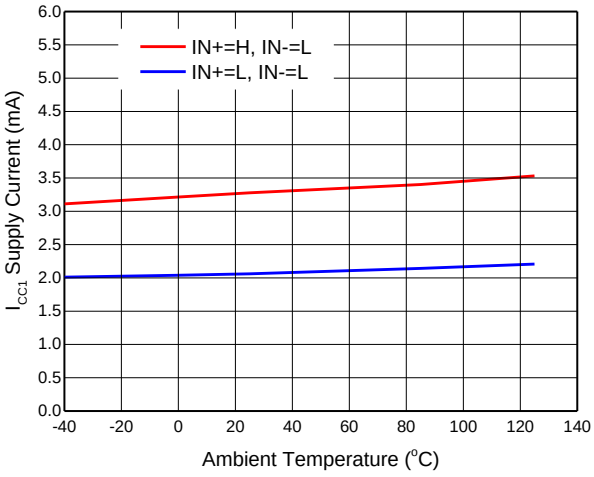


Figure 14. I_{CC1} Supply Current vs Temperature

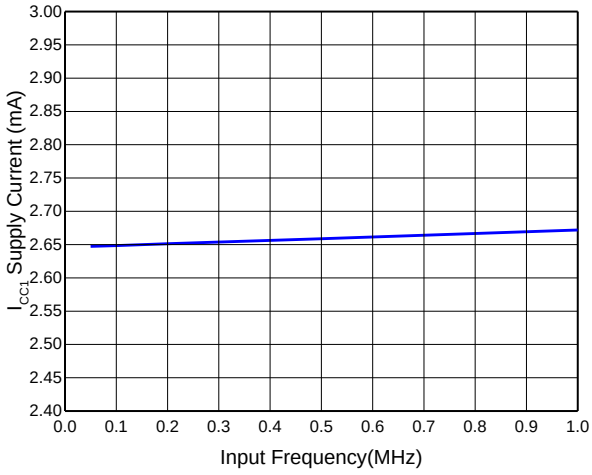


Figure 15. I_{CC1} Supply Current vs Input Frequency(Duty Cycle=50%)

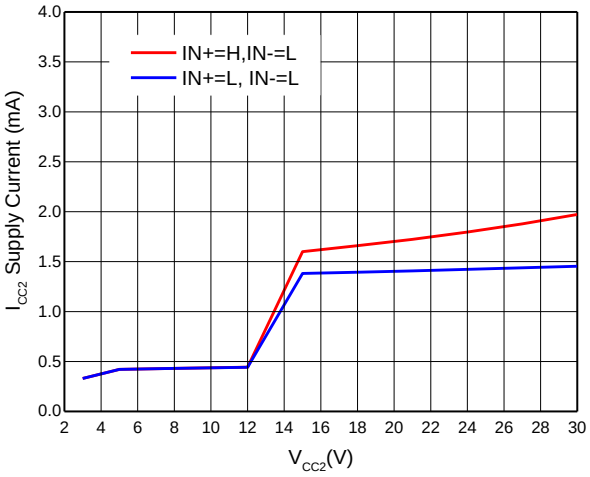


Figure 16. I_{CC2} Supply Current vs V_{CC2} Voltage (UVLO=12.5V)

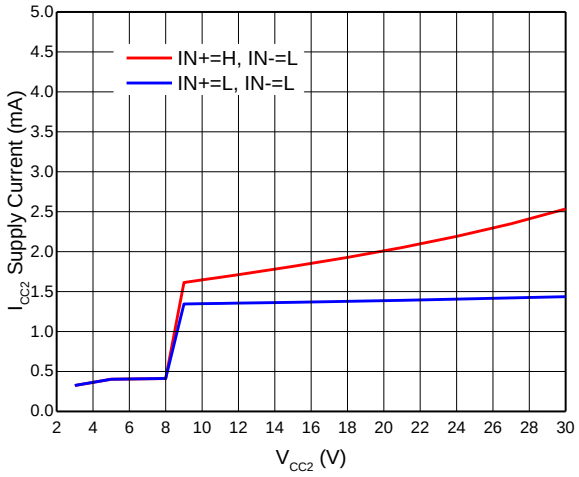


Figure 17. I_{CC2} Supply Current vs V_{CC2} Voltage (UVLO=8.5V)

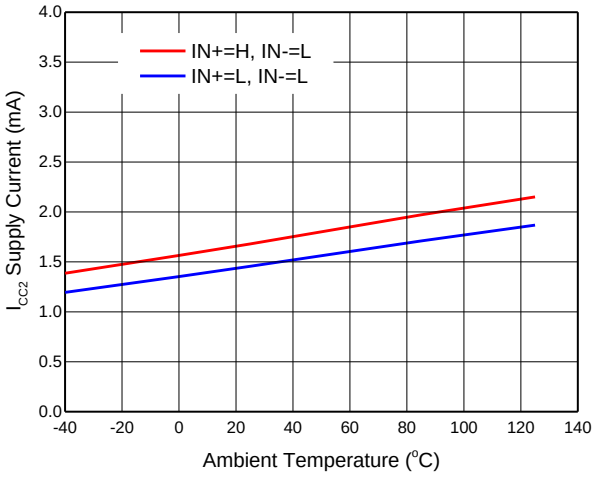


Figure 18. I_{CC2} Supply Current vs Temperature

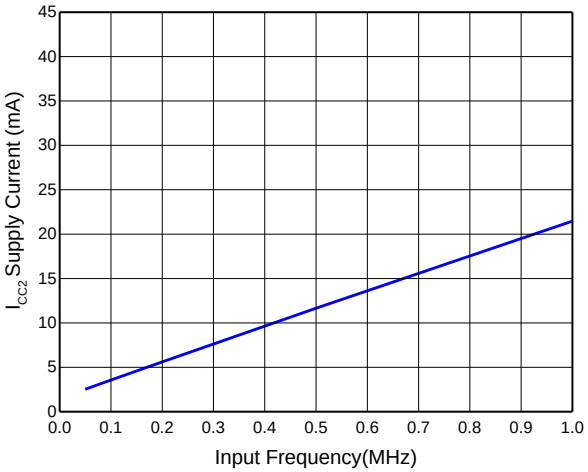


Figure 19. I_{CC2} Supply Current vs Input Frequency

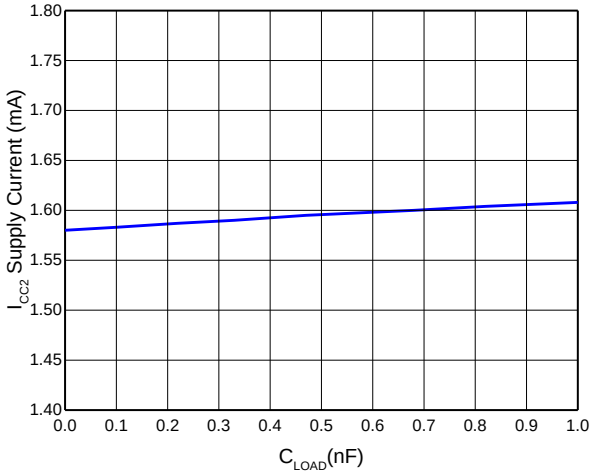


Figure 20. I_{CC2} Supply Current vs Load Capacitance (f_{SW}=1kHz)

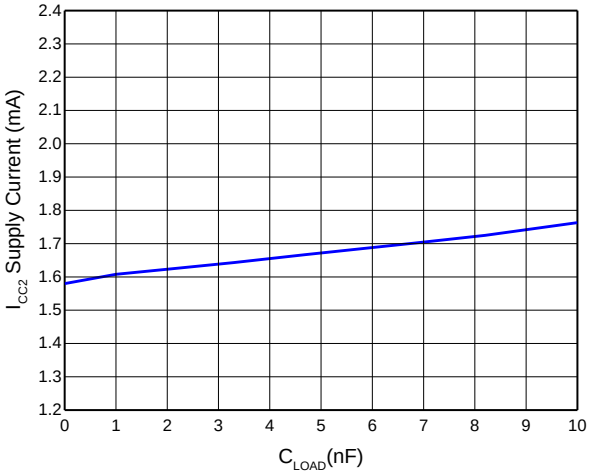


Figure 21. I_{CC2} Supply Current vs Load Capacitance (f_{SW}=1kHz)

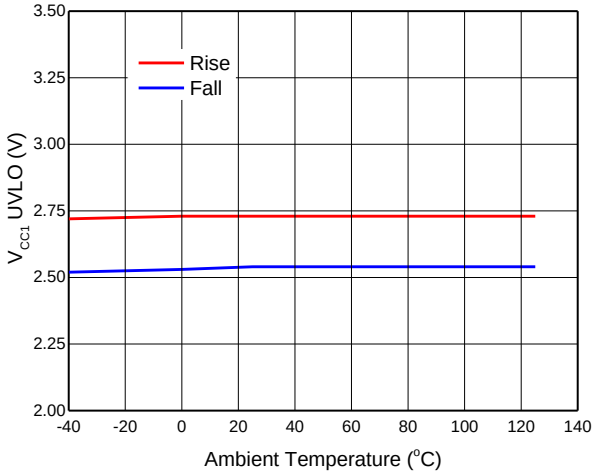


Figure 22. V_{CC1} UVLO vs Temperature

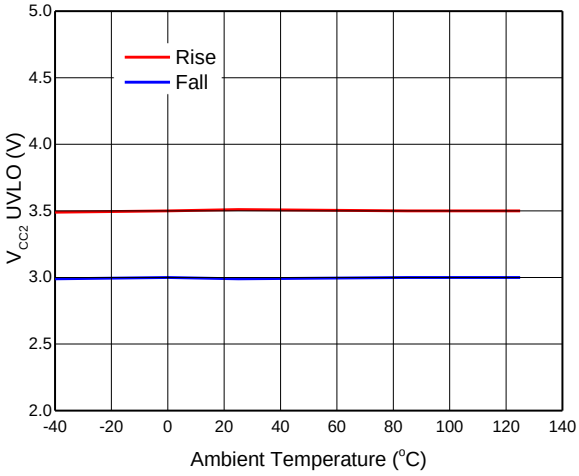


Figure 23. V_{CC2} UVLO vs Temperature (UVLO=3.5V)

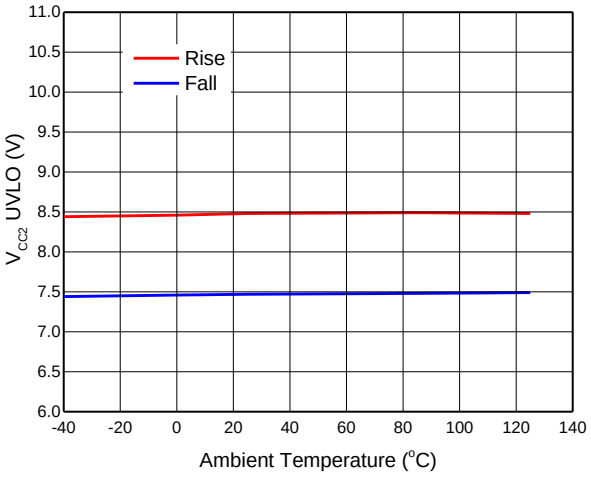


Figure 24. V_{CC2} UVLO vs Temperature (UVLO=8.5V)

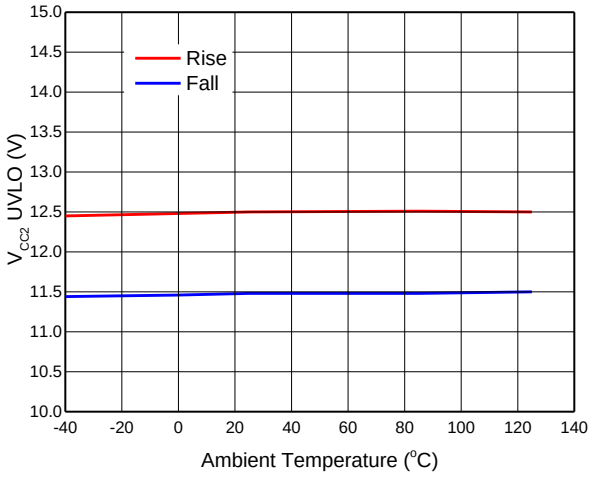


Figure 25. V_{CC2} UVLO vs Temperature (UVLO=12.5V)

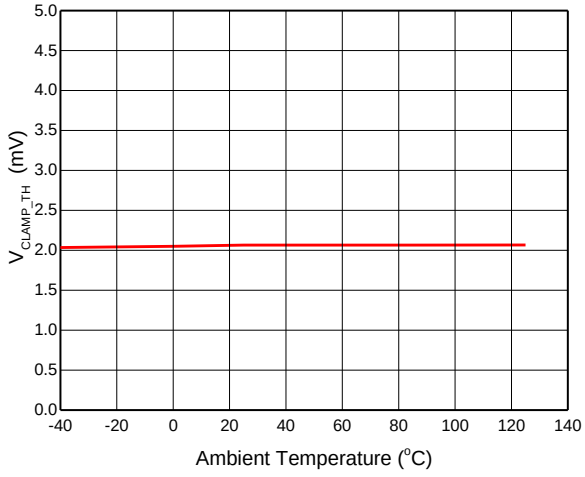


Figure 26. V_{CLAMP_TH} vs Temperature

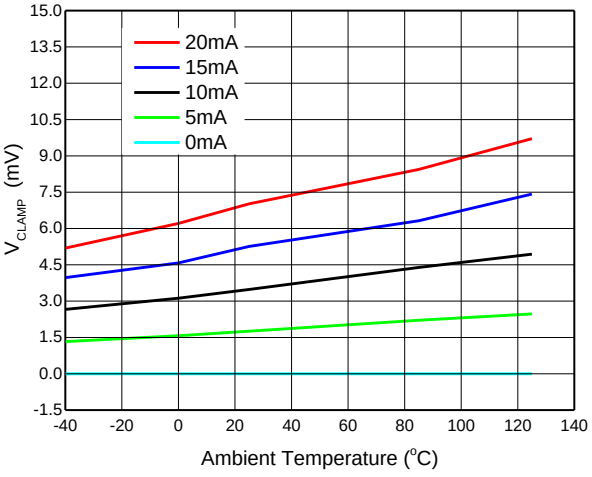


Figure 27. V_{CLAMP} vs Temperature (I_{CLAMP}=0~20mA)

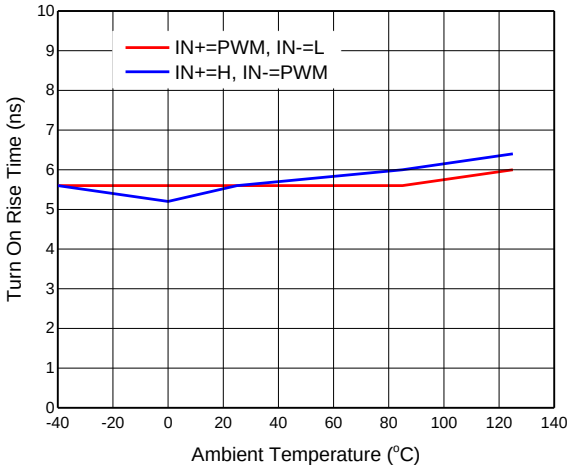


Figure 28. Rise Time vs Temperature

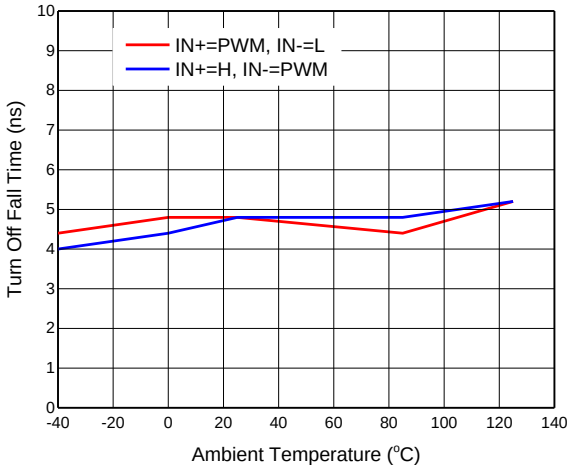


Figure 29. Fall Time vs Temperature

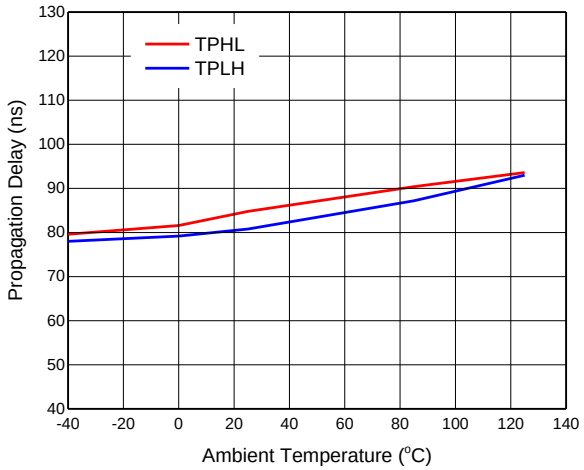


Figure 30. Propagation Delay vs Temperature

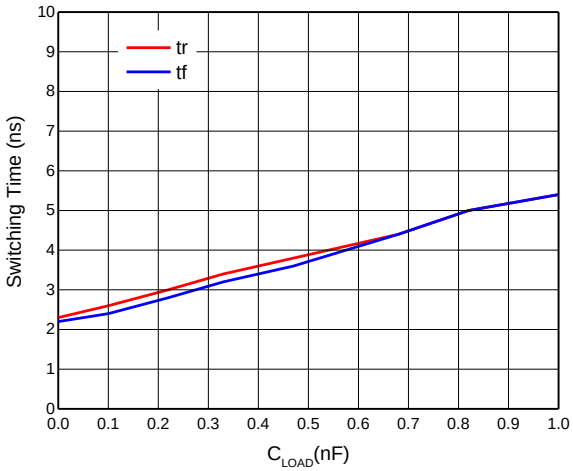


Figure 31. Switching Time vs Load Capacitance

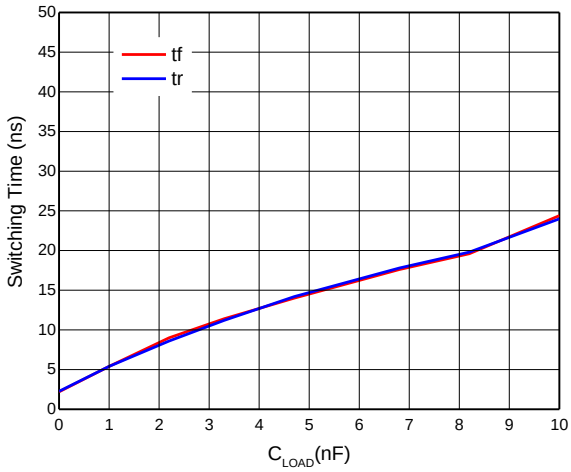


Figure 32. Switching Time vs Load Capacitance

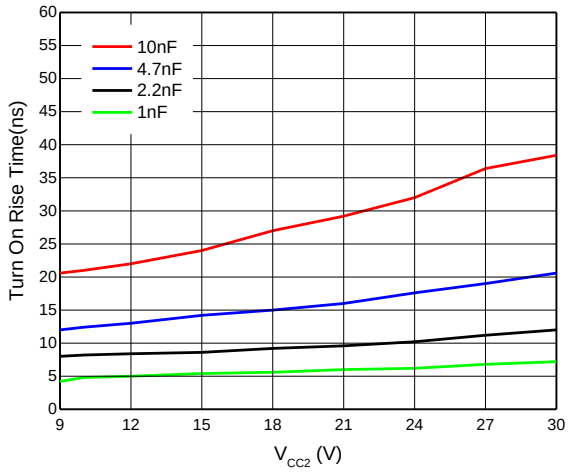


Figure 33. Rise Time vs C_{LOAD} and V_{CC2}

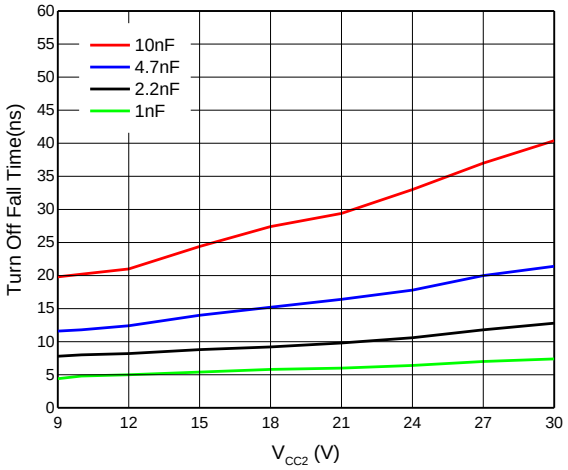


Figure 34. Fall Time vs C_{LOAD} and V_{CC2}

FEATURE DESCRIPTION

The SiLM5350-AQ family of isolated gate drivers has two variations: SiLM5350S/R/H-AQ has split output and SiLM5350M/F/P-AQ has internal clamp to prevent false turn-on caused by miller current. The isolation inside the SiLM5350-AQ family is implemented with high voltage SiO_2 based capacitors. It also incorporates advanced circuit techniques to maximize the CMTI performance.

Power Supply

The VCC1 input power supply supports a wide voltage range from 3 V to 18 V and the VCC2 driver supply supports a voltage up to 30V.

For operation with bipolar supplies, as shown in Figure 11, the power device is turned off with a negative voltage on the gate with respect to the emitter or source. This configuration prevents the power device from false turn on because of current induced from the Miller effect.

Under Voltage Lockout (UVLO)

The SiLM5350-AQ has under voltage lock out (UVLO) protection feature on driver power supply voltage, VCC2. When the VCC2 voltage is lower than $V_{UVLO\_VCC2\_R}$, during device start up or lower than $V_{UVLO\_VCC2\_F}$, after start up, the VCC2 UVLO feature holds the driver output low, regardless of the status of the input pins. A hysteresis on the VCC2 UVLO feature prevents glitch when there is noise from the power supply.

The SiLM5350-AQ also monitors the input power supply and there is an internal under voltage lock out protection feature on the VCC1. The driver outputs (OUTL or OUT) are hold low when the voltage on the VCC1 is lower than $V_{UVLO\_VCC1\_R}$ during start up or lower than $V_{UVLO\_VCC1\_F}$ after start up. There is a hysteresis on the VCC1 UVLO feature to prevent glitch due the noise on the VCC1 power supply.

Input Stage

The SiLM5350-AQ has two input signals, IN+ and IN-, to control the output. The Table 7 shows the relationship between the input signals and output assuming the voltage on the VCC1 and VCC2 are in the recommended range.

Table 7. SiLM5350-AQ Pin Description

IN+	IN-	OUTH	OUTL	OUT
Low	X	Hi-Z	Low	Low
X	High	Hi-Z	Low	Low
High	Low	High	High-Z	High

Output Stage

The output stage in the SiLM5350-AQ is capable of supplying 10A peak source and 10A peak sink current pulses. The output voltage swings between VCC2 and VEE2 providing rail-to-rail operation, thanks to the MOS-output stage which delivers very low drop-out.

Active Output Pulldown

The active output pulldown feature ensures that the OUT(L) is clamped to approximately 1.7V higher than VEE2 to ensure safe IGBT off-state during VCC2 is open.

Internal Active Miller Clamp

A Miller clamp circuit integrates in the SiLM5350M/F/P-AQ which allows the control of the Miller current during a high dV/dt situation and can eliminate the use of a negative supply voltage in most of the applications. During turn off, the gate voltage is monitored through the CLAMP and the clamp circuit is activated when the voltage on the CLAMP pin goes below the clamp voltage threshold (2V typical, relative to VEE2). A clamp low sink current is generated when the clamp circuit is activated. The clamp circuit is disabled when the input on signal is triggered again.

APPLICATION INFORMATION

Typical Application Circuit

The circuit in Figure 35 and Figure 36 show the typical application circuit for SiLM5350S/R/H-AQ and SiLM5350M/F/P-AQ.

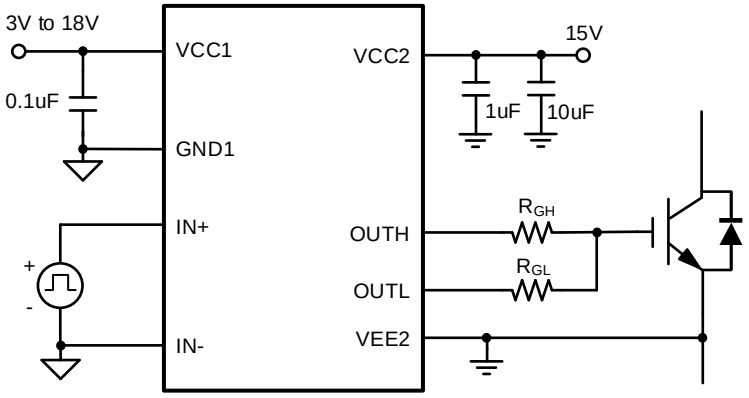


Figure 35. SiLM5350S/R/H-AQ Typical Application Circuit

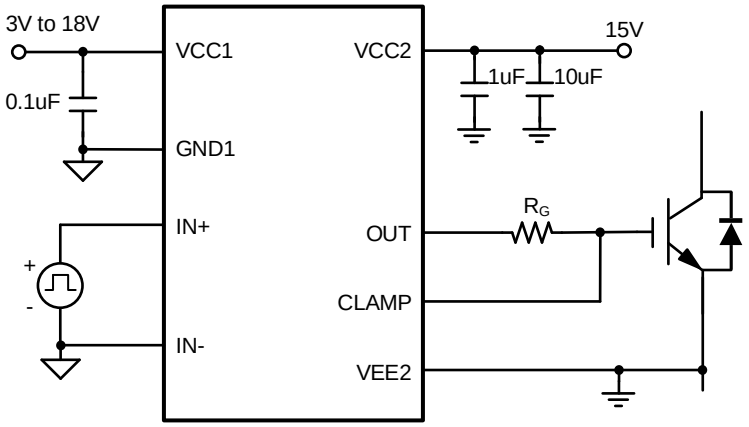


Figure 36. SiLM5350M/F/P-AQ Typical Application Circuit

Layout

In order to achieve optimum performance for the SiLM5350-AQ, some suggestions on PCB layout.

Component placement:

- Low ESR and low ESL capacitors must be connected close to the device between the VCC2 and VEE2 pins to bypass noise and to support high peak currents when turning on the external power transistor.
- To avoid large negative transients on the VEE2 pins connected to the switch node, the parasitic inductances between the source of the top transistor and the source of the bottom transistor must be minimized.

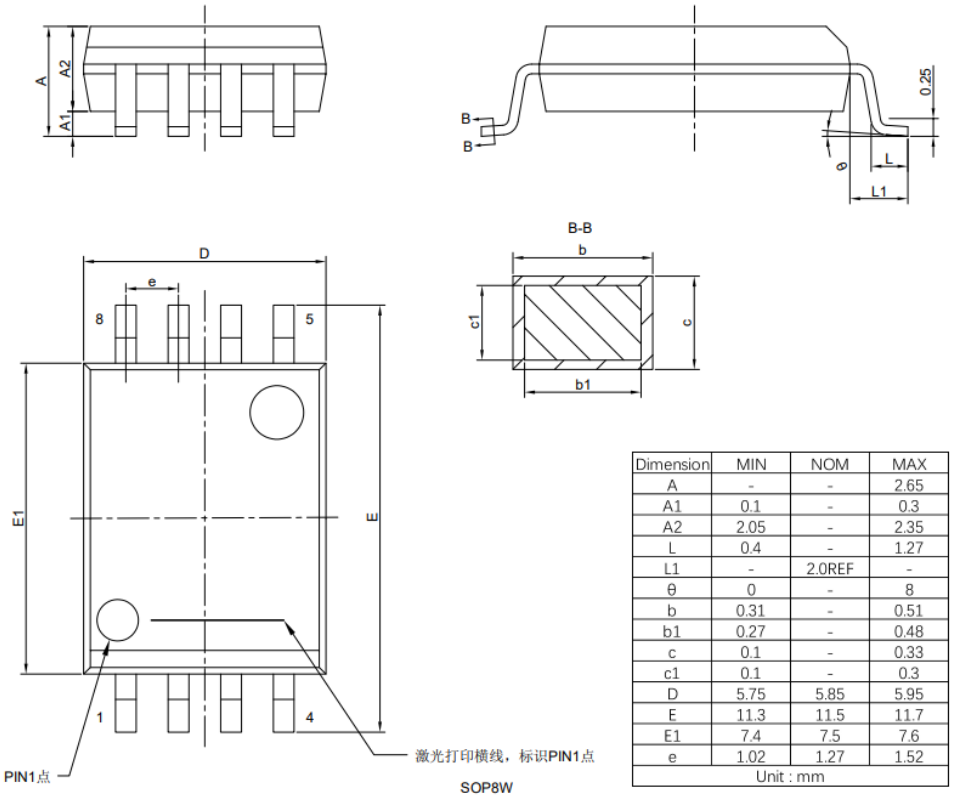
Grounding considerations:

- Limiting the high peak currents that charge and discharge the transistor gates to a minimal physical area is essential. This limitation decreases the loop inductance and minimizes noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.

High-voltage considerations:

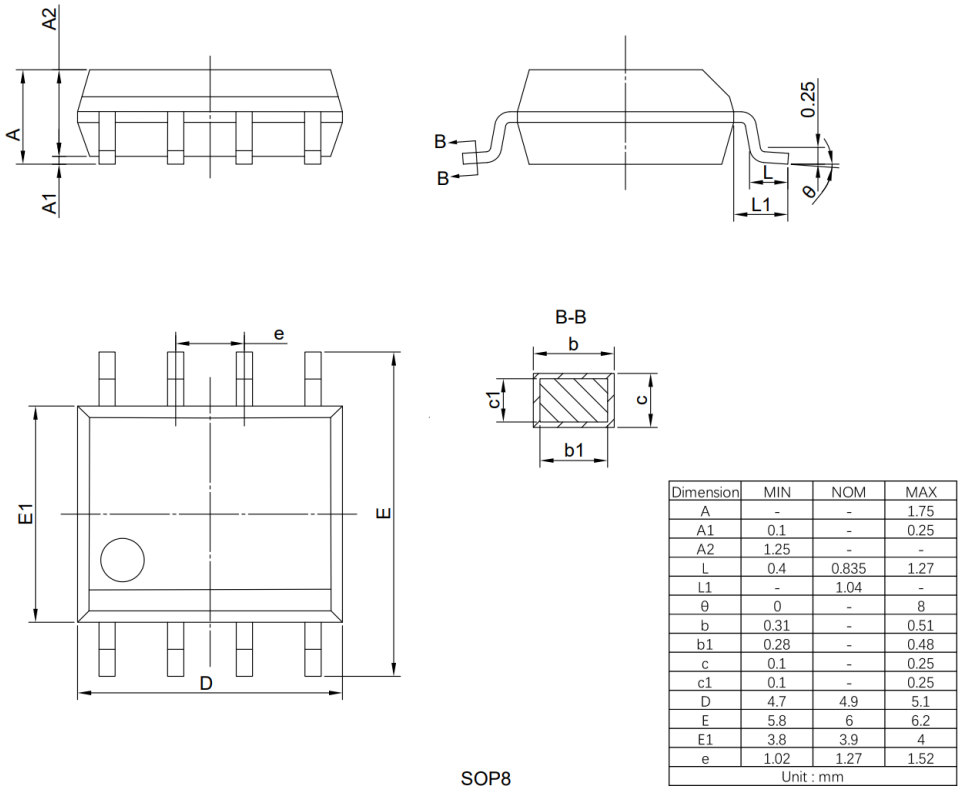
- To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the driver device. A PCB cutout or groove is recommended in order to prevent contamination that may compromise the isolation performance.

PACKAGE CASE OULTLINES



Dimension	MIN	NOM	MAX
A	-	-	2.65
A1	0.1	-	0.3
A2	2.05	-	2.35
L	0.4	-	1.27
L1	-	2.0REF	-
θ	0	-	8
b	0.31	-	0.51
b1	0.27	-	0.48
c	0.1	-	0.33
c1	0.1	-	0.3
D	5.75	5.85	5.95
E	11.3	11.5	11.7
E1	7.4	7.5	7.6
e	1.02	1.27	1.52
Unit : mm			

Figure 37. SOP8W Package Outline Dimensions



Dimension	MIN	NOM	MAX
A	-	-	1.75
A1	0.1	-	0.25
A2	1.25	-	-
L	0.4	0.835	1.27
L1	-	1.04	-
θ	0	-	8
b	0.31	-	0.51
b1	0.28	-	0.48
c	0.1	-	0.25
c1	0.1	-	0.25
D	4.7	4.9	5.1
E	5.8	6	6.2
E1	3.8	3.9	4
e	1.02	1.27	1.52
Unit : mm			

Figure 38. SOP8 Package Outline Dimensions

REVISION HISTORY

Note: page numbers for previous revisions may differ from page numbers in current version.

Page or Item	Subjects (major changes since previous revision)
Rev 1.0 datasheet: 2023-05-10	
Whole document	Initial datasheet release
Rev 1.1 datasheet: 2024-10-11	
Page 15	Update t_{PLH}, t_{PHL}, t_{PWD} and t_{PDD} in Switching Characteristics (AC) table