High Speed Dual Channel Digital Isolator

GENERAL DESCRIPTION

The SiLM572x devices are high performance, dual channel digital isolator with 5.0 kV_{RMS} (SOP8W) and 3 kV_{RMS} (SOP8) isolation rating per UL1577. The SiLM572x devices provide high electromagnetic immunity and low emissions at low power consumption.

The SiLM5720 device has both channels in the same direction while the SiLM5721 device has both channels in the opposite direction. In the event of input power or signal loss, the default output is high for devices without suffix F and low for devices with suffix F.

APPLICATION

- Isolated line receiver
- Microprocessor system interface
- Digital isolation for A/D, D/A conversion
- PLC, ATE input/output isolation
- Power transistor isolation in motor drives
- Isolation of high-speed logic systems

FEATURES

- Data rate 100Mbps
- Propagation delay 12ns (Typ)
- CMTI 150kV/us (Min)
- Low power consumption: 1.5mA/Channel (Typ)
- Wide supply voltage: 2.25V to 5.5V
- 2.25V to 5.5V level translation
- Default output High (SiLM572x) and Low (SiLM572xF) Options
- Robust electromagnetic compatibility (EMC)
  - System Level ESD, EFT, and surge immunity
  - ±8 kV IEC 61000-4-2 contact discharge protection across isolation barrier
  - Low emissions
- Operation temperature: –40°C to +125°C
- Safety certifications:
  - 3kV_{RMS} isolation for 1 minute per UL 1577 for SOP8 package
  - 5.0kV_{RMS} isolation for 1 minute per UL 1577 for SOP8W package
  - CQC certification per GB4943.1-2022
  - DIN VDE 0884-17: 2021-10 (Pending)

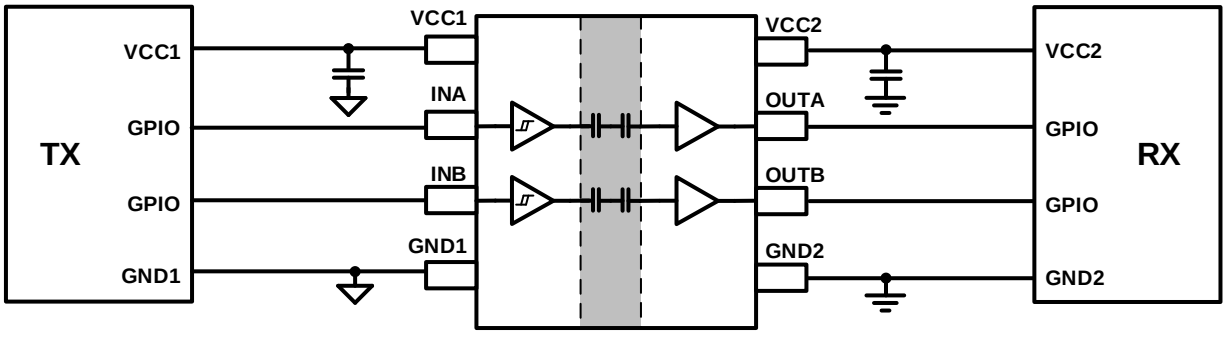

Figure 1. SiLM5720 Typical Application Circuit

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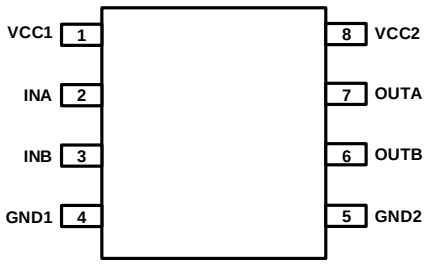
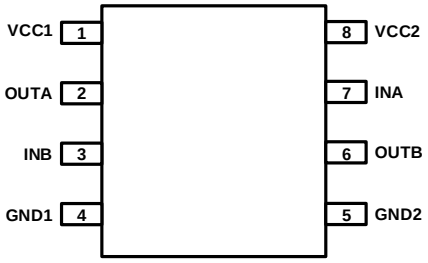
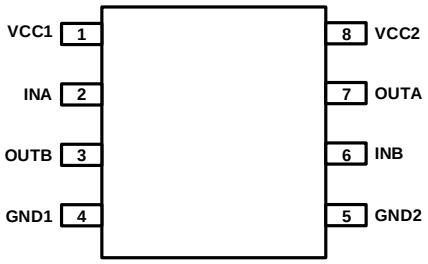
PIN CONFIGURATION

Part Name	Pin Configuration (Top View)
	SOP8/SOP8W
SiLM5720	
SiLM5721	
SiLM5722	

PIN DESCRIPTION

Table 1. SiLM5720 SOP8/SOP8W Pin Description

No.	Pin Name	Description
1	VCC1	Input power supply
2	INA	Channel A input
3	INB	Channel B input
4	GND1	Input power ground
5	GND2	Output power ground
6	OUTB	Channel B output
7	OUTA	Channel A output
8	VCC2	Output power supply

Table 2. SiLM5721 SOIC8/SOP8W Pin Description

No.	Pin Name	Description
1	VCC1	Input power supply
2	OUTA	Channel A output
3	INB	Channel B input
4	GND1	Input power ground
5	GND2	Output power ground
6	OUTB	Channel B output
7	INA	Channel A input
8	VCC2	Output power supply

Table 3. SiLM5722 SOIC8/SOP8W Pin Description

No.	Pin Name	Description
1	VCC1	Input power supply
2	INA	Channel A input
3	OUTB	Channel B output
4	GND1	Input power ground
5	GND2	Output power ground
6	INB	Channel B input
7	OUTA	Channel A output
8	VCC2	Output power supply

FUNCTIONAL BLOCK DIAGRAM

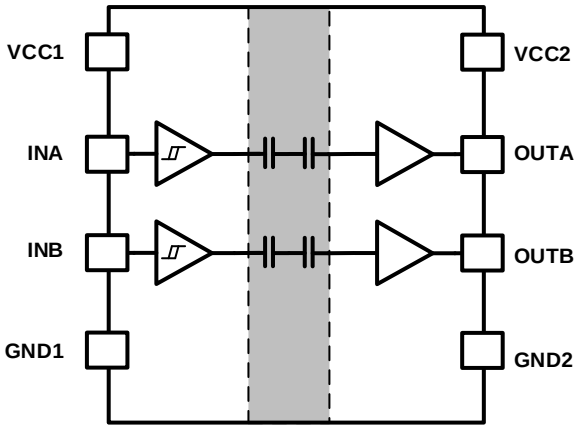


Figure 2. SiLM5720 Functional Block

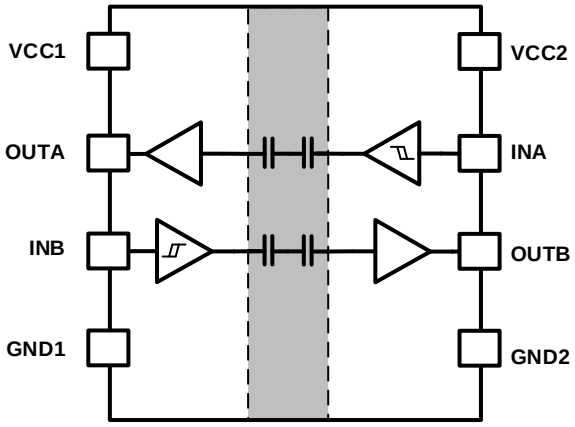


Figure 3. SiLM5721 Functional Block

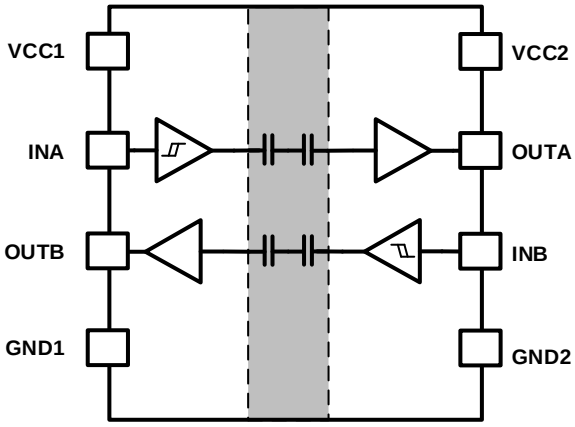


Figure 4. SiLM5722 Functional Block

ORDERING INFORMATION

Order Part No.	Package	QTY
SiLM5720CA-DG	SOP8, Pb-Free	2500/Reel
SiLM5720CM-DG	SOP8W, Pb-Free	1000/Reel
SiLM5720FCA-DG	SOP8, Pb-Free	2500/Reel
SiLM5720FCM-DG	SOP8W, Pb-Free	1000/Reel
SiLM5721CA-DG	SOP8, Pb-Free	2500/Reel
SiLM5721CM-DG	SOP8W, Pb-Free	1000/Reel
SiLM5721FCA-DG	SOP8, Pb-Free	2500/Reel
SiLM5721FCM-DG	SOP8W, Pb-Free	1000/Reel
SiLM5722CA-DG	SOP8, Pb-Free	2500/Reel
SiLM5722CM-DG	SOP8W, Pb-Free	1000/Reel
SiLM5722FCA-DG	SOP8, Pb-Free	2500/Reel
SiLM5722FCM-DG	SOP8W, Pb-Free	1000/Reel

ABSOLUTE MAXIMUM RATINGS

Symbol	Definition	Min.	Max.	Units
V_{CC1}, V_{CC2}	Supply voltage, VCC1 and VCC2	-0.3	6	V
V_I	Voltage at Inx, referenced to input side ground	-0.3	V_{CC}+0.3	V
V_{OUT}	Voltage at OUTx, reference to output side ground	-0.3	V_{CC}+0.3	V
I_O	Output Current	-15	15	mA
T_J	Junction temperature	-55	150	°C
T_S	Storage temperature	-65	150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the Recommended Operation Conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. All voltage parameters are referenced to local ground terminal, GND1 or GND2.

RECOMMENDED OPERATION CONDITIONS

Symbol	Definition	Min.	Max.	Units
V_{CC1}, V_{CC2}	Supply voltage	2.25	5.5	V
I_{OH}	High level output current @ V_{CCO}(1)=5V	-4		mA
	High level output current @ V_{CCO}=3.3V	-2		mA
	High level output current @ V_{CCO}=2.5V	-1		mA
I_{OL}	Low level output current @ V_{CCO}=5V		4	mA
	Low level output current @ V_{CCO}=3.3V		2	mA
	Low level output current @ V_{CCO}=2.5V		1	mA
V_{IH}	High Level Input Voltage	0.7× V_{CCI}	V_{CCI}(1)	V
V_{IL}	Low Level Input Voltage	0	0.3× V_{CCI}	V
DR	Data Rate	0	100	Mbps
T_J	Junction temperature	-40	150	°C
T_A	Ambient temperature	-40	125	°C

(1) V_{CCI} =Input side V_{CC}, V_{CCO}=Output side V_{CC}

ESD RATINGS

Symbol	Definition	Value	Units
V_{ESD}	HBM	±8000	V
	CDM	±2000	V

THERMAL INFORMATION

Symbol	Definition	Value		Unit
		SOP8	SOP8W	
$R_{\theta JA}$	Junction to ambient thermal resistance	135.3	84.5	°C/W
$R_{\theta JC}$	Junction to case (top) thermal resistance	48	43	°C/W

PACKAGE SPECIFICATIONS

Symbol	Definition	Min.	Typ.	Max.	Units
R_{IO}	Resistance (Input Side to Output Side)		10^{12}		Ω
C_{IO}	Capacitance (Input Side to Output Side)		0.95		pF

INSULATION SPECIFICATIONS

Symbol	Definition	Test Condition	Value		Units
			SOP8	SOP8W	
CLR	External clearance	Shortest terminal to terminal distance through air	>4.0	>8.0	mm
CPG	External creepage	Shortest terminal to terminal distance across the package surface	>4.0	>8.0	mm
DTI	Distance through the insulation	Minimum internal gap	>16	>16	um
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11), IEC 60112	>600	>600	V
	Material Group		I		
	Overvoltage category	Rated mains voltage ≤150V_{RMS}	I-IV	I-IV	
		Rated mains voltage ≤300 V_{RMS}	I-III	I-IV	
		Rated mains voltage ≤600 V_{RMS}	I-II	I-III	
		Rated mains voltage ≤1000 V_{RMS}	I-I	I-II	
DIN VDE 0884-17(1)					
V_{IORM}	Maximum repetitive peak isolation voltage		1000	1414	V_{PK}
V_{IOWM}	Maximum isolation working voltage		707	1000	V_{RMS}
V_{IOTM}	Maximum transient isolation voltage	60s	4242	7000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage	Test method per IEC62368, 1.2/50us waveform, V_{TEST}=1.3xV_{IOSM} for SOP8, V_{TEST}=1.6 x V_{IOSM} for SOP8W	6000	6250	V_{PK}
q_{pd}	Apparent charge		≤5	≤5	pC
	Climatic Category		40/125/21	40/125/21	
	Pollution Degree		2	2	

Symbol	Definition	Test Condition	Value		Units
			SOP8	SOP8W	
UL1577					
V_{ISO}	Withstand Isolation Voltage	$V_{TEST}=V_{ISO}$, t=60s (qualification), $V_{TEST}=1.2 \times V_{ISO}$, t=1s (100% production)	3000	5000	V_{RMS}

Note1: Certification pending

SAFETY RELATED CERTIFICATIONS (SOP8)

VDE	UL	CQC
DIN VDE 0884-17: 2021-10	UL 1577 component recognition program	Certified according to GB4943.1-2022
Basic Insulation, V_{IORM} = 1000 V_{PK} V_{IOTM} = 4242 V_{PK}	Single protection, 3000 V_{RMS}	Basic insulation, Altitude≤ 5000m
Certification Pending	File number: E521801	File number: CQC23001373092

SAFETY LIMITING VALUES (SOP8)

Symbol	Parameter	Condition	Value	Unit
I_S	Safety input, output, or supply current	$R_{\theta JA}$=135.3°C/W, VCC1=VCC2=5.5V, T_J=150°C, T_A=25°C	168	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$=135.3°C/W, T_J=150°C, T_A=25°C	924	mW
T_S	Maximum safety temperature		150	°C

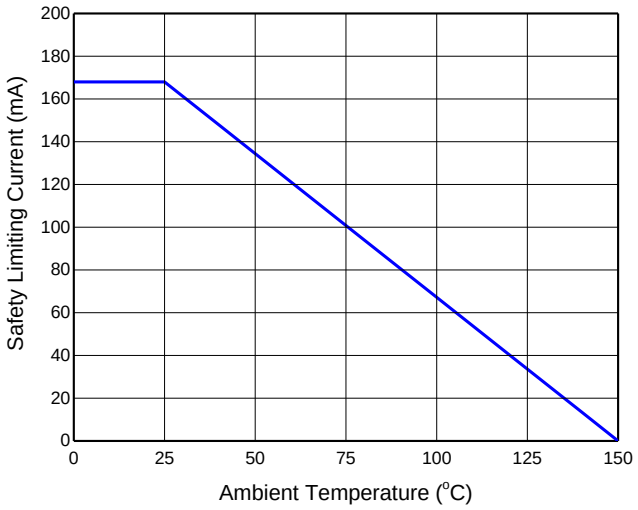


Figure 5. Thermal Derating Curve for Limiting Current per VDE (SOP8)

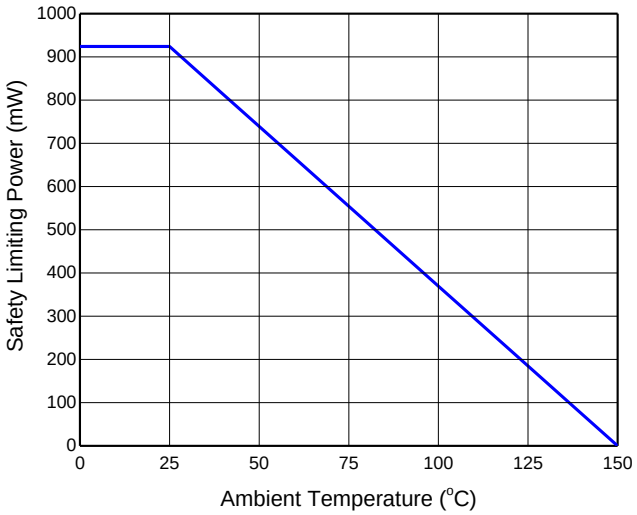


Figure 6. Thermal Derating Curve for Limiting Power per VDE (SOP8)

SAFETY RELATED CERTIFICATIONS (SOP8W)

VDE	UL	CQC
DIN VDE 0884-17: 2021-10	UL 1577 component recognition program	Certified according to GB4943.1-2022
Reinforced insulation, V_{IORM} = 1500 V_{PK} V_{IOTM} = 7000 V_{PK}	Single protection, 5000 V_{RMS}	Reinforced insulation, Altitude≤ 5000m
Certification Pending	File number: E521801	File number: CQC23001376521

SAFETY LIMITING VALUES (SOP8W)

Symbol	Parameter	Condition	Value	Unit
I_S	Safety input, output, or supply current	$R_{\theta JA}$=84.5°C/W, VCC1=VCC2=5.5V, T_J=150°C, T_A=25°C	269	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$=84.5°C/W, T_J=150°C, T_A=25°C	1480	mW
T_S	Maximum safety temperature		150	°C

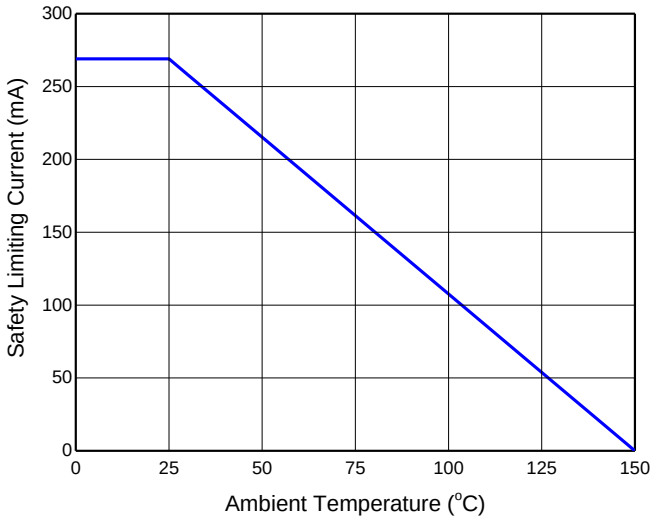


Figure 7. Thermal Derating Curve for Limiting Current per VDE (SOP8W)

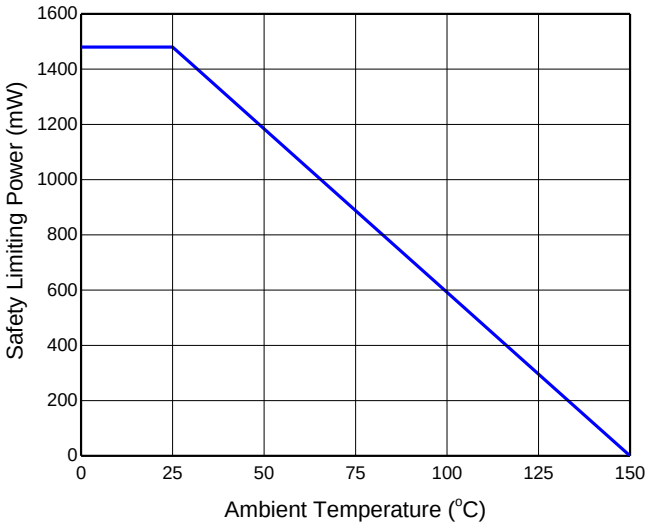


Figure 8. Thermal Derating Curve for Limiting Power per VDE (SOP8W)

ELECTRICAL CHARACTERISTICS (DC) WITH 5V SUPPLY

V_{CC1} = V_{CC2}=5V±10% (over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ.	Max.	Unit
Power Supply UVLO						
$UVLO_R$	Under Voltage Lockout V_{CCx} rising			2.05	2.25	V
$UVLO_F$	Under Voltage Lockout V_{CCx} falling		1.7	1.9		V
$UVLO_{HYS}$	Under Voltage Lockout Hysteresis			0.15		V
Power Supply Current (SiLM5720)						
I_{CC1_QH}	Current on VCC1 with DC Signal	V_I = V_{CCI} (SiLM5720), V_I = 0 V (SiLM5720F)		0.4	0.6	mA
I_{CC1_QL}		V_I = 0 V (SiLM5720), V_I = V_{CCI} (SiLM5720F)		2.8	4.1	mA
I_{CC2_QH}	Current on VCC2 with DC Signal	V_I = V_{CCI} (SiLM5720), V_I = 0 V (SiLM5720F)		1.4	2.0	mA
I_{CC2_QL}		V_I = 0 V (SiLM5720), V_I = V_{CCI} (SiLM5720F)		1.5	2.2	mA
$I_{CC1\_OP\_1M}$	Current on VCC1 with AC Signal. All channel switching with square wave clock input	1 Mbps, C_L = 15pF		1.6	2.3	mA
$I_{CC1\_OP\_10M}$		10 Mbps, C_L = 15pF		1.6	2.4	mA
$I_{CC1\_OP\_100M}$		100 Mbps, C_L = 15pF		2.1	2.9	mA
$I_{CC2\_OP\_1M}$	Current on VCC2 with AC Signal. All channel switching with square wave clock input	1 Mbps, C_L = 15pF		1.7	2.3	mA
$I_{CC2\_OP\_10M}$		10 Mbps, C_L = 15pF		3.6	4.9	mA
$I_{CC2\_OP\_100M}$		100 Mbps, C_L = 15pF		15.9	22	mA
Power Supply Current (SiLM5721/2)						
I_{CC1_QH}	Current on VCC1 with DC Signal	V_I = V_{CCI} (SiLM5721/2), V_I = 0 V (SiLM5721/2F)		0.9	1.3	mA
I_{CC1_QL}		V_I = 0 V (SiLM5721/2), V_I = V_{CCI} (SiLM5721/2F)		2.1	3.1	mA
I_{CC2_QH}	Current on VCC2 with DC Signal	V_I = V_{CCI} (SiLM5721/2), V_I = 0 V (SiLM5721/2F)		0.9	1.3	mA
I_{CC2_QL}		V_I = 0 V (SiLM5721/2), V_I = V_{CCI} (SiLM5721/2F)		2.2	3.1	mA
$I_{CC1\_OP\_1M}$	Current on VCC1 with AC Signal. All channel switching with square wave clock input	1 Mbps, C_L = 15pF		1.6	2.3	mA

Symbol	Parameter	Condition	Min	Typ.	Max.	Unit
$I_{CC1\_OP\_10M}$	Current on VCC1 with AC Signal. All channel switching with square wave clock input	10 Mbps, C_L = 15pF		2.7	3.7	mA
$I_{CC1\_OP\_100M}$		100 Mbps, C_L = 15pF		8.8	12	mA
$I_{CC2\_OP\_1M}$	Current on VCC2 with AC Signal. All channel switching with square wave clock input	1 Mbps, C_L = 15pF		1.6	2.3	mA
$I_{CC2\_OP\_10M}$		10 Mbps, C_L = 15pF		2.7	3.7	mA
$I_{CC2\_OP\_100M}$		100 Mbps, C_L = 15pF		8.8	12	mA
Input Logic Interface						
V_{IH}	Rising input threshold voltage			0.6× V_{CCI}	0.7× V_{CCI}	V
V_{IL}	Falling input threshold voltage		0.3× V_{CCI}	0.4× V_{CCI}		V
V_{IHYS}	Input threshold voltage hysteresis			0.2× V_{CCI}		V
I_{IH}	High level input current	INx = V_{CCI}			15	uA
I_{IL}	Low level input current	Inx = 0V	-15			uA
Output Logic Interface						
V_{OH}	High level output voltage	I_{OH} = -4mA	V_{CCO} -0.4	4.8		V
V_{OL}	Low level output voltage	I_{OL} = 4mA		0.12	0.3	V
CMTI						
$CMTI_H$	Output High Level Common Mode Transient Immunity	V_I = V_{CCI}, V_{CM}=1200V, C_L=15pF	150	200		kV/us
$CMTI_L$	Output Low Level Common Mode Transient Immunity	V_I = 0V, V_{CM}=1200V, C_L=15pF	150	200		kV/us

SWITCHING CHARACTERISTICS (AC) WITH 5V SUPPLY

V_{CC1} = V_{CC2}=5V±10% (over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{PLH}	Propagation delay, Low to High	C_L=15pF		12	20	ns
t_{PHL}	Propagation delay, High to Low	C_L=15pF		12	20	ns
t_r	Turn on rise time	C_L=15pF		2		ns

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_f	Turn off fall time	C_L=15pF		2		ns
t_{PWD}	Pulse Width Distortion	C_L=15pF			10	ns
t_{SKO}	Channel to Channel Output Skew Time	C_L=15pF, same direction in single device			8	ns
t_{SKP}	Part to Part Skew Time	C_L=15pF, same direction			8	ns
t_{DO}	Default output delay time from input power loss	Measured from the time that the input voltage goes below 1.7V, C_L = 15pF		40		ns

ELECTRICAL CHARACTERISTICS (DC) WITH 3.3V SUPPLY

V_{CC1} = V_{CC2}=3.3V±10% (over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ.	Max.	Unit
Power Supply UVLO						
$UVLO_R$	Under Voltage Lockout V_{CCx} rising			2.05	2.25	V
$UVLO_F$	Under Voltage Lockout V_{CCx} falling		1.7	1.9		V
$UVLO_{HYS}$	Under Voltage Lockout Hysteresis			0.15		V
Power Supply Current (SiLM5720)						
I_{CC1_QH}	Current on VCC1 with DC Signal	V_I = V_{CCI} (SiLM5720), V_I = 0 V (SiLM5720F)		0.4	0.6	mA
I_{CC1_QL}		V_I = 0 V (SiLM5720), V_I = V_{CCI} (SiLM5720F)		2.8	4.0	mA
I_{CC2_QH}	Current on VCC2 with DC Signal	V_I = V_{CCI} (SiLM5720), V_I = 0 V (SiLM5720F)		1.3	2.0	mA
I_{CC2_QL}		V_I = 0 V (SiLM5720), V_I = V_{CCI} (SiLM5720F)		1.5	2.1	mA
$I_{CC1\_OP\_1M}$	Current on VCC1 with AC Signal. All channel switching with square wave clock input	1 Mbps, C_L = 15pF		1.6	2.3	mA
$I_{CC1\_OP\_10M}$		10 Mbps, C_L = 15pF		1.6	2.3	mA
$I_{CC1\_OP\_100M}$		100 Mbps, C_L = 15pF		2.0	2.7	mA
$I_{CC2\_OP\_1M}$	Current on VCC2 with AC Signal. All channel switching with square wave clock input	1 Mbps, C_L = 15pF		1.5	2.2	mA
$I_{CC2\_OP\_10M}$		10 Mbps, C_L = 15pF		2.3	3.3	mA
$I_{CC2\_OP\_100M}$		100 Mbps, C_L = 15pF		10.2	13.7	mA
Power Supply Current (SiLM5721/2)						
I_{CC1_QH}	Current on VCC1 with DC Signal	V_I = V_{CCI} (SiLM5721/2), V_I = 0 V (SiLM5721/2F)		0.9	1.3	mA
I_{CC1_QL}		V_I = 0 V (SiLM5721/2), V_I = V_{CCI} (SiLM5721/2F)		2.1	3.0	mA
I_{CC2_QH}	Current on VCC2 with DC Signal	V_I = V_{CCI} (SiLM5721/2), V_I = 0 V (SiLM5721/2F)		0.9	1.3	mA
I_{CC2_QL}		V_I = 0 V (SiLM5721/2), V_I = V_{CCI} (SiLM5721/2F)		2.1	3.0	mA
$I_{CC1\_OP\_1M}$	Current on VCC1 with AC Signal. All channel switching with square wave clock input	1 Mbps, C_L = 15pF		1.5	2.2	mA

Symbol	Parameter	Condition	Min	Typ.	Max.	Unit
$I_{CC1\_OP\_10M}$	Current on VCC1 with AC Signal. All channel switching with square wave clock input	10 Mbps, C_L = 15pF		2.0	2.8	mA
$I_{CC1\_OP\_100M}$		100 Mbps, C_L = 15pF		5.8	7.8	mA
$I_{CC2\_OP\_1M}$	Current on VCC2 with AC Signal. All channel switching with square wave clock input	1 Mbps, C_L = 15pF		1.5	2.2	mA
$I_{CC2\_OP\_10M}$		10 Mbps, C_L = 15pF		2.0	2.8	mA
$I_{CC2\_OP\_100M}$		100 Mbps, C_L = 15pF		5.8	7.8	mA
Input Logic Interface						
V_{IH}	Rising input threshold voltage			0.6× V_{CCI}	0.7× V_{CCI}	V
V_{IL}	Falling input threshold voltage		0.3× V_{CCI}	0.4× V_{CCI}		V
V_{IHYS}	Input threshold voltage hysteresis			0.2× V_{CCI}		V
I_{IH}	High level input current	INx = V_{CCI}			12	uA
I_{IL}	Low level input current	Inx = 0V	-12			uA
Output Logic Interface						
V_{OH}	High level output voltage	I_{OH} = -2mA	V_{CCO} -0.3	3.2		V
V_{OL}	Low level output voltage	I_{OL} = 2mA		0.07	0.2	V
CMTI						
$CMTI_H$	Output High Level Common Mode Transient Immunity	V_I = V_{CCI}, V_{CM}=1200V, C_L=15pF	150	200		kV/us
$CMTI_L$	Output Low Level Common Mode Transient Immunity	V_I = 0V, V_{CM}=1200V, C_L=15pF	150	200		kV/us

SWITCHING CHARACTERISTICS (AC) WITH 3.3V SUPPLY

V_{CC1} = V_{CC2}=3.3V±10% (over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{PLH}	Propagation delay, Low to High	C_L=15pF		12	25	ns
t_{PHL}	Propagation delay, High to Low	C_L=15pF		12	25	ns
t_r	Turn on rise time	C_L=15pF		2		ns

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_f	Turn off fall time	C_L=15pF		2		ns
t_{PWD}	Pulse Width Distortion	C_L=15pF			10	ns
t_{SKO}	Channel to Channel Output Skew Time	C_L=15pF, same direction in single device			8	ns
t_{SKP}	Part to Part Skew Time	C_L=15pF, same direction			8	ns
t_{DO}	Default output delay time from input power loss	Measured from the time that the input voltage goes below 1.7V, C_L = 15pF		40		ns

ELECTRICAL CHARACTERISTICS (DC) WITH 2.5V SUPPLY

V_{CC1} = V_{CC2}=2.5V±10% (over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ.	Max.	Unit
Power Supply UVLO						
$UVLO_R$	Under Voltage Lockout V_{CCx} rising			2.05	2.25	V
$UVLO_F$	Under Voltage Lockout V_{CCx} falling		1.7	1.9		V
$UVLO_{HYS}$	Under Voltage Lockout Hysteresis			0.15		V
Power Supply Current (SiLM5720)						
I_{CC1_QH}	Current on VCC1 with DC Signal	V_I = V_{CCI} (SiLM5720), V_I = 0 V (SiLM5720F)		0.4	0.6	mA
I_{CC1_QL}		V_I = 0 V (SiLM5720), V_I = V_{CCI} (SiLM5720F)		2.8	3.9	mA
I_{CC2_QH}	Current on VCC2 with DC Signal	V_I = V_{CCI} (SiLM5720), V_I = 0 V (SiLM5720F)		1.3	1.9	mA
I_{CC2_QL}		V_I = 0 V (SiLM5720), V_I = V_{CCI} (SiLM5720F)		1.5	2.1	mA
$I_{CC1\_OP\_1M}$	Current on VCC1 with AC Signal. All channel switching with square wave clock input	1 Mbps, C_L = 15pF		1.6	2.2	mA
$I_{CC1\_OP\_10M}$		10 Mbps, C_L = 15pF		1.6	2.3	mA
$I_{CC1\_OP\_100M}$		100 Mbps, C_L = 15pF		2.1	2.7	mA
$I_{CC2\_OP\_1M}$	Current on VCC2 with AC Signal. All channel switching with square wave clock input	1 Mbps, C_L = 15pF		1.5	2.1	mA
$I_{CC2\_OP\_10M}$		10 Mbps, C_L = 15pF		2.1	3	mA
$I_{CC2\_OP\_100M}$		100 Mbps, C_L = 15pF		8.1	10.8	mA
Power Supply Current (SiLM5721/2)						
I_{CC1_QH}	Current on VCC1 with DC Signal	V_I = V_{CCI} (SiLM5721/2), V_I = 0 V (SiLM5721/2F)		0.9	1.3	mA
I_{CC1_QL}		V_I = 0 V (SiLM5721/2), V_I = V_{CCI} (SiLM5721/2F)		2.1	3.0	mA
I_{CC2_QH}	Current on VCC2 with DC Signal	V_I = V_{CCI} (SiLM5721/2), V_I = 0 V (SiLM5721/2F)		0.9	1.3	mA
I_{CC2_QL}		V_I = 0 V (SiLM5721/2), V_I = V_{CCI} (SiLM5721/2F)		2.1	3.0	mA
$I_{CC1\_OP\_1M}$	Current on VCC1 with AC Signal. All channel switching with square wave clock input	1 Mbps, C_L = 15pF		1.5	2.1	mA

Symbol	Parameter	Condition	Min	Typ.	Max.	Unit
$I_{CC1\_OP\_10M}$	Current on VCC1 with AC Signal. All channel switching with square wave clock input	10 Mbps, C_L = 15pF		1.8	2.6	mA
$I_{CC1\_OP\_100M}$		100 Mbps, C_L = 15pF		4.7	6.2	mA
$I_{CC2\_OP\_1M}$	Current on VCC2 with AC Signal. All channel switching with square wave clock input	1 Mbps, C_L = 15pF		1.5	2.1	mA
$I_{CC2\_OP\_10M}$		10 Mbps, C_L = 15pF		1.8	2.6	mA
$I_{CC2\_OP\_100M}$		100 Mbps, C_L = 15pF		4.7	6.2	mA
Input Logic Interface						
V_{IH}	Rising input threshold voltage			0.6× V_{CCI}	0.7× V_{CCI}	V
V_{IL}	Falling input threshold voltage		0.3× V_{CCI}	0.4× V_{CCI}		V
V_{IHYS}	Input threshold voltage hysteresis			0.2× V_{CCI}		V
I_{IH}	High level input current	INx = V_{CCI}			10	uA
I_{IL}	Low level input current	Inx = 0V	-10			uA
Output Logic Interface						
V_{OH}	High level output voltage	I_{OH} = -1mA	V_{CCO} -0.2	2.45		V
V_{OL}	Low level output voltage	I_{OL} = 1mA		0.04	0.1	V
CMTI						
$CMTI_H$	Output High Level Common Mode Transient Immunity	V_I = V_{CCI}, V_{CM}=1200V, C_L=15pF	150	200		kV/us
$CMTI_L$	Output Low Level Common Mode Transient Immunity	V_I = 0V, V_{CM}=1200V, C_L=15pF	150	200		kV/us

SWITCHING CHARACTERISTICS (AC) WITH 2.5V SUPPLY

V_{CC1} = V_{CC2}=2.5V±10% (over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{PLH}	Propagation delay, Low to High	C_L=15pF		14	27	ns
t_{PHL}	Propagation delay, High to Low	C_L=15pF		14	27	ns
t_r	Turn on rise time	C_L=15pF		2		ns

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_f	Turn off fall time	C_L=15pF		2		ns
t_{PWD}	Pulse Width Distortion	C_L=15pF			10	ns
t_{SKO}	Channel to Channel Output Skew Time	C_L=15pF, same direction in single device			8	ns
t_{SKP}	Part to Part Skew Time	C_L=15pF, same direction			8	ns
t_{DO}	Default output delay time from input power loss	Measured from the time that the input voltage goes below 1.7V, C_L = 15pF		40		ns

PARAMETER MEASUREMENT INFORMATION

Switching Characteristics Test Timing

Figure 9 shows the timing of propagation delay, rise and fall time

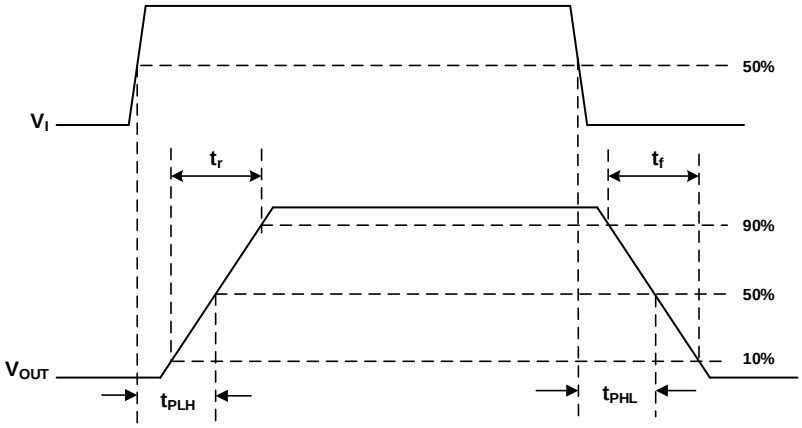


Figure 9. Propagation Delay, Rise Time and Fall Time

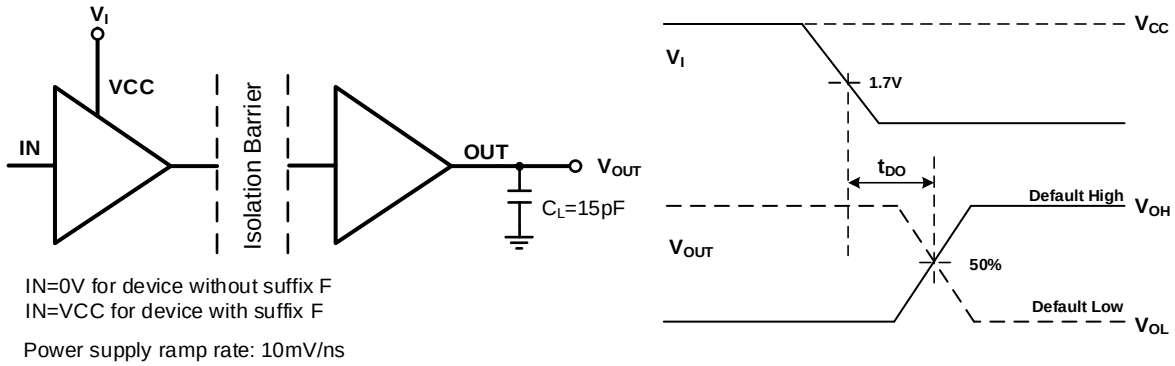


Figure 10. Default Output Delay Time Test

CMTI Testing

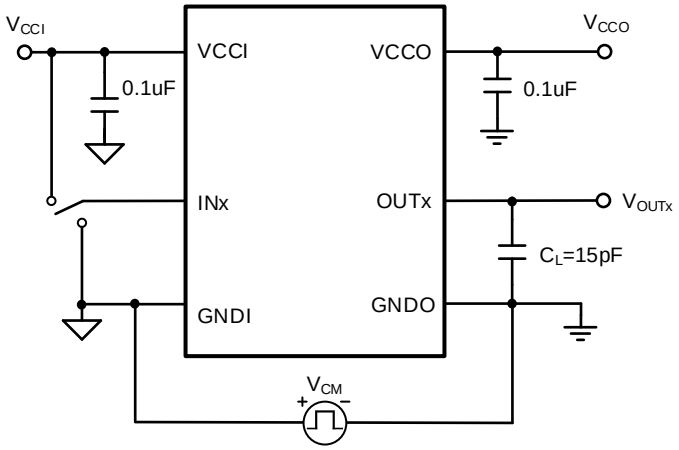


Figure 11. CMTI Test Configuration

FEATURE DESCRIPTION

The SiLM572x devices are high-performance, dual-channel digital isolators with default output state options to enable a variety of application uses. The supply voltage range is from 2.25 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. With innovative chip design and layout techniques, the electromagnetic compatibility of the SiLM572x devices has been significantly enhanced to improve the robustness of overall system.

Device Functional Modes

The Table 4 shows the functional modes of the SiLM572x.

Table 4. Function Table

V_{CCI} (1)	V_{CCO}(1)	Input (Inx)	Output (OUTx)	Function Description
PU(2)	PU	H	H	Normal operation. The output is controlled by the input
		L	L	
		Open	Default	Default mode. When Inx is open, the corresponding output goes to the default logic. The default is high for SiLM572x and low for SiLM572xF.
PD(2)	PU	X	Default	Default mode. When VCCI is unpowered, channel output based on the default option. The default is high for SiLM572x and low for SiLM572xF.
X	PD	X	Undetermined(3)	When VCCO is unpowered, channel output is undermined.

(1) V_{CCI} =Input side V_{CC}, V_{CCO}=Output side V_{CC}.

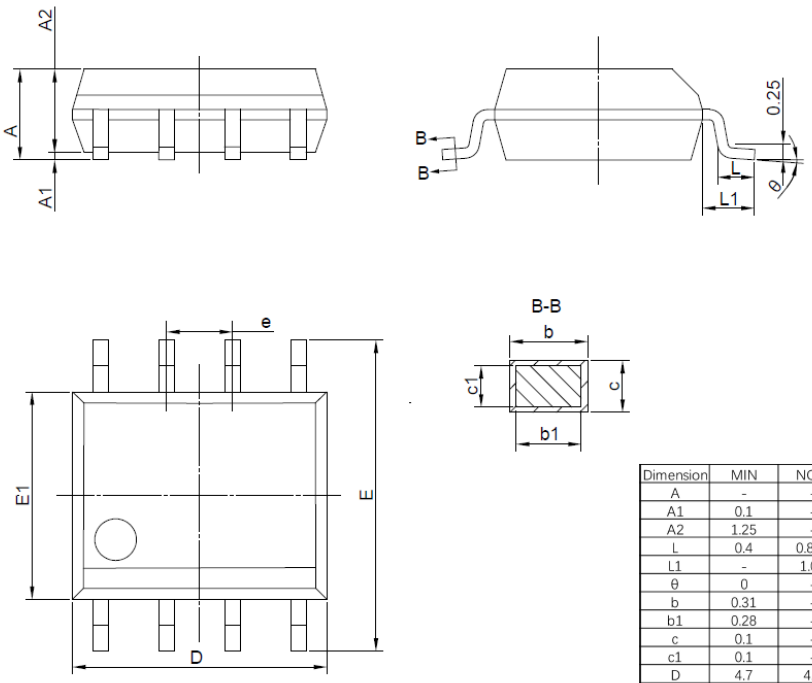
(2) PU=Powered up, $V_{CC} \geqslant 2.25V$; PD=Powered down, $V_{CC} \leqslant 1.7V$

(3) The outputs are in undermined state when $1.7 < V_{CCI}$, $V_{CCO} < 2.25V$

Power Supply Recommendation

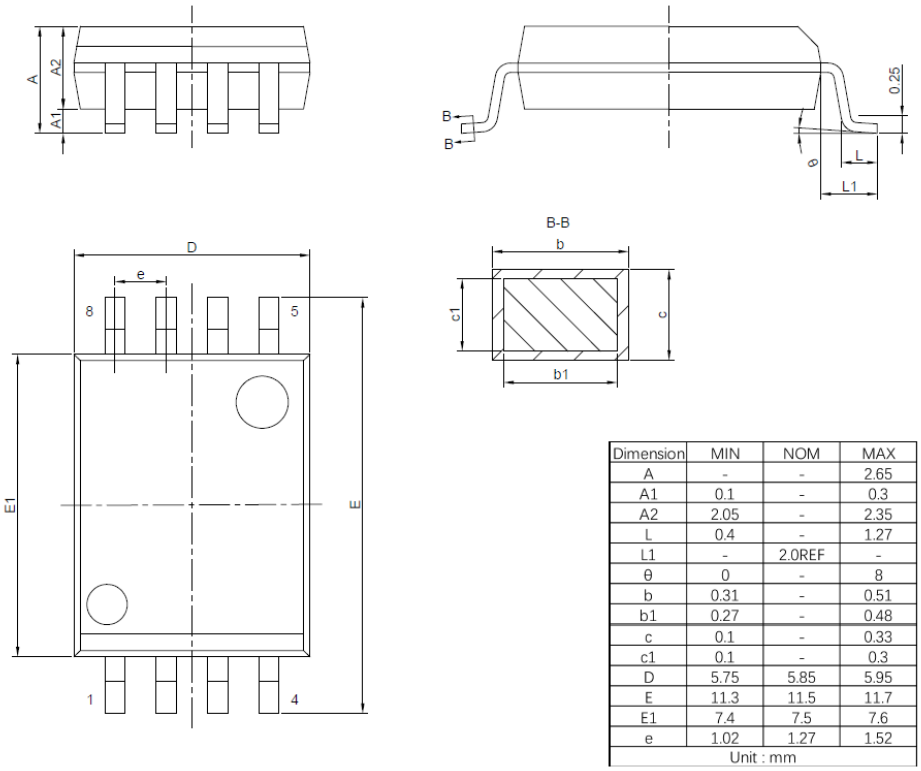
A 0.1μF bypass capacitor is recommended at the input and output supply pins (V_{CC1} and V_{CC2}) to help ensure reliable operation. The capacitors should be placed as close to the supply pins as possible.

PACKAGE CASE OUTLINES



Dimension	MIN	NOM	MAX
A	-	-	1.75
A1	0.1	-	0.25
A2	1.25	-	-
L	0.4	0.835	1.27
L1	-	1.04	-
θ	0	-	8
b	0.31	-	0.51
b1	0.28	-	0.48
c	0.1	-	0.25
c1	0.1	-	0.25
D	4.7	4.9	5.1
E	5.8	6	6.2
E1	3.8	3.9	4
e	1.02	1.27	1.52
Unit : mm			

Figure 12. SOP8 Package Outline Dimensions



Dimension	MIN	NOM	MAX
A	-	-	2.65
A1	0.1	-	0.3
A2	2.05	-	2.35
L	0.4	-	1.27
L1	-	2.0REF	-
θ	0	-	8
b	0.31	-	0.51
b1	0.27	-	0.48
c	0.1	-	0.33
c1	0.1	-	0.3
D	5.75	5.85	5.95
E	11.3	11.5	11.7
E1	7.4	7.5	7.6
e	1.02	1.27	1.52
Unit : mm			

Figure 13. SOP8W Package Outline Dimensions

REVISION HISTORY

Note: page numbers for previous revisions may differ from page numbers in current version

Page or Item	Subjects (major changes since previous revision)
Rev 1.0 datasheet: 2023-05-30	
Whole document	Initial datasheet release