PLC Receiver for Photovoltaic Array Rapid Shutdown

GENERAL DESCRIPTION

The SiLM6000 is an integrated power line communication (PLC) receiver that is designed for photovoltaic array rapid shutdown. With the integrated NFET driver, the SiLM6000 provides a simple system design that complies with the requirements of the National Electric Code for photovoltaic module level shutdown.

When the PLC receiver detects a system generated keep alive signal on the DC power line, the gate driver controls an external switch to connect the PV module to the string. In the absence of the keep alive signal, the gate drive turns off the external switch and allows the PV module to be disconnected from the string. The SiLM6000 additionally provides a 1V, 10mA regulated output that can be applied to the PV array during shutdown which compliance with the SunSpec™ Alliance specification.

The SiLM6000 operates with input voltage from 10.5V to 110V and supports junction temperature between -40℃ to 125℃.

FEATURES

- Receiver supports SunSpec™ Alliance “Communication Signal for Rapid Shutdown” power line communication protocol
- Provides 1V output voltage during system keep alive signal is absent
- Operates with PV voltage from 10.5V to 110V
- Integrated NFET driver
- Support flash test
- TSSOP14-EP package
- Junction temperature range: -40℃ to 125℃

APPLICATION

- Photovoltaic Rapid Shutdown
- PLC Communication Module (RX only)

TYPICAL APPLICATION CIRCUIT

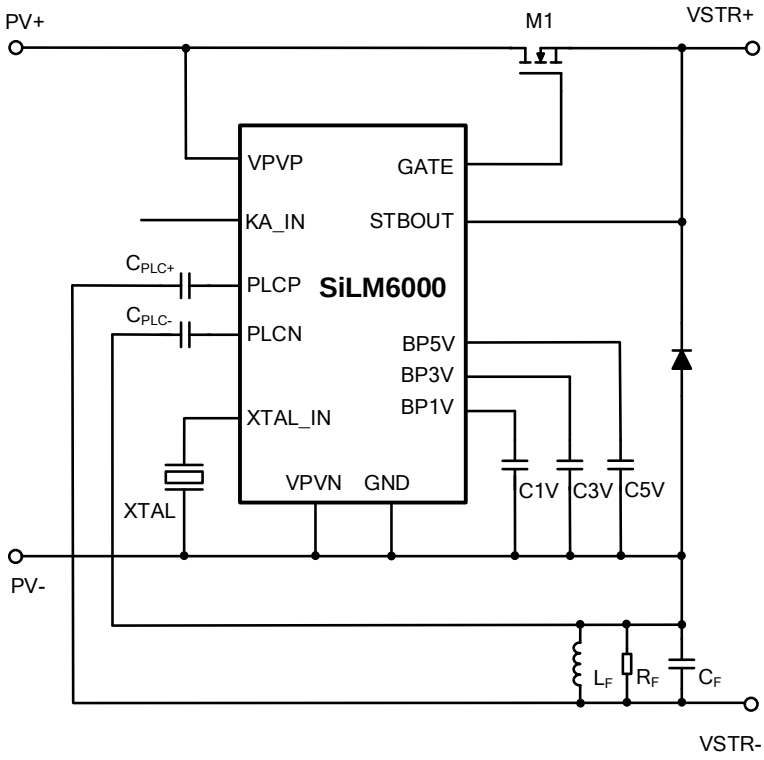

Figure 1. Typical Application Circuit

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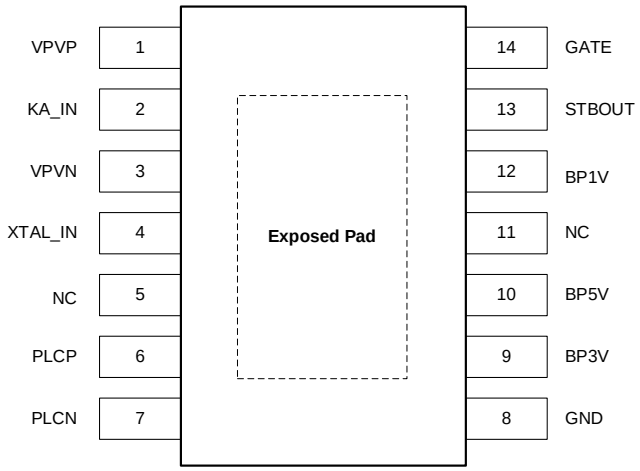
PIN CONFIGURATION

Package	Pin Configuration (Top View)
TSSOP14-EP	

PIN DESCRIPTION

Pin Number	Pin Name	Description
1	VPVP	PV positive input.
2	KA_IN	Input for force keep-alive
3	VPVN	PV negative input
4	XTAL_IN	Input for the crystal oscillator.
5	NC	No connection
6	PLCP	Line coupling input for power line communication
7	PLCN	Line coupling input for power line communication.
8	GND	IC ground.
9	BP3V	3.3V regulator output. Connect a 1uF capacitor between this pin and ground.
10	BP5V	5.0V regulator output. Connect a 1uF capacitor between this pin and ground. This BP5V also support external power supply to power the IC. The external voltage should be between 5.1V to 5.5V.
11	NC	No connection
12	BP1V	1.0V regulator output. Connect a 1uF capacitor between this pin and ground.
13	STBOUT	Output for shutdown mode. This pin should connect to the source of the external NFET.
14	GATE	Output driver for external NFET. During keep-alive mode, the GATE turn on an external NFET. While in shutdown mode, the GATE turn off an external NFET.
EPAD	Exposed Pad	The exposed pad should be soldered to an external ground plane underneath the IC for thermal dissipation.

FUNCTIONAL BLOCK DIAGRAM

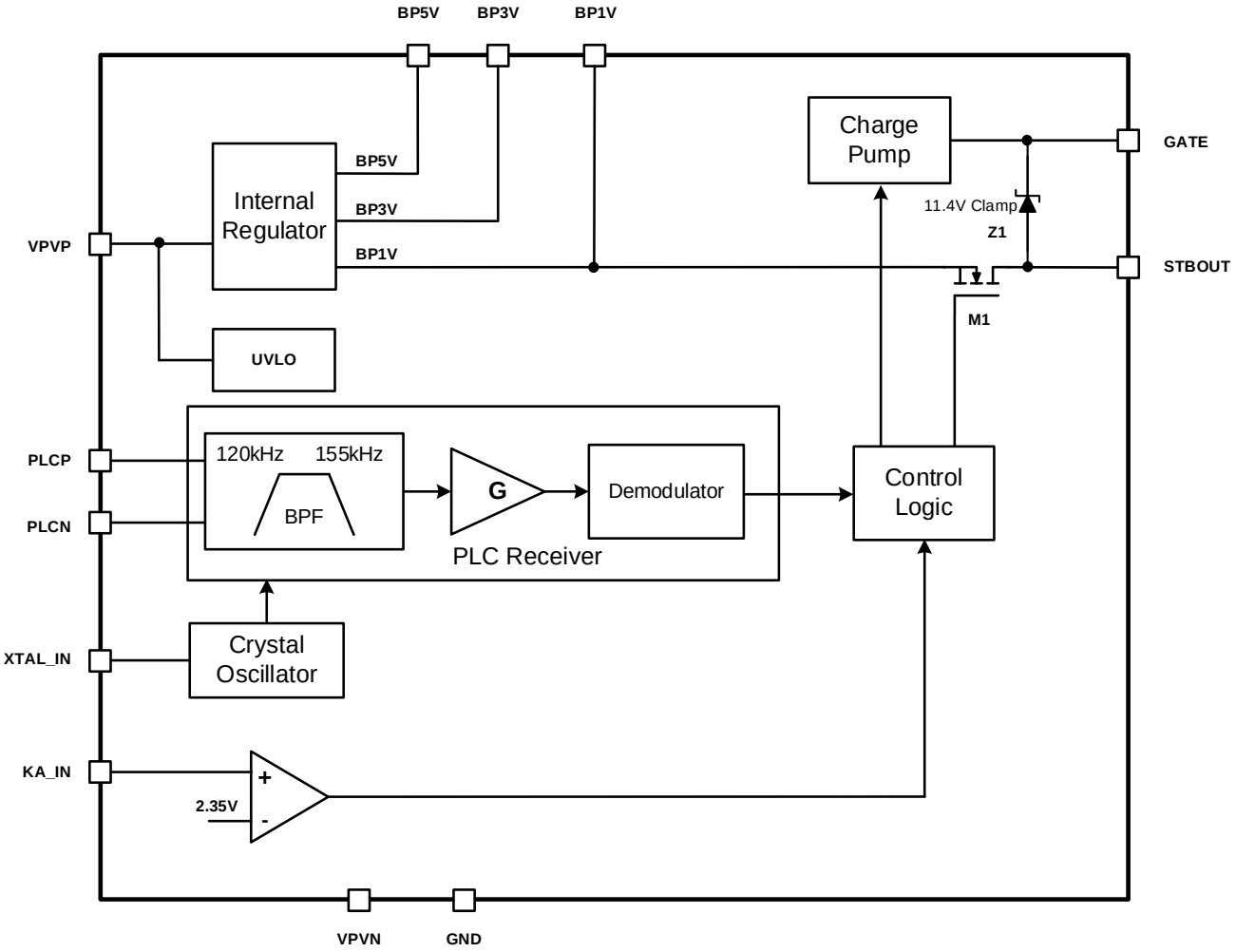


Figure 2. Function Block Diagram

ABSOLUTE MAXIMUM RATINGS

All parameters are specified with T_J= -40℃ to 125℃; all voltages are with respect to VPVN (unless otherwise noted)

Symbol	Definition	Min	Max	Unit
V_{PVP}	Voltage on VPVP	-0.3	120	V
V_{STBOUT}	Voltage on STBOUT	-0.3	120	V
V_{GATE}	Voltage on the GATE	-0.3	V_{STBOUT}+16	V
V_{KA_IN}	Voltage on KA_IN	-0.3	120	V
V_{BP1V}	Voltage on BP1V	-0.3	6	V
V_{BP3V}	Voltage on BP3V	-0.3	6	V
V_{BP5V}	Voltage on BP5V	-0.3	6	V
V_{PLCP}	PLCP voltage with respect to VPVN	-0.3	6	V
V_{PLCN}	PLCN voltage with respect to VPVN	-0.3	6	V
V_{GND}	Voltage at GND pin respect to VPVN	-0.3	0.3	V
T_J	Operating junction temperature	-40	125	℃
T_{STG}	Storage temperature	-65	150	℃
Lead temperature	Soldering, 10 sec.	300		℃
	Reflow	260		℃

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATION CONDITIONS

over operating free-air temperature range (unless otherwise noted)

Symbol	Definition	Min	Max	Unit
V_{PVP}	Voltage on the VPVP pin	10.5	110	V
V_{PLCP}, V_{PLCN}	Power line communication coupling input	1.2	142	mVrms

THERMAL INFORMATION

Symbol	Definition	Value	Unit
R_{thJC}	Junction to Case(1)	17	℃/W
R_{thJA}	Junction to Ambient(1)	67	℃/W

(1) Device mounted on the JESD51-3 standard board. 3 inch x 3 inch with 2oz. copper traces on the bottom of the board.

ESD RATINGS

		Value	Unit
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY
SiLM6000MF-DG	TSSOP14-EP	5000/Reel

ELECTRICAL CHARACTERISTICS

All parameters are specified within T_J = -40°C to 125°C, 10.5V ≤V_{PVP}≤110V, unless otherwise specified.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage (VPVP Pin)						
Voltage range on VPVP	V_{PVP}		10.5		110	V
VPVP Under-Voltage Lockout Threshold	$V_{PVP\_UVLO\_R}$	VPVP rising	8.55	9.5	10.45	V
	$V_{PVP\_UVLO\_F}$	VPVP falling	6.75	7.5	8.25	V
Quiescent current on VPVP	I_Q	KA_IN high, or keep alive signal received	6	7.4	9.1	mA
Shutdown current on VPVP	I_{SHDN}	KA_IN low and no keep alive signal	6	7.4	9.3	mA
Internal Regulator (BP5V, BP3V and BP1V Pin)						
Voltage on BP5V	V_{BP5V}		4.8	5	5.2	V
Current limit on BP5V	I_{LMIT_BP5V}		60	84	120	mA
Output short fold-back threshold	$V_{SC\_TH\_}$		2.3	2.7	3.3	V
Voltage on BP3V	V_{BP3V}		3.23	3.3	3.37	V
Current limit on BP3V	I_{LMIT_BP3V}		12	16	21	mA
Voltage on BP1V	V_{BP1V}		0.9	1.05	1.2	V
Current limit on BP1V	I_{LMIT_BP1V}		20	30	40	mA
Power Line Communication Receiver (PLCP and PLCN Pin)						
PLC modulation		Spread frequency shift keying	S-FSK			
Mark frequency	f_M	Accuracy +/- 0.01%	131.24	131.25	131.26	kHz
Space frequency	f_S	Accuracy +/- 0.01%	143.74	143.75	143.76	kHz
Bit period	T_S		5.1195	5.12	5.1205	ms
Logic 1 code word	W1	+1=mark, -1=space	{-1, -1, -1, +1, +1, +1, -1, +1, +1, -1, +1}			
Logic 0 code word	W0	+1=mark, -1=space	{+1, +1, +1, -1, -1, -1, +1, -1, -1, +1, -1}			
Zero energy word	ZE	0=zero energy	{0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0}			
Cyclical transmission		A, B, C are W0 or W1; Z is Zero energy word	{A, B, C, Z, Z, Z, Z, Z, Z, Z, Z, Z, Z, Z, Z, Z, Z, Z, Z}			
PLCP/PLCN input current		V_{PLCP}, V_{PLCN}=2.85V		128	148	μA
RX input voltage maximum	V_{RX_MAX}		142			mVrms
RX input voltage minimum sensitivity	V_{RX_SENSE}				1.2	mVrms

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Receiver band lower bound			120			kHz
Receiver band upper bound					155	kHz
KEEP Alive (KA_IN Pin)						
KA_IN input current			3	4	5	μA
KA_IN high threshold	$V_{KA\_IN\_H}$			2.3		V
KA_IN low threshold	$V_{KA\_IN\_L}$			1.35		V
KA_IN threshold hysteresis	$V_{KA\_IN\_HYS}$			0.95		V
Gate Driver (GATE Pin)						
GATE pin output high voltage	ΔV_{GATE}	V_{GATE}-V_{STBOUT}, VPVP>10V	10	11.6	14	V
GATE pin pull-up current	I_{GATE_UP}	ΔV_{GATE}=0V	72	103		μA
GATE pin pull-down current	I_{GATE_DW}	ΔV_{GATE}=10V	0.8	1		mA
KA_IN to GATE high propagation delay	$t_{GATE\_DLY\_H}$			3.4		μs
KA_IN to GATE low propagation delay	$t_{GATE\_DLY\_L}$			3.8		μs
Flash test time	t_{FLASH}	Default		0		ms
		Option 1	9.6	16	22.4	ms
		Option 2	19.2	32	44.8	ms
		Option 3	38.4	64	89.6	ms
		Option 4	76.8	128	179.2	ms
		Option 5	153.6	256	358.4	ms
		Option 6	307.2	512	716.8	ms
		Option 7	614.4	1024	1433.6	ms
Crystal Oscillator (XTAL_IN Pin)						
Jitter					500	ps
Crystal oscillator frequency				12		MHZ
External quartz crystal frequency tolerance			-100		+100	ppm
Load capacitance					15	pF
Thermal Shutdown						
Thermal shutdown threshold	T_{SD}			150		°C
Thermal shutdown hysteresis	T_{SD_HYS}			15		°C

DETAILED DESCRIPTION

Overview

The SiLM6000 is a power line communication (PLC) receiver with a SunSpec™ compliant demodulator. An internal charge pump turns on an external NFET to connect the PV module to the string when the PLC receive detects a keep alive signal on the DC power line and turns off the external NFET in the absence of the keep alive signal. The SiLM6000 also integrates a fixed output regulator for string voltage regulation in shutdown mode. The fixed output regulator provides an 1V output with 10mA driving capability. when the keep alive signal is not detected, this output can be switched to the string for the purpose of simplifying installation.

Power line Communication Receiver

The SiLM6000 uses Spread Frequency Shift Keying (S-FSK) as a frequency modulation scheme. S-FSK is a modulation and demodulation technique combining some of the advantages of a classical spread spectrum system, such as immunity against narrowband interferences with the advantages of a classical FSK system, low-complexity, and well-investigated implementations.

The transmitter assigns the space frequency f_S to “data 0” and the mark frequency f_M to “data 1”. The difference between S-FSK and the classical FSK lies in the fact that F_S and F_M are placed far from each other (spreading). By placing f_S far from f_M, their transmission quality becomes independent, and each frequency will have its own attenuation factor and local narrow-band noise spectrum.

The receiver performs conventional FSK demodulation at the two possible frequencies (the half-channels) resulting in two demodulated signals D_S and D_M. If the average reception quality of the two half-channels is similar, then the decision unit decides on the higher of the two demodulated channels (“data 0” if D_S>D_M, “data 1” if D_S<D_M). If, however, the average reception quality of one half-channel is significantly better than the quality of the other half-channel, then the decision unit compares the demodulated signal of the better channel with a threshold T, thus ignoring the worse channel.

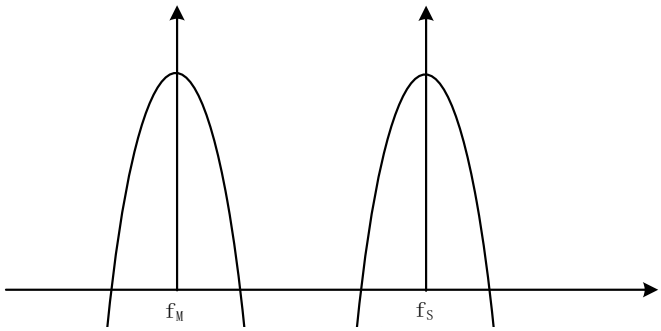


Figure 3. S-FSK Waveform on Frequency Domain

The Keep alive signal is comprised of an 11 bits packet as shown in Figure 4. The tone representing each bit in the sequence is transmitted every 5.12ms (T_S) and one word includes 11 bits. One full frame consists of 3 keep alive words and 16 zero energy words with a frame length of 1.07008 second.

All the tone frequencies and the bit rate should be within a ±100ppm tolerance when in operation, including with temperature and aging change.

The Table 1 shows all the code sequences that supported by the SiLM6000.

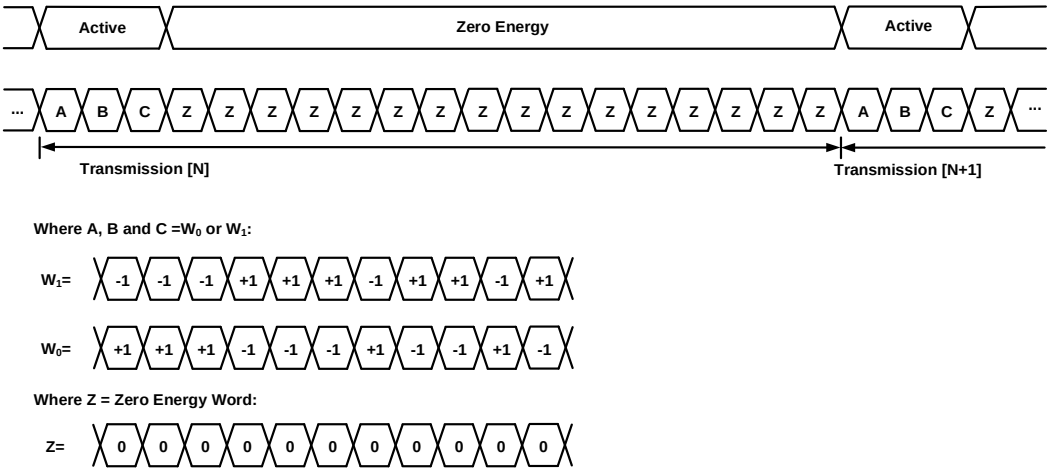


Figure 4. Keep Alive Duty Cycle Timing Diagram

Table 1. Allowable Code Sequences

Transmitter Specification	Code	SunSpec Remark	SiLM6000 Response
Permission to Operate	ABC=W_1 W_1 W_1	Mandatory	GATE becomes high after receiving the Permission to Operate code (PTOC). GATE becomes low in about 8.38 seconds if no PTOC received.
Accelerated Shutdown	ABC= W_0 W_0 W_0	Optional	GATE becomes low in 0.25 seconds after receiving this code
Proprietary Use 1 Includes Permission to Operate	ABC= W_1 W_0 W_1	Optional	GATE becomes high after receiving the PTOC. GATE becomes low in about 8.38 seconds if no PTOC received.
Proprietary Use 2 Without Permission to Operate	ABC= W_0 W_1 W_0	Optional	GATE will not be high when receiving this code
Reserved Includes Permission to Operate	ABC= W_1 W_1 W_0	Do Not Use	GATE becomes high after receiving the PTOC. GATE becomes low in about 8.38 seconds if no PTOC received.
Reserved Without Permission to Operate	ABC= W_0 W_0 W_1	Do Not Use	GATE will not be high when receiving this code
Reserved Without Permission to Operate	ABC= W_0 W_1 W_1	Do Not Use	GATE will not be high when receiving this code
Reserved Without Permission to Operate	ABC= W_1 W_0 W_0	Do Not Use	GATE will not be high when receiving this code

Functional Mode

The SiLM6000 has two operation mode, one is normal operation mode and another is shutdown mode.

Normal operation occurs when the SiLM6000 receives the proper keep alive signal and responds by pulling high the voltage between GATE and STBOUT.

Shutdown mode operation occurs when the SiLM6000 does not receive the keep alive signal. In the shutdown mode, the SiLM6000 pull low the voltage between the GATE and STBOUT, and outputs a regulated 1 V supply on the STBOUT pin.

The SiLM6000 also features a digital input, KA_IN, that can be used to override the input from the PLC receiver to activate GATE. When the KA_IN is high, the GATE is forced to high ignoring the PLC input signal. If the KA_IN is low, the GATE pin is controlled by the signal from the PLC.

Internal Regulator

The SiLM6000 integrates three regulators. The 5.0V and 3.3V regulator provides power supply for internal circuits and the 1V regulator are connected to the STBOUT pin during the shutdown mode.

The BP5V also support external power supply to power the IC to reduce the power dispassion in some high PV voltage system. The external support voltage should between 5.1V to 5.5V.

Flash Test

The SiLM6000 supports the flash testing in the PV system. When the VPVP voltage ramps up from a voltage below VPVP under-voltage lockout falling threshold ($V_{PVP\_UVLO\_F}$) to a voltage above VPVP under-voltage lockout rising threshold ($V_{PVP\_UVLO\_R}$), the GATE pin is forced on for a fixed time (t_{FLASH}). After this fixed time, the GATE pin is controlled by the PLC signal or the KA_IN.

Quartz Crystal

In order for SiLM6000 to operate properly a 12 MHz crystal will need to be used as input to the XTAL_IN pin. It is important to select a crystal with a temperature rating (-40 to 125°C), tolerance (+/-100 ppm) and lifetime spec that matches the requirements of the PV system being designed. The load capacitance (CL) of the crystal should equal 12 pF. The losses (internal R from the crystal) should be less than 120 Ω and the shunt capacitor should be less than 3 pF. In the reference design, a YangXing Technology XC322512MOB4SA-18 quartz crystal is chosen to meet these requirements.

RLC filter

The RLC resonant filter is used to couple the AC communication signal to the DC blocking caps feeding the device pins. It also provides a small amount of noise filtering from the DC power line.

The resistor value is chosen to meet the receiver input impedance (Z_{in}) specification of 0.7 – 1.5 Ω at both f_S and f_M.

Ideally, the bandwidth is designed to be above 50 kHz. We can relate the bandwidth to the L and C values as in Equation 1.

$$Q = \frac{f_c}{BW} = R\sqrt{\frac{C}{L}} \quad (1)$$

The inductor L and capacitor C are then chosen to meet the center frequency in Equation 2.

$$f_c = 137.5\ kHz = \frac{1}{2\pi\sqrt{LC}} \quad (2)$$

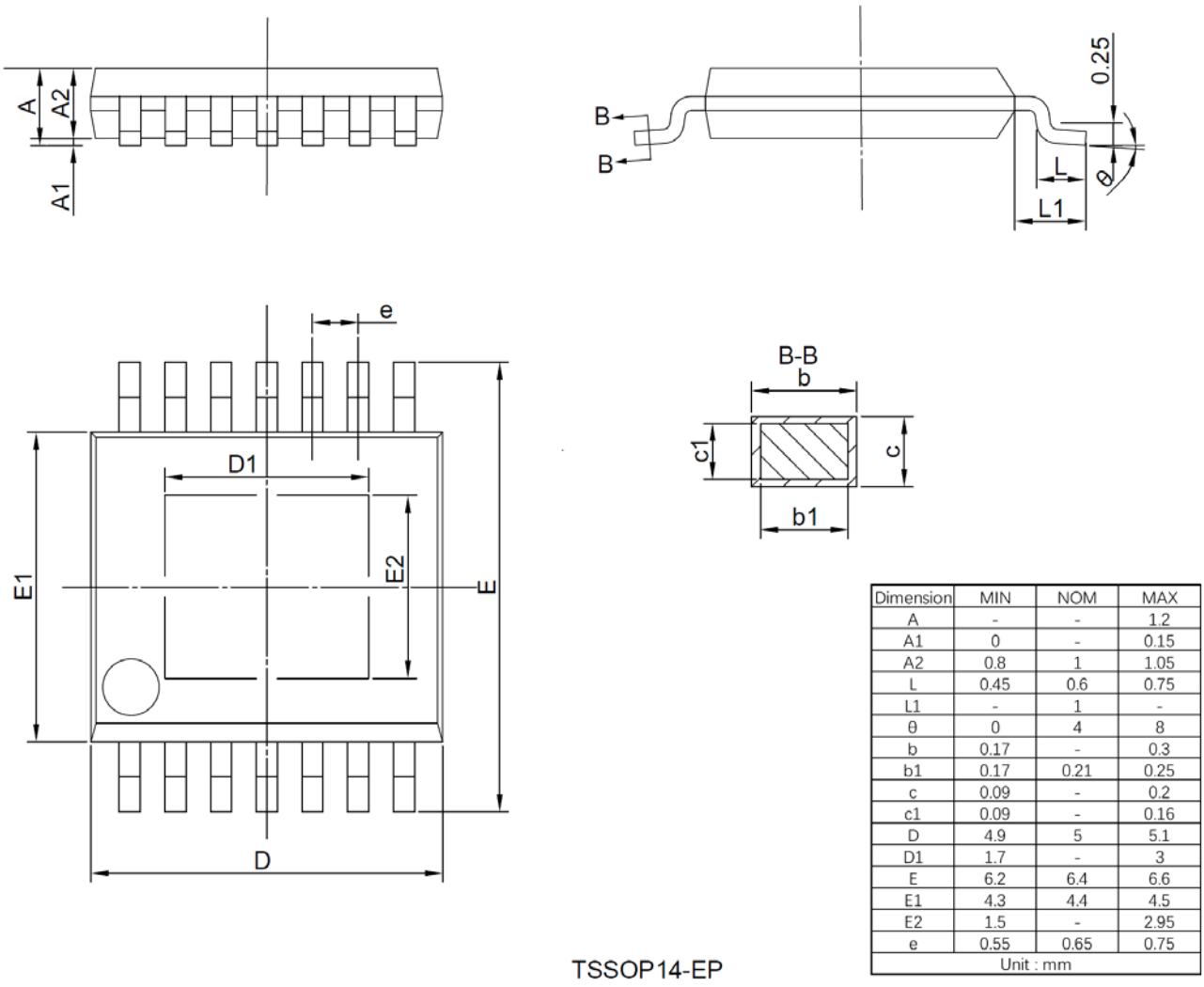
In the example design, the following values are chosen: L = 1 uH, C = 1.3 uF, R = 1 Ω.

Thermal Shutdown

The SiLM6000 has thermal shutdown function to protect itself if the junction temperature exceeds 150°C.

The thermal shutdown has a hysteresis of 15°C. The only function controlled by the thermal shutdown is the 1 V regulator. When the junction temperature exceeds the thermal shutdown threshold, the 1V regulator will be disabled. When the die temperature decreases below 135°C, the 1 V regulator will be re-enabled.

PACKAGE CASE OUTLINES



Dimension	MIN	NOM	MAX
A	-	-	1.2
A1	0	-	0.15
A2	0.8	1	1.05
L	0.45	0.6	0.75
L1	-	1	-
θ	0	4	8
b	0.17	-	0.3
b1	0.17	0.21	0.25
c	0.09	-	0.2
c1	0.09	-	0.16
D	4.9	5	5.1
D1	1.7	-	3
E	6.2	6.4	6.6
E1	4.3	4.4	4.5
E2	1.5	-	2.95
e	0.55	0.65	0.75
Unit : mm			

TSSOP14-EP

Figure 5. TSSOP14-EP Package Outline Dimensions

REVISION HISTORY

Note: page numbers for previous revisions may differ from page numbers in current version

Page or Item	Subjects (major changes since previous revision)
Datasheet Rev 1.0: 22/May/2023	
Whole document	Initial release