

Half-Bridge N-Channel MOSFET Driver for DC/DC Conversion

FEATURES

- 5-V Gate Drive
- Undervoltage Lockout
- Internal Bootstrap Diode
- PWM pin tristate enable feature
- Switching Frequency up to 1 MHz
- Drive MOSFETs In 4.5- to 50-V Systems



Pb-free Available

APPLICATIONS

- Multi-Phase DC/DC Conversion
- High Current Synchronous Buck Converters
- High Frequency Synchronous Buck Converters
- Asynchronous-to-Synchronous Adaptations
- Mobile Computer DC/DC Converters
- Desktop Computer DC/DC Converters

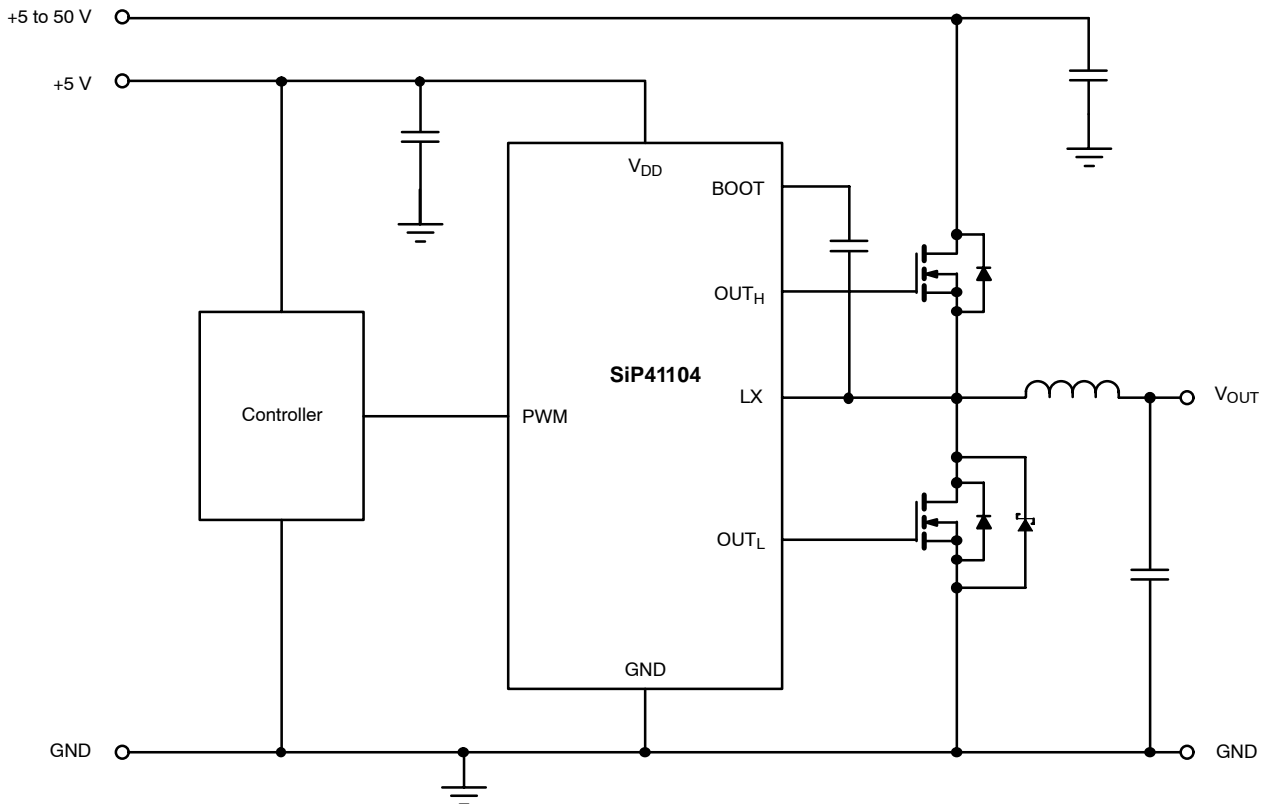
DESCRIPTION

The SiP41104 is a high-speed half-bridge MOSFET driver for use in high frequency, high current, multiphase dc-to-dc synchronous rectifier buck power supplies. It is designed to operate at switching frequencies up to 1 MHz. The high-side driver is bootstrapped to allow driving n-channel MOSFETs.

The SiP41104 comes with adaptive shoot-through protection to prevent simultaneous conduction of the external MOSFETs.

The SiP41104 is available in both standard and lead (Pb)-free 8-Pin SOIC packages and is specified to operate over the industrial temperature range of $-40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (ALL VOLTAGES REFERENCED TO GND = 0 V)

V_{DD} , PWM	7 V	Power Dissipation ^a	
LX, BOOT	55 V	SO-8	770 mW
BOOT to LX	7 V	Thermal Impedance (Θ_{JA}) ^a	
Storage Temperature	-40 to 150°C	SO-8	130°C/W
Operating Junction Temperature	125°C	Notes	
		a. Device mounted with all leads soldered or welded to PC board.	
		a. Derate 7.7 mW/°C	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE (ALL VOLTAGES REFERENCED TO GND = 0 V)

V_{DD}	4.5 V to 5.5 V	C_{BOOT}	100 nF to 1 μ F
V_{BOOT}	4.5 V to 50 V	Operating Temperature Range	-40 to 85°C

SPECIFICATIONS ^a						
Parameter	Symbol	Test Conditions Unless Specified $V_{DD} = 5\text{ V}$, $V_{BOOT} - V_{LX} = 5\text{ V}$, $C_{LOAD} = 3\text{ nF}$ $T_A = -40\text{ to }85^\circ\text{C}$	Limits			Unit
			Min ^a	Typ ^b	Max ^a	
Power Supplies						
Supply Voltage	V_{DD}		4.5		5.5	V
Supply Quiescent	I_{DDQ}	$f_{PWM} = 1\text{ MHz}$, $C_{LOAD} = 0$		2.5	3.5	mA
Tristate Current	I_{DDT}	PWM = Open		500	1000	μ A
Reference Voltage						
Break-Before-Make	V_{BBM}			1		V
PWM Input						
Input High	V_{IH}		4.0		V_{DD}	V
Input Low	V_{IL}				0.5	
Bias Current	I_B	$T_A = 25^\circ\text{C}$		± 700	± 1400	μ A
Tristate Threshold	High	V_{TSH}	3.2			V
	Low	V_{TSL}			1.9	
Tristate Shutdown Timeout ^c	t_{TST}	Rising or Falling		425		ns
High-Side Undervoltage Lockout						
Threshold	V_{UVHS}	Rising or Falling	2.5	3.35	3.75	V
Bootstrap Diode						
Forward Voltage	V_F	$I_F = 10\text{ mA}$, $T_A = 25^\circ\text{C}$	0.70	0.76	0.82	V
MOSFET Drivers						
High-Side Drive Current ^c	$I_{PKH(source)}$	$V_{BOOT} - V_{SH} = 4.5\text{ V}$		0.9		A
	$I_{PKH(sink)}$			1.1		
Low-Side Drive Current ^c	$I_{PKL(source)}$	$V_{DD} = 4.5\text{ V}$		0.8		
	$I_{PKL(sink)}$			1.5		
High-Side Driver Impedance	$R_{DH(source)}$	$V_{DD} = 4.5\text{ V}$, $S_H = \text{GND}$		2.5	3.8	Ω
	$R_{DH(sink)}$			2.2	3.3	
Low-Side Driver Impedance	$R_{DL(source)}$	$V_{DD} = 4.5\text{ V}$		3.4	5.1	
	$R_{DL(sink)}$			1.4	2.1	



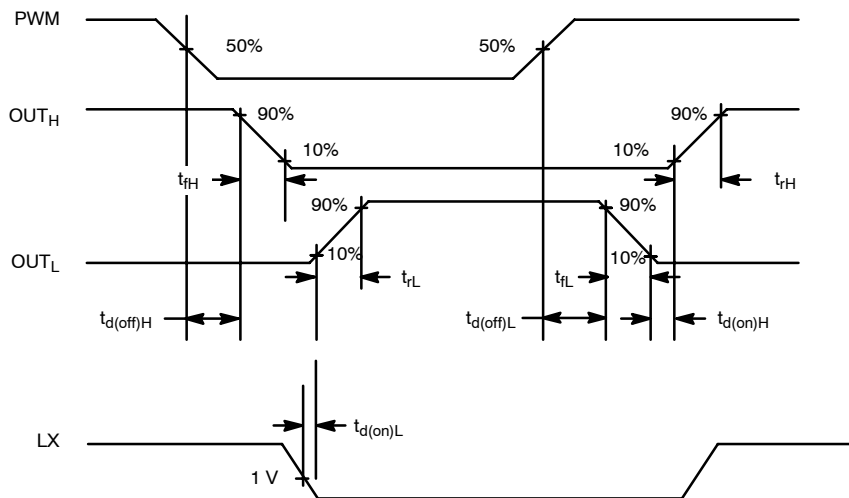
SPECIFICATIONS^a

Parameter	Symbol	Test Conditions Unless Specified $V_{DD} = 5\text{ V}$, $V_{BOOT} - V_{LX} = 5\text{ V}$, $C_{LOAD} = 3\text{ nF}$ $T_A = -40\text{ to }85^\circ\text{ C}$	Limits			Unit
			Min ^a	Typ ^b	Max ^a	
MOSFET Drivers						
High-Side Rise Time	t_{rH}	10% – 90%		32	40	ns
High-Side Fall Time	t_{fH}	90% – 10%		36	45	
High-Side Propagation Delay ^c	$t_{d(off)H}$	See Timing Waveforms		20		
	$t_{d(on)H}$	See Timing Waveforms		30		
Low-Side Rise Time	t_{rL}	10% – 90%		45	55	
Low-Side Fall Time	t_{fL}	90% – 10%		20	30	
Low-Side Propagation Delay ^c	$t_{d(off)L}$	See Timing Waveforms		30		
	$t_{d(on)L}$	See Timing Waveforms		30		
LX Timer						
LX Falling Timeout ^c	t_{LX}			420		ns
V_{DD} Undervoltage Lockout						
Threshold Rising	V_{UVLOR}			4.3	4.5	V
Threshold Falling	V_{UVLOF}		3.7	4.1		
Hysteresis				0.4		
Power on Reset Time				2.5		ms
Thermal Shutdown						
Temperature	T_{SD}	Temperature Rising		165		°C
Hysteresis	T_H	Temperature Falling		25		

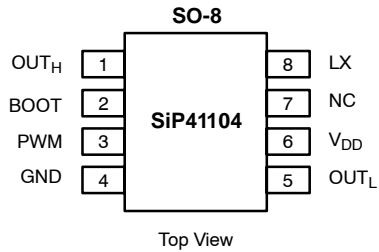
Notes

- a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum (–40° to 85°C).
- b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing and are measured at $V_{CC} = 5\text{ V}$ unless otherwise noted.
- c. Guaranteed by design.

TIMING WAVEFORMS



PIN CONFIGURATION AND TRUTH TABLE



TRUTH TABLE		
PWM	OUT _H	OUT _L
L	L	H
H	H	L
TriState	L	L

ORDERING INFORMATION		
Part Number	Temperature Range	Marking
SiP41104DY-T1	-40 to 85°C	41104
SiP41104DY-T1—E3		

Eval Kit	Temperature Range
SiP41104DB	-40 to 85°C

PIN DESCRIPTION		
Pin Number	Name	Function
1	OUT _H	High-side MOSFET gate drive
2	BOOT	Bootstrap supply for high-side driver. A capacitor connects between BOOT and LX.
3	PWM	Input signal for the MOSFET drivers
4	GND	Ground
5	OUT _L	Synchronous or low-side MOSFET gate drive
6	V _{DD}	+5-V supply
7	NC	No Connect
8	LX	Connection to source of high-side MOSFET, drain of the low-side MOSFET, and the inductor

Shutdown

The driver enters shutdown mode when the signal driving PWM enters HiZ or “tristate” mode for more than 400 ns.

V_{DD} Bypass Capacitor

MOSFET drivers draw large peak currents from the supplies when they switch. A local bypass capacitor is required to supply this current and reduce power supply noise. Connect a 1- μ F ceramic capacitor as close as practical between the V_{DD} and GND pins.

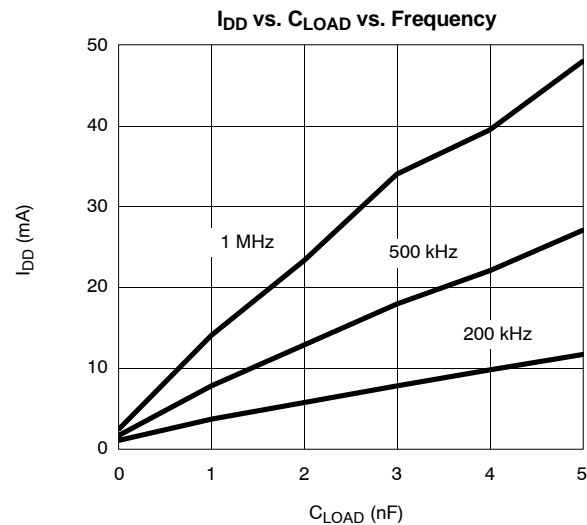
Undervoltage Lockout

Undervoltage lockout prevents control of the circuit until the supply voltages reach valid operating levels. The UVLO circuit forces OUT_L and OUT_H to low when V_{DD} is below its specified voltage. A separate UVLO forces OUTH low when the voltage between BOOT and LX is below the specified voltage.

Thermal Protection

If the die temperature rises above 165°C, the thermal protection disables the drivers. The drivers are re-enabled after the die temperature has decreased below 140°C.

TYPICAL CHARACTERISTICS



TYPICAL WAVEFORMS

Figure 2. PWM Signal vs. LX (Rising)

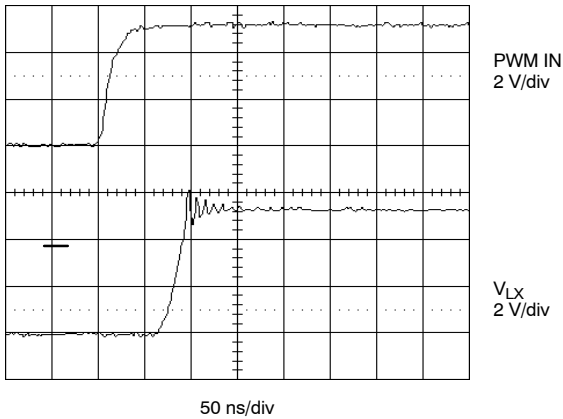


Figure 3. PWM Signal vs. LX (Falling)

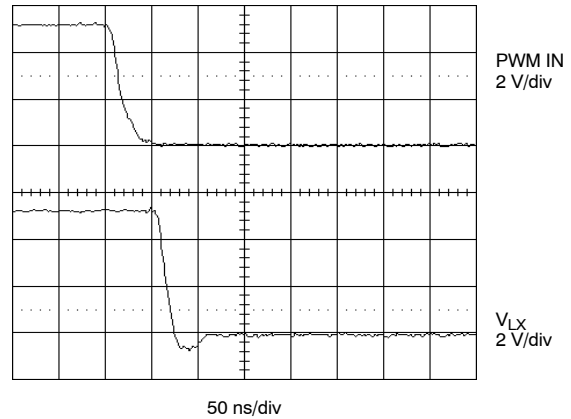


Figure 4. PWM Signal vs. HS Gate and LS Gate (Rising)

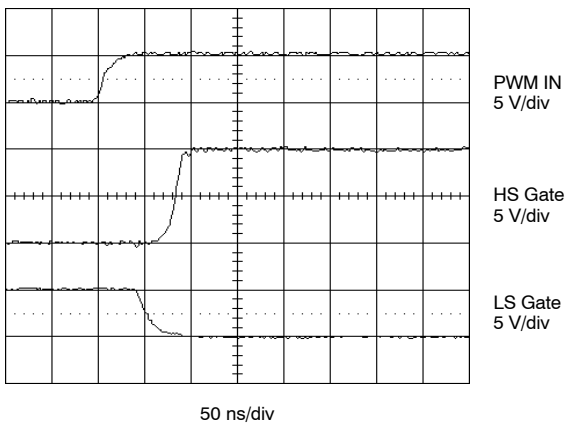
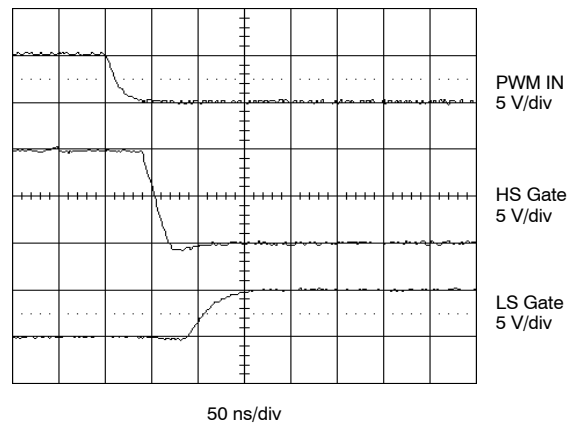


Figure 5. PWM Signal vs. HS Gate and LS Gate (Falling)



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