

Vishay Siliconix

N-Channel 100-V (D-S) MOSFET

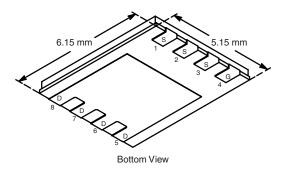
PRODUCT SUMMARY					
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A) ^a	Q _g (Typ.)		
100	0.0306 at V _{GS} = 10 V	28.4	15.5 nC		
	0.0327 at V _{GS} = 7.5 V	27.5	13.5110		

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC



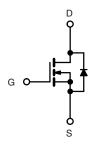
PowerPAK SO-8



Ordering Information: SiR432DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

APPLICATIONS

Primary Side Switch



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS	S T _A = 25 °C, unle	ss otherwise not	ed		
Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V_{DS}	100	V	
Gate-Source Voltage		V_{GS}	± 20]	
	T _C = 25 °C		28.4		
Continuous Drain Current (T _{.I} = 150 °C)	T _C = 70 °C		22.7		
Continuous Diam Current (1) = 130 C)	T _A = 25 °C	I _D	8.6 ^{b, c}		
	T _A = 70 °C		6.9 ^{b, c}		
Pulsed Drain Current		I _{DM}	40	A	
Continuous Course Prain Diade Current	T _C = 25 °C	I-	40 ^g		
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	4.2 ^{b, c}		
Avalanche Current	L = 0.1 mH	I _{AS}	17	mJ	
Single-Pulse Avalanche Energy	L=0.1 mn	E _{AS}	14.5		
	T _C = 25 °C		54		
Maximum Power Dissipation	T _C = 70 °C	P _D	34.7	w	
Maximum Power Dissipation	T _A = 25 °C	' b	5.0 ^{b, c}		
	T _A = 70 °C		3.2 ^{b, c}		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature) ^{d, e}			260		

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{b, f}	t ≤ 10 s	R_{thJA}	20	25	°C/W	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	1.8	2.3	- C/VV	

Notes:

- a. Based on $T_C = 25$ °C.
- b. Surface Mounted on 1" x 1" FR4 board.
- c. t = 10 s.
- d. See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- f. Maximum under Steady State conditions is 65 °C/W.

SiR432DP

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SPECIFICATIONS $T_J = 25 ^{\circ}C_1$, unless oth	nerwise noted					
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	100			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I _D = 250 μA		100		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	ι _D = 250 μΑ		- 8.6			
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2		4	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zovo Coto Voltago Desig Occurrent	I	V _{DS} = 100 V, V _{GS} = 0 V			1	μА	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V, T _J = 55 °C			10		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \le 5 \text{ V}, V_{GS} = 10 \text{ V}$	40			Α	
	D.	$V_{GS} = 10 \text{ V}, I_D = 8.6 \text{ A}$		0.0255	0.0306	Ω	
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 7.5 \text{ V}, I_D = 8.3 \text{ A}$		0.0272	0.0327		
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 8.6 A		38		S	
Dynamic ^b				•	l .		
Input Capacitance	C _{iss}			1170		pF	
Output Capacitance	C _{oss}	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		115			
Reverse Transfer Capacitance	C _{rss}			45			
Total Gate Charge	Q_g $V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 8.6 \text{ A}$ $V_{DS} = 50 \text{ V}, V_{GS} = 7.5 \text{ V}, I_D = 8.6 \text{ A}$	$V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 8.6 \text{ A}$		21	32	nC	
Total date offarge				15.5	24		
Gate-Source Charge			5.9		nC		
Gate-Drain Charge	Q_{gd}			5.4			
Gate Resistance	R_g	f = 1 MHz	0.2	0.9	1.8	Ω	
Turn-On Delay Time	t _{d(on)}			12	20	ns	
Rise Time	t _r	$V_{DD} = 50 \text{ V, } R_L = 7.2 \Omega$ $I_D \cong 6.9 \text{ A, } V_{GEN} = 10 \text{ V, } R_g = 1 \Omega$		10	20		
Turn-Off Delay Time	t _{d(off)}			20	30		
Fall Time	t _f			8	16		
Turn-On Delay Time	t _{d(on)}			14	21		
Rise Time	t _r	V_{DD} = 50 V, R_L = 7.2 Ω		9	18		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 6.9 \text{ A}, V_{GEN} = 7.5 \text{ V}, R_g = 1 \Omega$		18	27		
Fall Time	t _f			8	16		
Drain-Source Body Diode Characterist	ics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			40	A	
Pulse Diode Forward Current ^a	I _{SM}				40		
Body Diode Voltage	V_{SD}	I _S = 6.9 A		8.0	1.2	V	
Body Diode Reverse Recovery Time	t _{rr}			43	65	ns	
Body Diode Reverse Recovery Charge	Q _{rr}	I _F = 6.9 A, dl/dt = 100 A/μs, T _{.I} = 25 °C		80	120	nC	
	t _a	1 _F = 0.0 Λ, αι/αι = 100 Λ/μο, 1 _J = 20 0		33		no	
Reverse Recovery Fall Time	¹а			00	<u></u>	ns	

Notes:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.

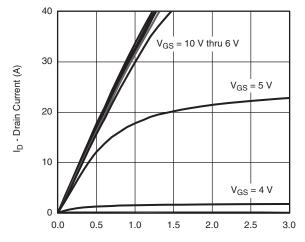
b. Guaranteed by design, not subject to production testing.

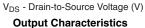


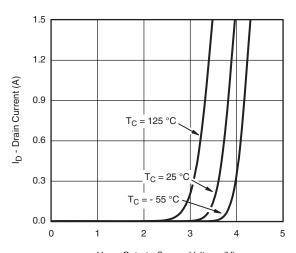




TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

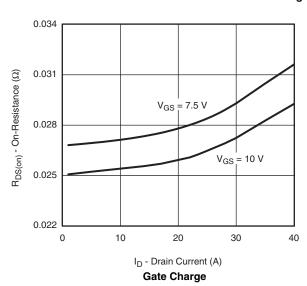


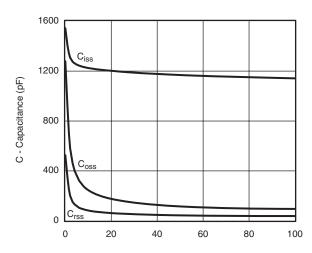




V_{GS} - Gate-to-Source Voltage (V)

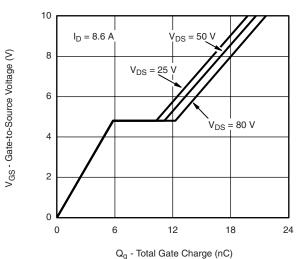
On-Resistance vs. Drain Current and Gate Voltage



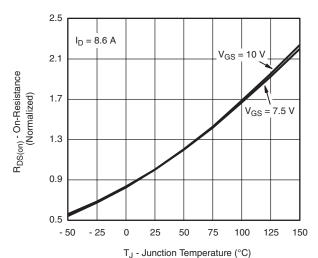


V_{DS} - Drain-to-Source Voltage (V)





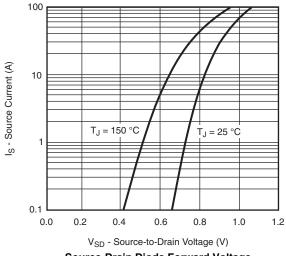
Capacitance

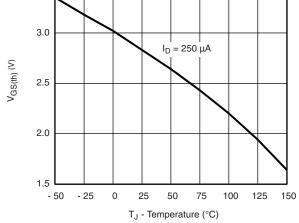


On-Resistance vs. Junction Temperature

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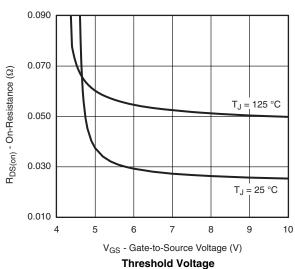
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



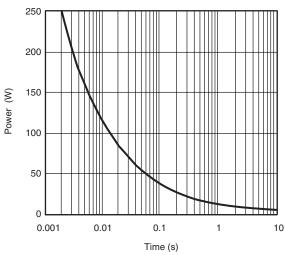


3.5

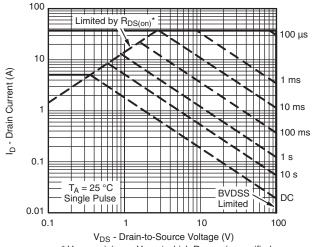




On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient

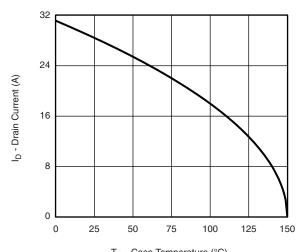


* $V_{GS} > \mbox{ minimum } V_{GS}$ at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

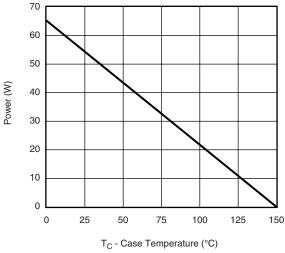


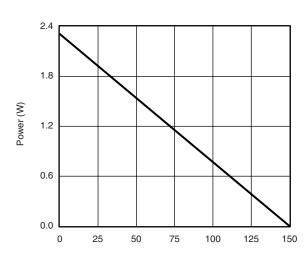
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



 $T_{\mbox{\scriptsize C}}$ - Case Temperature (°C)

Current Derating*





T_A - Ambient Temperature (°C)

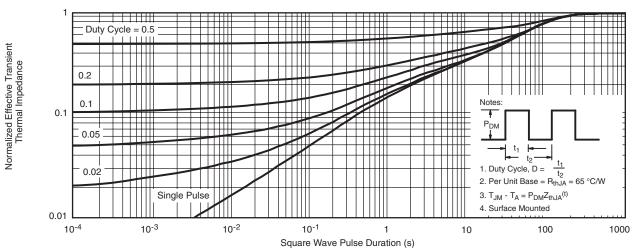
Power Derating Power Derating

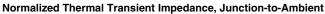
^{*} The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

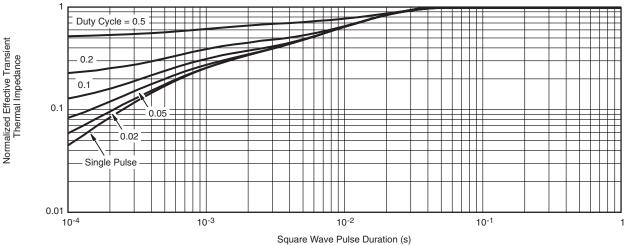
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted







Normalized Thermal Transient Impedance, Junction-to-Case

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