SiT1568 PRELIMINARY

1.2 mm² µPower, 5 ppm, 32.768 kHz TCXO with In-System Auto-Calibration

SiTime

Features

- 32.768 kHz ±5 ppm all-inclusive frequency stability
- In-system auto-calibration:
  - Compensates for board-level stress-induced frequency errors
  - Improves all-inclusive frequency stability
- World's smallest TCXO Footprint: 1.2 mm²
  - 1.5 x 0.8 mm CSP
  - No external bypass cap required
- Drives multiple loads and eliminates multiples XTALs
- Low integrated phase jitter (IPJ) suitable for multiplying up for portable audio: 2.5ns$_{RMS}$
- Ultra-low power: 4.5 µA
- Supply voltage: 1.8V ±10%
- Operating temperature ranges: -20°C to +70°C, -40°C to +85°C
- Pb-free, RoHS and REACH compliant

Applications

- Smart watches, health and wellness monitors
- Ultra-accurate RTC reference clock
- Smart utility meters, E-meters
- Internet of Things (IoT)

TempFlat MEMS™

Electrical Characteristics

Table 1. Electrical Characteristics

Conditions: Min/Max limits are over temperature, Vdd = 1.8V ±10%, unless otherwise stated. Typicals are at 25°C and Vdd = 1.8V.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency and Stability						
Output Frequency	Fout		32.768		kHz	
Total Frequency Stability after Overmold [1]	F_stab	-5		5	ppm	All inclusive, **after** overmold, **post** in-system calibration.
		-25		25	ppm	All inclusive, **after** overmold, **before** in-system calibration.
Total Frequency Stability without Overmold or Calibration [1]		-5		5	ppm	All inclusive, under influence of up to 5°C/sec temp gradient and board-level underfill.
Allan Deviation	AD		1e-8	4e-8	-	1 second averaging time.
First Year Frequency Aging	F_aging		±1		ppm	T_A = 25°C, Vdd = 1.8V, with overmold.
Jitter and Frequency Response Performance						
Integrated Phase Jitter	IPJ		1.8	2.5	ns$_{RMS}$	Integration bandwidth = 100 Hz to 16.384 kHz. Inclusive of 50 mV peak-to-peak sinusoidal noise on Vdd. Noise frequency 100 Hz to 20 MHz.
RMS Period Jitter	PJ$_{RMS}$		2.5	4	ns$_{RMS}$	10,000 samples, per JEDEC standard 65B
7Peak-to-Peak Period Jitter	PJ$_{p-p}$		20	35	ns$_{p-p}$	
Dynamic Temperature Frequency Response		-0.5		+0.5	ppm/sec	Under temp ramp up to 1.5°C/sec
Supply Voltage and Current Consumption						
Operating Supply Voltage	Vdd	1.62	1.8	1.98	V	
Supply Current	Idd		4.5	5.3	µA	No Load.
Start-up Time at Power-up	t_start			300	ms	Measured when supply reaches 90% of final Vdd to the first output pulse.
Operating Temperature Range						
Operating Temperature Range	Op_Temp	-20		70	°C	"C" ordering code.
		-40		85	°C	"I" ordering code.
LVCMOS Output						
Output Rise/Fall Time	tr, tf		9	20	ns	10-90% (Vdd), 15 pF Load.
Output Clock Duty Cycle	DC	45		55	%	
Output Voltage High	VOH	90%			Vdd	I_{OH} = -1 µA
Output Voltage Low	VOL			10%	Vdd	I_{OL} = 1 µA

Note:

1. Contact SiTime for specific overmold conditions. Relative to 32.768 kHz, includes initial tolerance, over temp, Vdd, load, hysteresis, board-level underfill, and, 3x reflow. Tested with Agilent 53132A frequency counter. Measured with 100ms gate time for accurate frequency measurement.

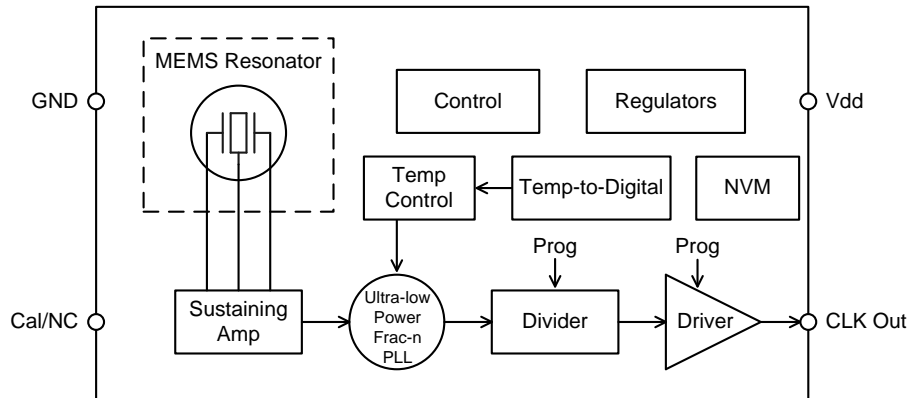## Description

SiT1568 is an ultra-small and ultra-low power 32.768 kHz TCXO optimized for battery-powered applications. SiTime's silicon MEMS technology enables the first 32 kHz TCXO in the world's smallest footprint and chip-scale packaging (CSP). Typical supply current is 4.5 µA under no load condition.

SiTime's MEMS oscillator consists of a MEMS resonator and a programmable analog circuit. SiT1568 MEMS resonator is built with SiTime's unique MEMS First™ process. A key manufacturing step is EpiSeal™ during which the MEMS resonator is annealed with temperatures over 1000°C. EpiSeal creates an extremely strong, clean, vacuum chamber that encapsulates the MEMS resonator and ensures the best performance and reliability. During EpiSeal, a poly silicon cap is grown on top of the resonator cavity, which eliminates the need for additional cap wafers or other exotic packaging. As a result, SiTime's MEMS resonator die can be used like any other semiconductor die. One unique result of SiTime's MEMS First and EpiSeal manufacturing processes is the capability to integrate SiTime's MEMS die with a SOC, ASIC, microprocessor or analog die within a package to eliminate external timing components and provide a highly integrated, smaller, cheaper solution to the customer.

TCXO Frequency Stability

SiT1568 is factory calibrated (trimmed) over multiple temperature points to guarantee extremely tight stability over temperature. Unlike quartz crystals that have a classic tuning fork parabola temperature curve with a 25°C turnover point with a 0.04 ppm/C^2 temperature coefficient, the SiT1568 temperature coefficient is calibrated and corrected over temperature with an active temperature correction circuit. The result is a 32 kHz TCXO with extremely tight frequency variation over the -40°C to +85°C temperature range.

When measuring the output frequency of SiT1568 with a frequency counter, it is important to make sure the counter's gate time is ≥100 ms. Shorter gate times may lead to inaccurate measurements.

In-System Auto Calibration

SiT1568 provides a unique, in-system calibration feature that compensates for assembly-related frequency offsets for improved overall frequency stability. The on-chip auto-calibration function is performed one-time during the customer's production system manufacturing process. In order to initiate the one-time auto calibration process, refer to the pin 1 auto-calibration description.

After assembly, follow the calibration steps as shown in the flow chart (Figure 3). Connect pin 1 to a 10 MHz reference (GPS disciplined or equivalent) and monitor the SiT1568 CLK Out for status and error flags. A summary of these flags is shown in Table 7. SiT1568 will compare its 32.768 kHz (plus the assembly-related error) frequency to the accurate 10 MHz reference, calibrate (remove) the error and store the calibration in its internal non-volatile memory. The result is a calibrated 32.768 kHz output frequency with an overall stability (accuracy) of ±5 ppm. The entire auto-calibration process typically takes about 2 seconds.

Auto calibration is intended to be performed one time to remove the board-related offset errors. The auto-calibration procedure can be repeated if process fails during the initial steps (see Table 7). The maximum number of retries is determined by the customer.

Dynamic Temperature Frequency Response

Dynamic Temperature Frequency Response is the rate of frequency change during temperature ramps. This is an important performance metric when the oscillator is mounted near a high power component (e.g. SoC or power management) that may rapidly change the temperature of surrounding components.

For moderate temperature ramp rates (< 2°C/sec), the dynamic response is primarily determined by the steady-state frequency vs. temperature of the device. The best dynamic response is obtained from parts which have been trimmed to be flat in frequency over temperature.

For high temperature ramp rates (>5°C/sec), the latency in the temperature compensation loop contributes a larger frequency error, which is dependent on the temperature compensation update rate. This part achieves excellent performance at 3Hz update rate. This device family supports faster update rates for further reducing dynamic frequency error at the expense of slightly increased current consumption.
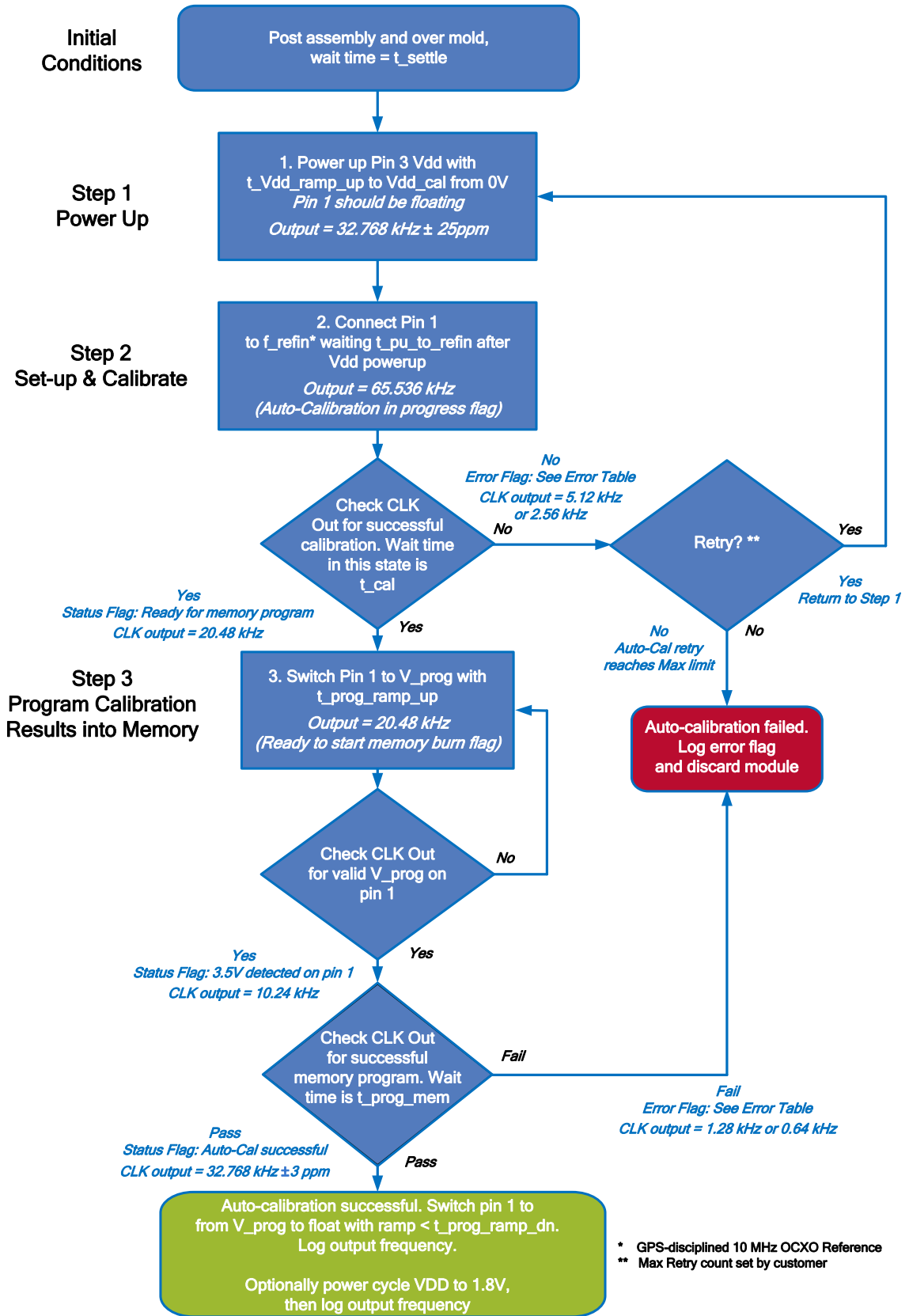
Initial Conditions

Post assembly and over mold, wait time = t_settle

Step 1 Power Up

1. Power up Pin 3 Vdd with t_Vdd_ramp_up to Vdd_cal from 0V
Pin 1 should be floating

Output = 32.768 kHz ± 25ppm

Step 2 Set-up & Calibrate

2. Connect Pin 1 to f_refin* waiting t_pu_to_refin after Vdd powerup

Output = 65.536 kHz
(Auto-Calibration in progress flag)

Check CLK Out for successful calibration. Wait time in this state is t_cal

No
Error Flag: See Error Table
CLK output = 5.12 kHz or 2.56 kHz

No

Retry? **

Yes

Yes
Return to Step 1

No
Auto-Cal retry reaches Max limit

No

Yes
Status Flag: Ready for memory program
CLK output = 20.48 kHz

Yes

Step 3 Program Calibration Results into Memory

3. Switch Pin 1 to V_prog with t_prog_ramp_up

Output = 20.48 kHz
(Ready to start memory burn flag)

Auto-calibration failed. Log error flag and discard module

Check CLK Out for valid V_prog on pin 1

No

Yes
Status Flag: 3.5V detected on pin 1
CLK output = 10.24 kHz

Yes

Check CLK Out for successful memory program. Wait time is t_prog_mem

Fail

Fail
Error Flag: See Error Table
CLK output = 1.28 kHz or 0.64 kHz

Pass
Status Flag: Auto-Cal successful
CLK output = 32.768 kHz ± 3 ppm

Pass

Auto-calibration successful. Switch pin 1 to from V_prog to float with ramp < t_prog_ramp_dn. Log output frequency.

Optionally power cycle VDD to 1.8V, then log output frequency

* GPS-disciplined 10 MHz OCXO Reference
** Max Retry count set by customer

Figure 3. Initial Offset Auto-Calibration Procedure

In-System Auto-Calibration

Table 4. Pin 1 Auto-Calibration Mode DC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Input Impedance	Z_IN	80			kΩ	Internal pull-down
Input VIH	VIH	70%			Vdd	
Input VIL	VIL			30%	Vdd	
Input Overshoot Voltage	V_IN_OD			75	mV	
Program Voltage	V_prog	3.4	3.5	3.63	V	Pin 1 NVM program voltage
Program Current	I_prog			30	mA$_{pk}$	Peak current required on pin 1 during auto-calibration
				5	mA$_{avg}$	Average current required on pin 1 during auto-calibration
Auto-Cal Voltage Noise Ripple				50	mVpp	Max noise on 3.5V auto-calibration voltage (pin 1)
Auto-Cal Vdd Supply	Vdd_cal	1.71	1.8	1.98	V	Vdd (pin 3) supply voltage during auto-calibration
Vdd Bypass Capacitor			0.1		µF	Vdd (pin 3) bypass cap required during auto-calibration
Pin 3 Idd Prog Current	Idd_prog			1	mA	Idd (pin 3) current required during auto-calibration
Pin 3 Min Power Down Threshold Voltage	Vdd_pd			0.7	V	Pin 1 Vdd threshold to guarantee internal device power-down

Table 5. Auto-Calibration Mode Timing Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Post System Assy Settling Time	t_settle	24			hr	Wait time between > absolute max storage temp exposure (150°C) and auto-cal start
Pin 3 Power Supply Ramp Rate	t_Vdd_ramp			100	ms	Ramp rate for Vdd pin during auto-calibration
Auto-Cal Ref-in Wait Time	t_pu_to_refin	0.5			sec	Time to supply auto-cal clock on pin 1 after within spec Vdd (pin 3)
Ref In Detection Time	t_refin_to_CLK_flag_65k			1.2	ms	Time to detect 10 MHz auto-cal reference inputs, 65.536 k Hz output
Auto-Cal Time	t_cal		2	5	sec	Time in Step 2, auto-calibration
Pin 1 Float Duration	t_refin_to_float	200			µs	Pin 1 float time required prior to applying prog voltage
Pin 1 Prog Voltage Ramp Rate	t_prog_ramp_up	1		100	µs	Ramp rate on Cal pin to V_prog during auto-calibration
Prog Voltage Detection Time	t_prog_to_CLK_flag_10k			100	ms	Time to detect program voltage, 10.24 kHz output flag
Pin 1 Prog Voltage Ramp Down	t_prog_ramp_dn	1		100	µs	Time to power-down prog voltage
Memory Programming Time	t_prog_mem			100	ms	Time in Step 3, Memory program
Pin 3 Power-Down Delay	t_prog_to_pd	1			ms	Pin 3 Vdd power-down delay from Pin 1 prog voltage power down

Table 6. Auto-Calibration Reference Clock Characteristics

| Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Auto-Cal Ref Clock Freq	f_refin	9.999999	10	10.000001	MHz	(10 MHz ± 100ppb) Correct reference frequency for auto-calibration
Auto-Cal Ref Clock Rise/Fall Time	t_refin_r/f	4		20	ns	20/80%; Rise and fall time of the auto-cal 10 MHz ref clock
Auto-Cal Ref Clock Duty Cycle	dc_refin	40		60	%	
Auto-Cal Ref Clock Period Jitter	pj_refin			200	ps$_{RMS}$	
Auto-Cal Ref Clock Allan Deviation	ad_refin			10	ppb	For averaging time = 1 second
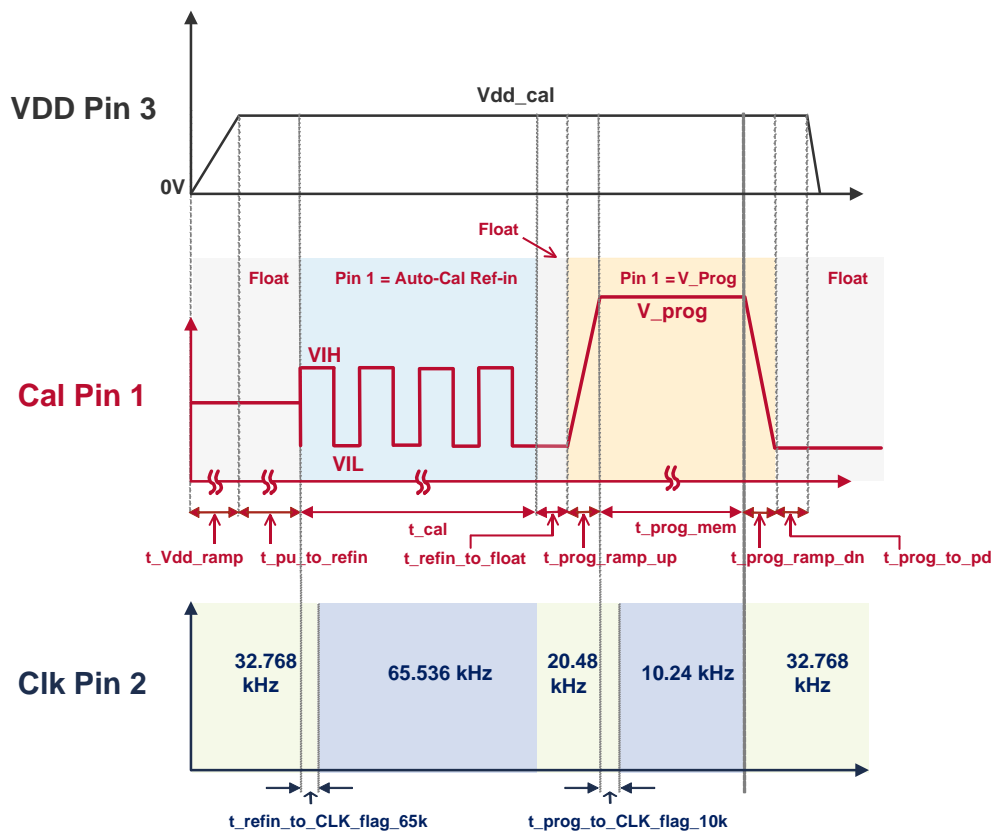
Figure 4. Auto-Calibration Timing Diagram

Table 7. Auto-Calibration Status and Error Flags

Flag Name	Output Frequency[2]	Recommended Minimum Gate Time	Status or Error Flag	Retry Calibration
Auto-Calibration in progress	65.536 kHz	10 ms	Status	N/A
Ready to start memory burn	20.48 kHz	10 ms	Status	N/A
3.3V on Pin 1 detected	10.24 kHz	10 ms	Status	N/A
Auto-Calibration successful	32.768 kHz ±3ppm	100 ms	Status	No
10 MHz reference lost during calibration step 3	5.12 kHz	10 ms	Error	Yes
Frequency correction out of range in step 3	2.56 kHz	10 ms	Error	Yes
Memory burn failed in step 3	1.28 kHz	10 ms	Error	No
3.3V lost on Pin 1 during memory burn step 3	0.64 kHz	10 ms	Error	No

Note:

2. Frequency tolerance is ±5% except for 32 kHz frequency output.
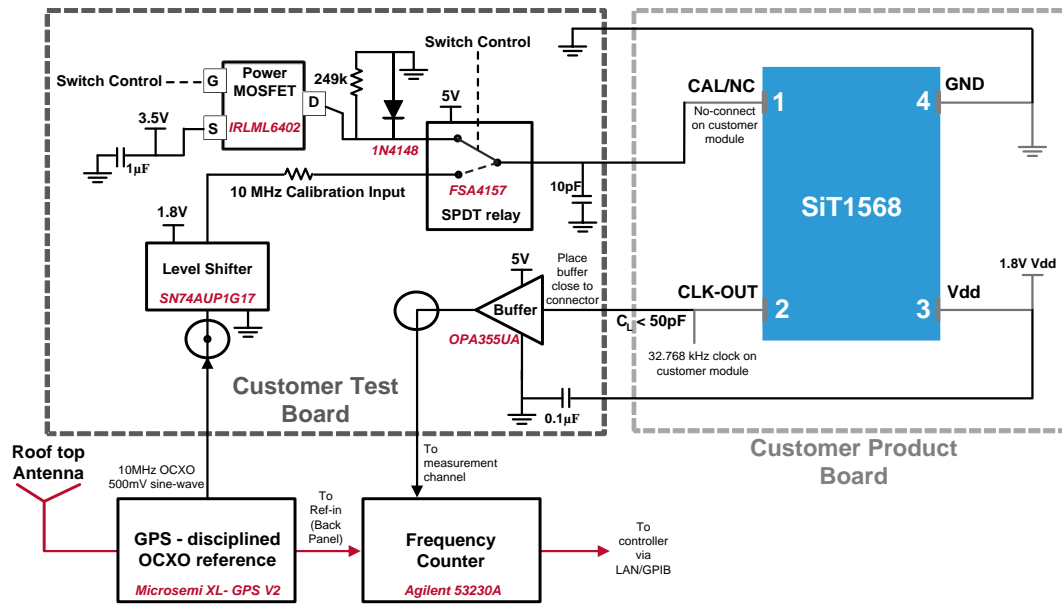
Figure 5. In-System Auto-Calibration Hardware Interface

Typical Operating Curves

(T$_A$ = 25°C, Vdd = 1.8V, supply current plots are no load, unless otherwise stated)
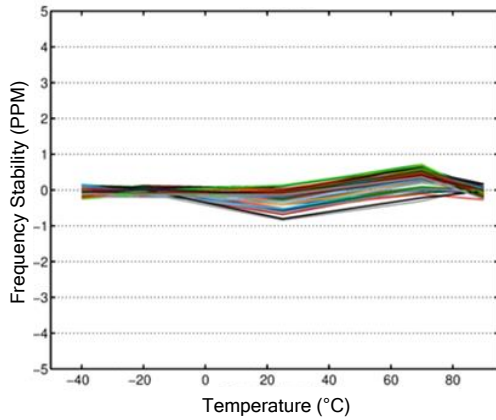
Figure 6. Frequency Stability over Temperature (Post Reflow)
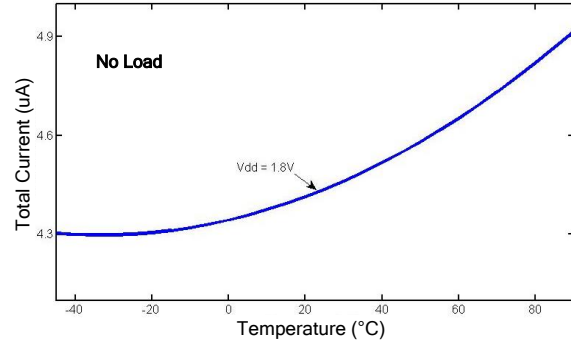
Figure 7. Supply Current over Temperature
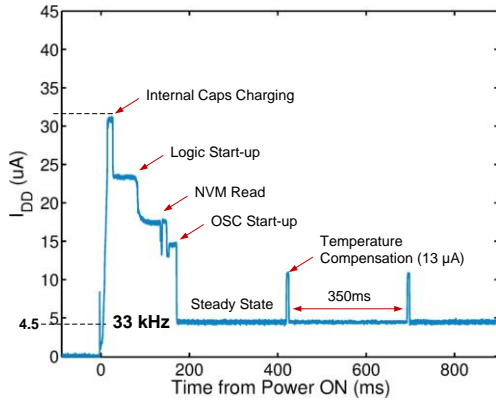
Figure 8. Start-up and Steady-State Current Profile
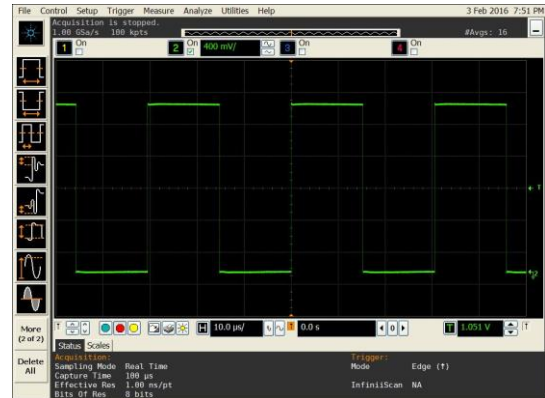
Figure 9. LVCMOS Output Swing
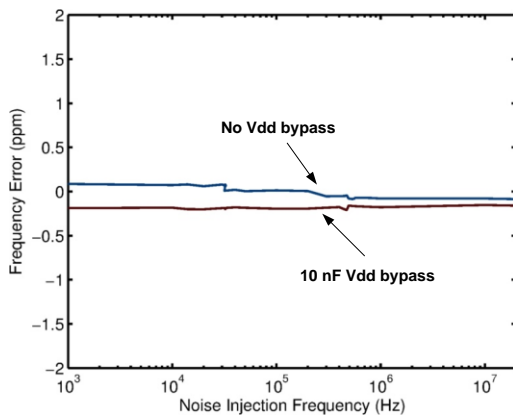
Figure 10. Power Supply Noise Rejection (PSNR)

Dynamic Frequency Response for Moderate Temperature Ramps
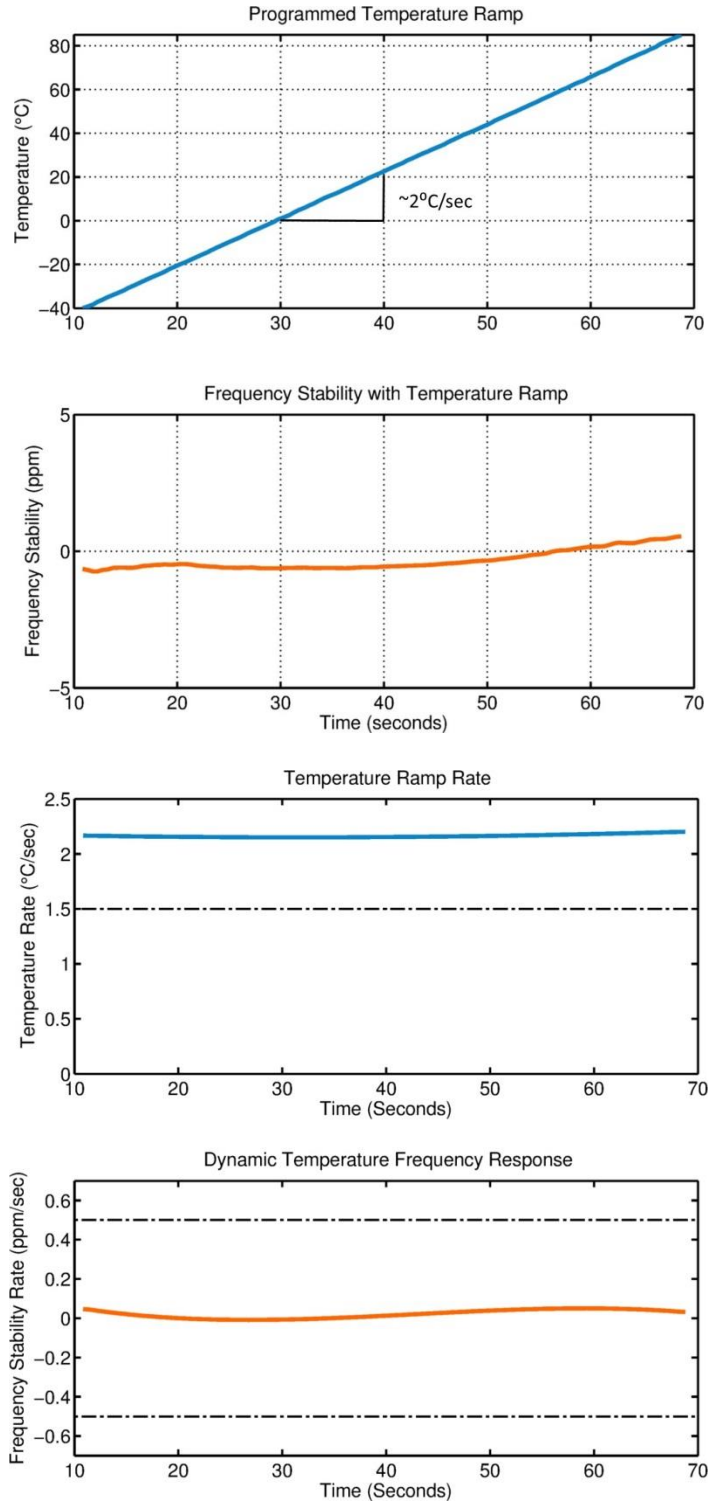
Frequency accuracy under a moderate temperature ramp up to 2°C/sec is limited by the TCXO's trimmed accuracy of the frequency stability over-temperature.

Note:
3. Measured relative to 32.768 kHz.

Dynamic Frequency Response for Fast Temperature Ramps
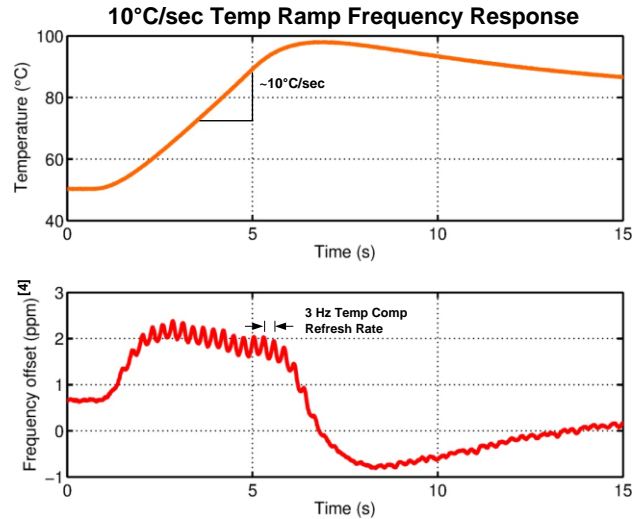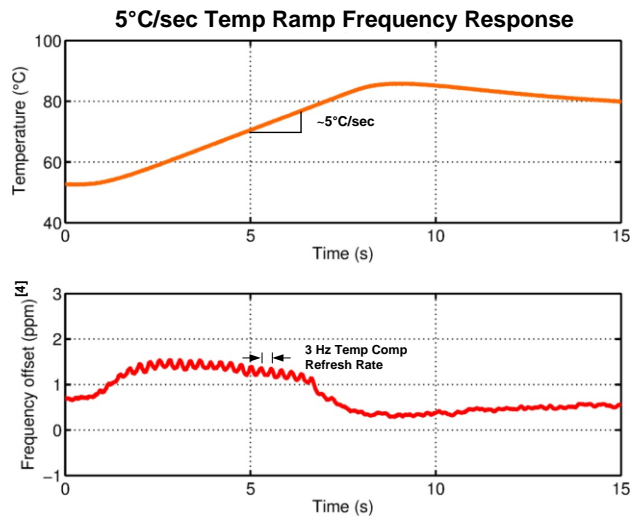
For temperature ramps >5°C/sec, the frequency accuracy is limited by the update rate of the temperature compensation path (see the 5°C/sec and 10°C/sec plots).

Contact SiTime for applications that require improved dynamic performance.

Note:
4. Referenced to 32.768 kHz.

Dimensions and Patterns

Package Size – Dimensions (Unit: mm)

Dimension Table (mm)				
Item	SYMBOL	MINIMUM	NOMINAL	MAXIMUM
Total Thickness	A	0.48	0.54	0.60
Stand Off	A1	0.22		0.28
MEMS Clearance	A2	0.027		0.113
Film Thickness	A3	0.036	0.040	0.044
Wafer Thickness	A4	0.225	0.250	0.275
Ball Diameter	b	0.30	0.315	0.33
Ball Pitch X	e		0.41 BSC	
Ball Pitch Y	e1		1.00 BSC	
MEMS X	D1		0.46 REF	
MEMS Y	E1		0.46 REF	
Body Size X	D		0.84 BSC	
Body Size Y	E		1.54 BSC	
Ball To Center X	SD		0.205 BSC	
Ball To Center Y	SE		0.500 BSC	
Package Edge Tolerance	aaa		0.040	
Coplanarity	ccc		0.075	

4 LD – 1.5 x 0.8 x 0.55 mm

Package Outline

POD-35 Rev A

SiTime®

Recommended Land Pattern (Unit: mm)

Ø0.25 (4x) NSMD pads

Ø0.35 (4x) Soldermask openings

(soldermask openings shown with dashed line around NSMD pad)

Recommended 4-mil (0.1mm) stencil thickness

Manufacturing Guidelines

1) No Ultrasonic or Megasonic cleaning: Do not subject the SiT1568 to an ultrasonic or megasonic cleaning environment. Permanent damage or long term reliability issues may occur.

2) Applying board-level underfill and overmold is acceptable and will not impact the reliability of the device. Any post assembly frequency shift can be calibrated with the in-system auto-calibration feature.

3) Reflow profile, per JESD22-A113D.

4) For additional manufacturing guidelines and marking/tape-reel instructions, refer to SiTime Manufacturing Notes.

Ordering Information

SiT1568AI-JE-DCC-32.768S

Part Family
"SiT1568"

Revision Letter
"A": is the revision

Temperature Range
"C": Extended Commercial, -20 to 70ºC
"I": Industrial, -40 to 85ºC

Package Size
"J": 1.5 mm x 0.8 mm CSP

All-Inclusive Over Temp Stability
"E": ±5 ppm

Packaging
"S": 8 mm Tape & Reel, 10ku reel
"D": 8 mm Tape & Reel, 3ku reel
"E": 8 mm Tape & Reel, 1ku reel

Samples in cut Tape

Output Clock Frequency (kHz)
32.768 kHz

LVCMOS Output
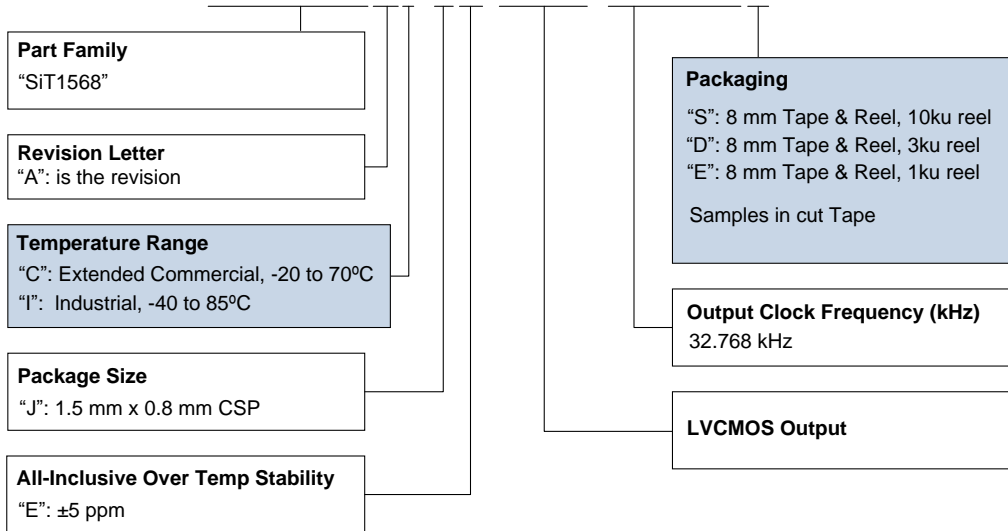
Table 8. Revision History

Version	Release Date	Change Summary
0.5	06/30/2015	Advanced datasheet initial release
0.8	03/10/2016	Preliminary datasheet initial release
1.0	03/15/2018	Updated POD (Package Outline Drawing) Updated logo and company address, other page layout changes

SiTime Corporation, 5451 Patrick Henry Drive, Santa Clara, CA 95054, USA | **Phone:** +1-408-328-4400 | **Fax:** +1-408-328-4439