# SiT1630

Ultra-Low Power, Ultra-Small 32.768 kHz or 16.384 kHz Oscillator

## Features

- <20 ppm initial tolerance
- <100 ppm stability over -40°C to +85°C
- Small SMD package: 2.0 x 1.2 mm (2012)[1]
- SOT23-5 package option for industrial and automotive applications
- Ultra-low power: 1.0 µA typ
- Vdd supply range: 1.5V to 3.63V
- Wide operating temperature range options
- Internal filtering eliminates external Vdd bypass capacitors
- Pb-free, RoHS and REACH compliant

**Note:**

1. For the smallest 32 kHz XO in CSP (1.2mm$^2$), consider the SiT1532.

## Applications

- Industrial timekeeping
- Industrial battery management
- Multi-drop 32 kHz clock distribution
- Bluetooth modules
- WiFi modules
- RTC Reference Clock

## Table 1. Electrical Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| **Frequency and Stability** | | | | | | |
| **Output Frequency** | Fout | | 32.768 or 16.384 | | kHz | |
| **Frequency Stability** | | | | | | |
| **Initial Tolerance**[2] | F_init | | | 20 | ppm | $T_A$ = 25°C, post reflow, Vdd: 1.5V – 3.63V. |
| **Frequency Stability Over Temperature**[3] | F_stab | | | 75 | ppm | $T_A$ = -10°C to +70°C, Vdd: 1.5V – 3.63V. |
| | | | | 100 | | $T_A$ = -40°C to +85°C, Vdd: 1.5V – 3.63V. |
| | | | | 150 | | $T_A$ = -40°C to +105°C, -55°C to +85C, Vdd: 1.8V – 3.63V. |
| **25°C Aging** | | -1 | | 1 | ppm | 1st Year |
| **Supply Voltage and Current Consumption** | | | | | | |
| **Operating Supply Voltage** | Vdd | 1.5 | | 3.63 | V | $T_A$ = over temperature |
| **Operating Current** | 2Idd | | 1.0 | | µA | $T_A$ = 25°C, Vdd: 1.5V – 3.3V. No load |
| | | | | 1.3 | | $T_A$ = -10°C to +70°C, Vdd max: 3.63V. No load |
| | | | | 1.4 | | $T_A$ = -40°C to +85°C, Vdd max: 3.63V. No load |
| | | | | 2.80 | | $T_A$ = -40°C to +105°C, Vdd max: 3.63V. No load |
| **Power-Supply Ramp** | t_Vdd Ramp | | | 100 | ms | Over temperature, 0 to 90% Vdd |
| **Start-up Time at Power-up** | T_start | | 180 | 300 | ms | -40°C ≤ $T_A$ ≤ 50°C, valid output |
| | | | | 450 | | -40°C ≤ $T_A$ ≤ 85°C, valid output |
| | | | | 500 + 1 period | | $T_A$ = -55°C and +105°C |
| **Operating Temperature Range** | | | | | | |
| **Commercial Temperature** | T_opn | -10 | | 70 | °C | Temp code “C” in part number ordering |
| **Industrial Temperature** | | -40 | | 85 | | Temp code “I” in part number ordering |
| **Extended Industrial Temperature** | | -40 | | 105 | | Temp code “E” in part number ordering. |
| **Extended Cold Industrial Temperature** | | -55 | | 85 | | Temp Code “D” in part number ordering. |
| **Automotive Temperature Range** | | -55 | | 105 | | Contact SiTime for Availability |
| **LVCMOS Output, $T_A$ = Over Temperature, typical values are at $T_A$ = 25°C** | | | | | | |
| **Output Rise/Fall Time** | tr, tf | | 100 | 200 | ns | 10-90%, 15 pF load, Vdd = 1.5V to 3.63V |
| | | | | | | 10-90% (Vdd), 5 pF load, Vdd ≥ 1.62V |
| **Output Clock Duty Cycle** | DC | 48 | | 52 | % | |
| **Output Voltage High** | VOH | 90% | | | V | Vdd: 1.5V – 3.63V. $I_{OH}$ = -10 µA, 15 pF |
| **Output Voltage Low** | VOL | | | 10% | V | Vdd: 1.5V – 3.63V. $I_{OL}$ = 10 µA, 15 pF |
| **Maximum Output Drive** | | | | 50 | pF | ≥80% LVCMOS swing, $T_A$ = over temperature, Vdd = 1.5V to 3.3V |
| **Period Jitter** | T_jitt | | 35 | | $ns_{RMS}$ | Cycles = 10,000, $T_A$ = 25°C |

**Notes:**

2. Measured peak-to-peak. Tested with Agilent 53132A frequency counter. Due to the low operating frequency, the gate time must be ≥100 ms to ensure an accurate frequency measurement.
3. Measured peak-to-peak. Inclusive of Initial Tolerance at 25°C, and variations over operating temperature, rated power supply voltage and load.

### Table 2. Pin Configuration

| SMD Pin | SOT23-5 Pin | Symbol | I/O | Functionality |
|---|---|---|---|---|
| 1 | 2, 3 | NC/GND | No Connect | Connect to GND or leave floating. |
| 2 | 1 | GND | Power Supply Ground | Connect to ground. All GND pins must be connected to power supply ground. |
| 3 | 5 | CLK Out | OUT | Oscillator clock output. When interfacing to an MCU's XTAL input, the CLK Out is typically connected to the receiving IC's X IN pin. |
| 4 | 4 | Vdd | Power Supply | Connect to power supply 1.5V ≤ Vdd ≤ 3.63V. Under normal operating conditions, Vdd does not require external bypass/decoupling capacitor(s). Internal power supply filtering will reject more than ±150 mVpp with frequency components through 10 MHz. |

**SOT23-5 (Top View)**

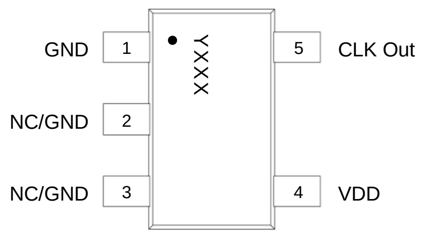



**Figure 1. Pin Assignments**

**SMD Package (Top View)**

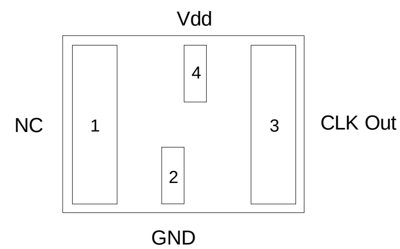



**Figure 2. Pin Assignments**

## System Block Diagram

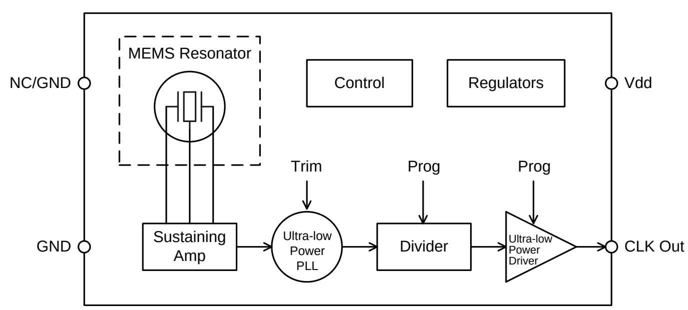



**Figure 3. SIT1630 Block Diagram**

### Table 3. Absolute Maximum

Attempted operation outside the absolute maximum ratings cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

| Parameter | Test Condition | Value | Unit |
|---|---|---|---|
| **Continuous Power Supply Voltage Range (Vdd)** | | -0.5 to 3.63 | V |
| **Short Duration Maximum Power Supply Voltage (Vdd)** | ≤30 minutes, over -40°C to +85°C | 4.0 | V |
| **Short Duration Maximum Operating Temperature Range** | Vdd = 1.5V - 3.63V, ≤30 mins | 125 | °C |
| **Maximum Continuous Operating Life at Temperature Extreme (meeting datasheet limits)** | $T_A$ = -55°C, Continuous<br>Vdd = 1.8V – 3.3V ±10% | 8 | Hours |
| **Human Body Model ESD Protection** | JESD22-A114 | 3000 | V |
| **Charge-Device Model (CDM) ESD Protection** | JESD22-C101 | 750 | V |
| **Machine Model (MM) ESD Protection** | JESD22-A115 | 300 | V |
| **Latch-up Tolerance** | JESD78 Compliant | | |
| **Mechanical Shock Resistance** | Mil 883, Method 2002 | 10,000 | g |
| **Mechanical Vibration Resistance** | Mil 883, Method 2007 | 70 | g |
| **2012 SMD Junction Temperature** | | 150 | °C |
| **SOT23-5 Junction Temperature** | | 150 | °C |
| **Storage Temperature** | | -65°C to 150°C | |

## Description

The SiT1630 is an ultra-small and ultra-low power 32.768 kHz oscillator optimized for battery-powered applications.

SiTime's MEMS oscillators consist of MEMS resonators and a programmable analog circuit. Our MEMS resonators are built with SiTime's unique MEMS First™ process. A key manufacturing step is EpiSeal™ during which the MEMS resonator is annealed with temperatures over 1000°C. EpiSeal creates an extremely strong, clean, vacuum chamber that encapsulates the MEMS resonator and ensures the best performance and reliability. During EpiSeal, a poly silicon cap is grown on top of the resonator cavity, which eliminates the need for additional cap wafers or other exotic packaging. As a result, SiTime's MEMS resonator die can be used like any other semiconductor die. One unique result of SiTime's MEMS First and EpiSeal manufacturing processes is the capability to integrate SiTime's MEMS die with a SOC, ASIC, microprocessor or analog die within a package to eliminate external timing components and provide a highly integrated, smaller, cheaper solution to the customer.

## Frequency Stability

The SiT1630 is factory calibrated (trimmed) to guarantee frequency stability to be less than 20 ppm at room temperature and very tight stability over temperature. Unlike quartz crystals that have a classic tuning fork parabola temperature curve with a 25°C turnover point, the SiT1630 temperature coefficient is extremely flat across temperature.

When measuring the SiT1630 output frequency with a frequency counter, it is important to make sure the counter's gate time is >100 ms. The slow frequency of a 32 kHz clock will give false readings with faster gate times.

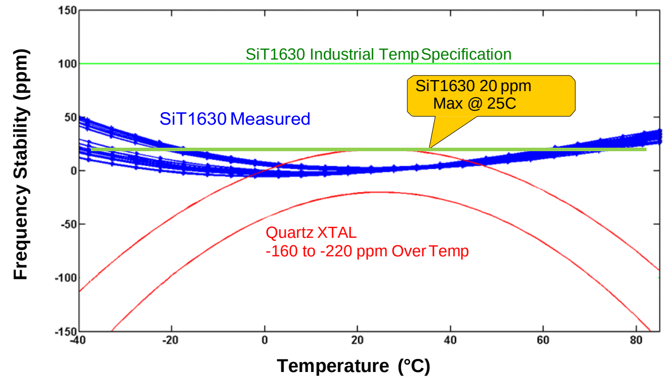



**Figure 4. SiTime vs. Quartz**

## Power Supply Noise Immunity

The SiT1630 is an ultra-small 32 kHz oscillator. In addition to eliminating external output load capacitors common with standard XTALs, this device includes special power supply filtering and thus, eliminates the need for an external Vdd bypass-decoupling capacitor. This feature further simplifies the design and keeps the footprint as small as possible. Internal power supply filtering is designed to reject AC-noise greater than ±150 mVpp magnitude and beyond 10 MHz frequency component.

## Power-up

The SiT1630 starts-up to a valid output frequency within 300 ms (180 ms typ). To ensure the device starts-up within the specified limit, make sure the power-supply ramps-up in approximately 10 – 20 ms (to within 90% of Vdd).

## Typical Operating Curves

**($T_A$ = 25°C, Vdd = 1.8V, unless otherwise stated)**

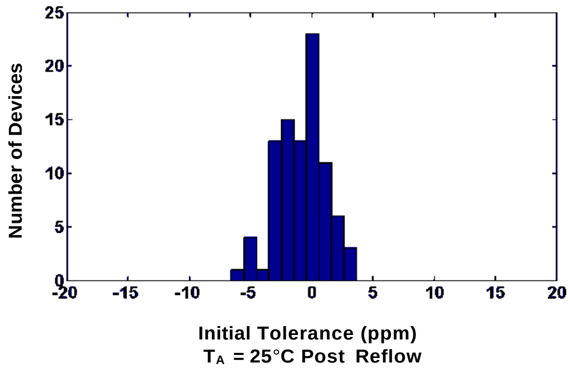



**Figure 5. Initial Tolerance Histogram**

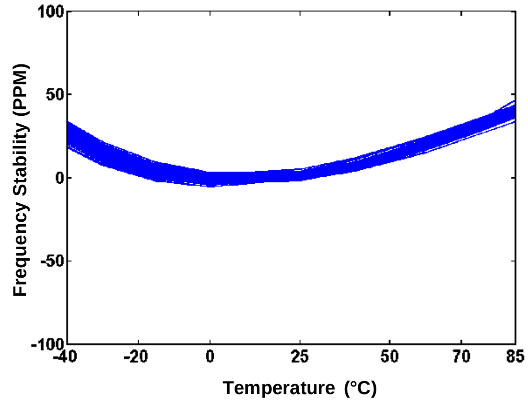



**Figure 6. Frequency Stability Over Temperature**

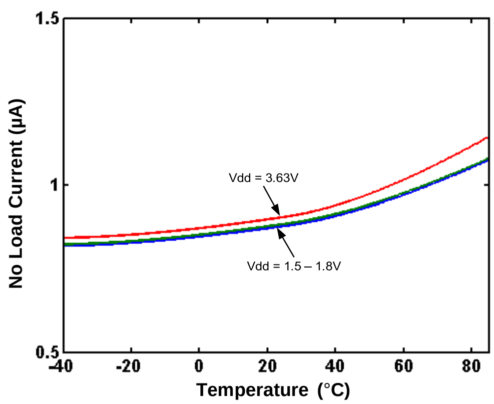



**Figure 7. Supply Current Over Temperature (No Load)**

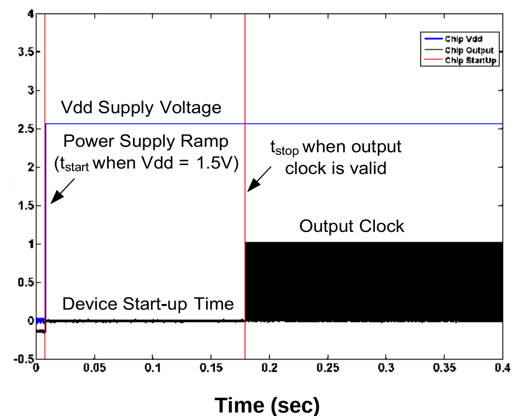



**Figure 8. Start-up Time**

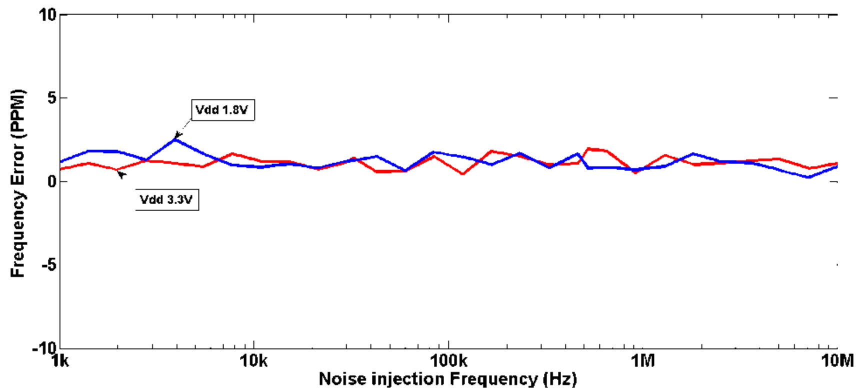



**Figure 9. Power Supply Noise Rejection (±150mV Noise)**

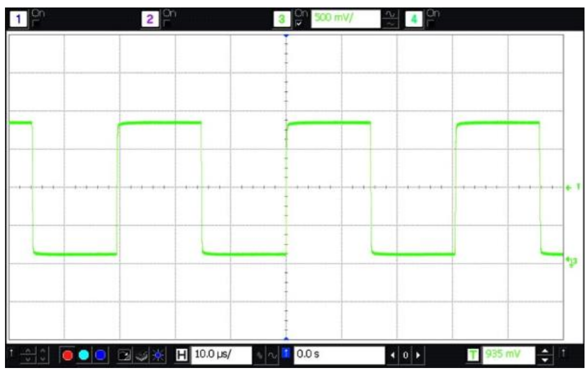
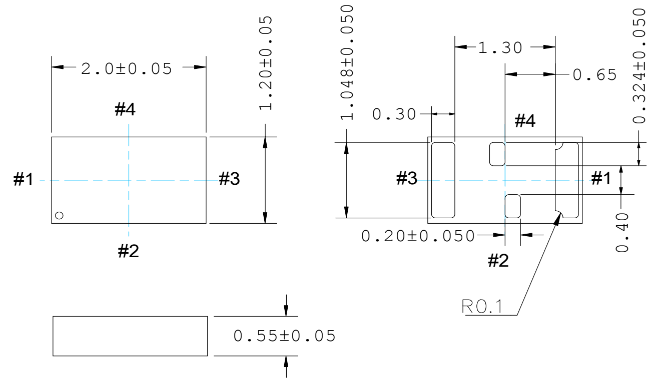
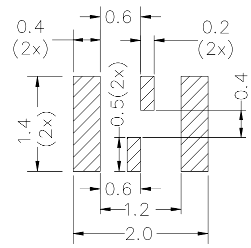
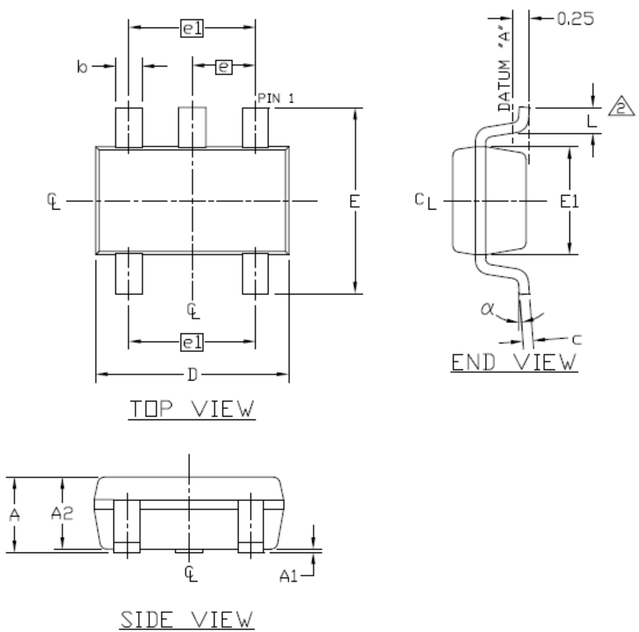
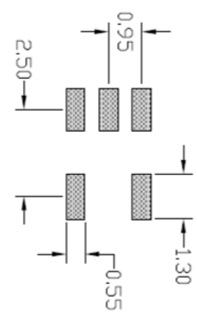


**Figure 10. LVCMOS Output Waveform (Vswing = 1.8V, SiT1630AI-H4-DCC-32.768)**

## Dimensions and Patterns

| Package Size – Dimensions (Unit: mm) | Recommended Land Pattern (Unit: mm) |
|---|---|
| **2.0 x 1.2 mm SMD**  |  |
| **2.90 x 2.80 mm SOT23-5**  |  |









### Table 4. SOT23-5 Dimension Table

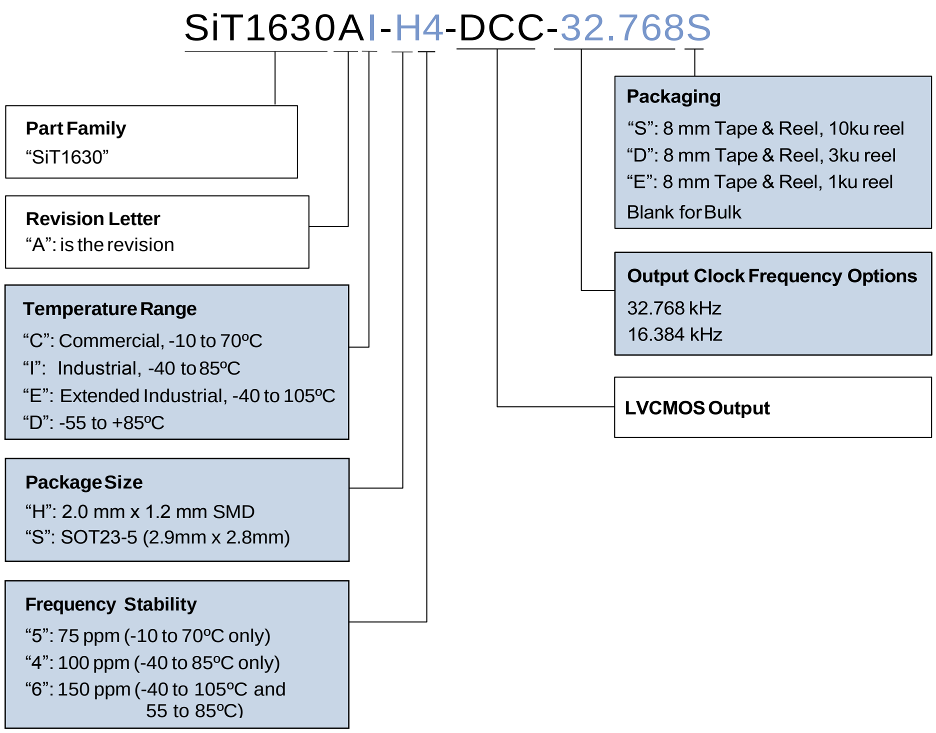
| Symbol | Min. | Nom. | Max. |
|---|---|---|---|
| A | 0.90 | 1.27 | 1.45 |
| A1 | 0.00 | 0.07 | 0.15 |
| A2 | 0.90 | 1.20 | 1.30 |
| b | 0.30 | 0.35 | 0.50 |
| c | 0.14 | 0.15 | 0.20 |
| D | 2.75 | 2.90 | 3.05 |
| E | 2.60 | 2.80 | 3.00 |
| E1 | 1.45 | 1.60 | 1.75 |
| L | 0.30 | 0.38 | 0.55 |
| L1 | 0.25 REF | | |
| e | 0.95 BSC. | | |
| e1 | 1.90 BSC. | | |
| $\alpha$ | 0° | – | 8° |

## Manufacturing Guidelines

1) No Ultrasonic Cleaning. Do not subject the SiT1630 to an ultrasonic cleaning environment. Permanent damage or long term reliability issues to the MEMS structure may occur.
2) For Noisy, high EM environments, we recommend the following design guidelines:
   - Place oscillator as far away from EM noise sources as possible (e.g., high-voltage switching regulators, motor drive control).
   - Route noisy PCB traces, such as digital data lines or high di/dt power supply lines, away from the SiTime oscillator.
   - Add a low ESR/ESL, 0.1uF to 1.0uF ceramic capacitor (X7R) to help filter high frequency noise on the Vdd power-supply line. Place it as close to the SiTime oscillator Vdd pin as possible.
   - Place a solid GND plane underneath the SiTime oscillator to shield the oscillator from noisy traces on the other board layers.
3) For additional manufacturing guidelines and marking/tape-reel instructions, refer to SiTime Manufacturing Notes.

## Ordering Information

Part number characters in blue represent the customer specific options. The other characters in the part number are fixed.



## Table 5. Revision History

| Version | Release Date | Change Summary |
|---|---|---|
| 1.0 | 09/03/2014 | Rev 0.85 Preliminary to Rev 1.0 Production Release<br>Updated start-up time specification<br>Deleted SOT23 package option<br>Added typical operating plots<br>Added maximum output drive specification<br>Added *Manufacturing Guidelines* section |
| 1.1 | 09/03/2014 | Updated start-up time plot in *Typical Operating Curves* section<br>Updated start-up time specification |
| 1.2 | 11/10/2014 | Added additional design-in/mfg guidelines |
| 1.3 | 02/09/2018 | Added SOT23-5 package option<br>Improved max supply current for commercial and industrial temp ranges<br>Improved max start-up time at 85°C<br>Updated start-up time temperature range conditions<br>Updated *Ordering Information* |

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