SiW1502 Radio Modem IC

1. INTRODUCTION

The SiW1502 Radio Modem IC is part of Silicon Wave's Odyssey™ solutions for Bluetooth™ wireless communications. The SiW1502 IC combines a 2.4-GHz radio transceiver and GFSK modem with digital control functions meeting Bluetooth specifications. The SiW1502 IC is designed to work with the Silicon Wave SiW1601 Link Controller IC or other compatible IC to enable production of Bluetooth wireless communication products.

2. FEATURES

- Radio and modem with combined RF analog and digital CMOS circuits on a single integrated silicon chip.
- Fully compliant with Bluetooth Specification 1.0 B.
- Pin-to-pin compatibility with the SiW1501.
- Direct-conversion radio architecture with integrated VCO and frequency synthesizer requiring minimal external components.
- Integrated analog-digital conversion circuits transform I/O signals between the radio and GFSK modem.
- Integrated GFSK modem with digital modulation, channel filtering, AFC, symbol timing recovery, and bit slicer.
- Integrated 0 dBm transmit driver with eight output power levels.
- Direct interface to Bluetooth controller ICs through a low pin-count, digital interface.
- Optimized design for low power consumption, low cost, and small size.

3. APPLICATIONS

The SiW1502 Radio Modem is suitable for all applications requiring a Bluetooth-compliant radio link in a low-power and cost-effective implementation.

- **Cellular Use**: mobile phone handset integration and accessories.
- **Office**: office PCs, notebook PCs, and laser printer interconnection.
- **Personal Data**: PDA, palmtop, and personal organizer communications.
- **Consumer**: digital cameras, handheld game units.
- **Automotive**: hands-free car kit.

4. DESCRIPTION

Figure 1 shows the functional block diagram. During the receive process, the radio signal is taken from a pair of balanced RF I/O pins that feed into the low noise amplifier (LNA). Direct I/Q down conversion and on-chip filtering send the processed I/Q data to the analog-to-digital converter before processing by the GFSK demodulator. Within the demodulator, data detection and timing recovery circuits convert the data for transfer to an external device. The transmit process operates in a similar fashion in reverse order. Digital control functions and a programming interface provide radio modem control and a flexible interface to external Bluetooth link controller ICs.

For efficient power management, each section of the radio may be powered down when not in use. The active circuitry required for the master clock reference and low-power clock used to supply clock signals to external devices is located on the SiW1502.

The transmitted signal is GFSK modulated data that is amplified on the chip to yield a radiated output of 0 dBm. A power control signal for an external amplifier is provided.

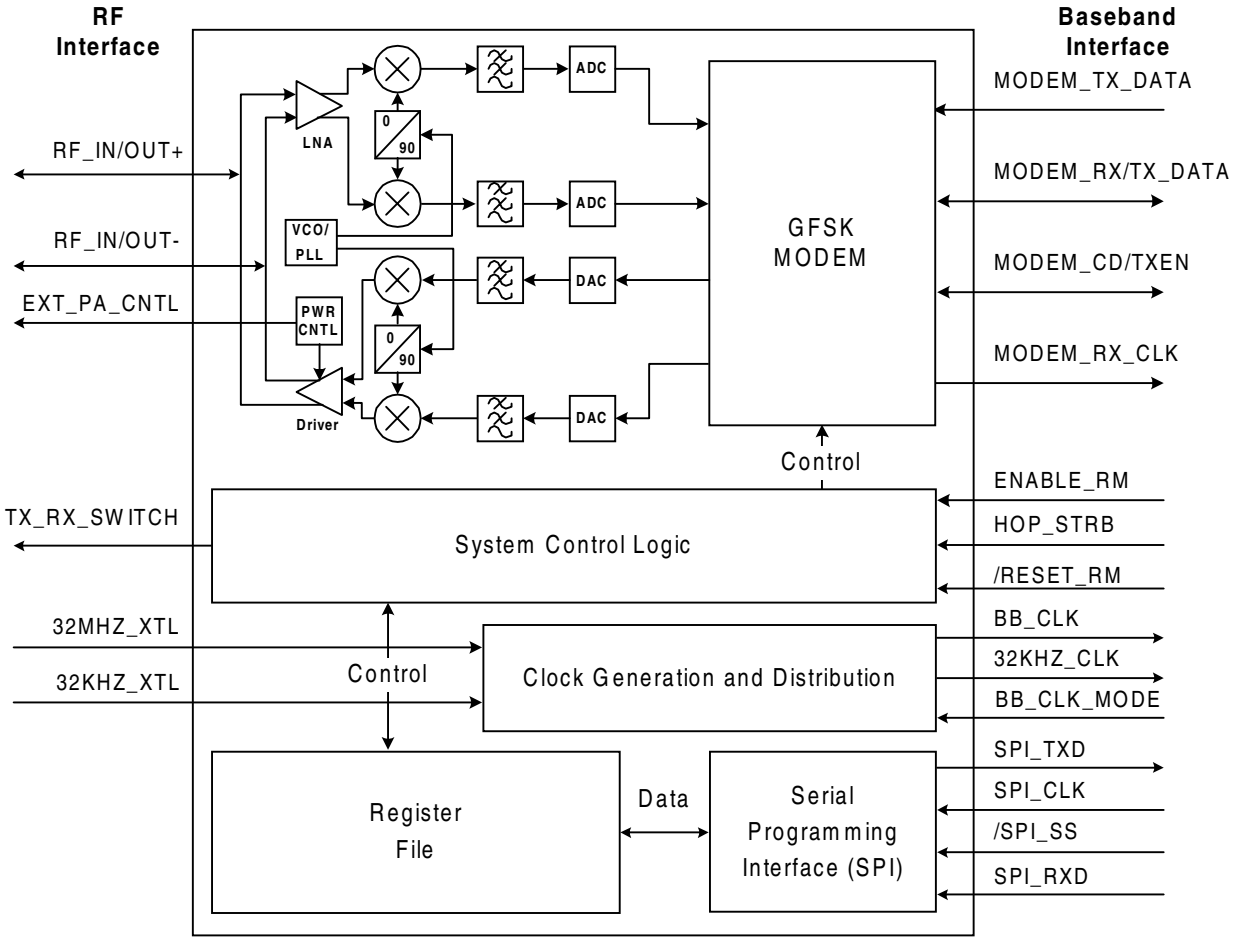


Figure 1: SiW1502 IC Block Diagram

5. PIN DESCRIPTION

The SiW1502 IC's radio and modem interface, the Serial Programming Interface (SPI), and the two clock inputs are required for proper operation.

5.1. Radio Interface

The radio interface provides an antenna connection through external circuitry to transmit and receive the Bluetooth radio signals. Control signals for the external transmit/receive switch and optional power amplifier are available.

NOTE: The RF signals occupy special pin locations on the device package. For an example, please refer to the application circuit in Section 8 on page 15.

External impedance matching and balun circuits are required to complete the interface to the antenna. Please refer to Figure 10 in Section 8 for the recommended external circuit details.

Name	Direction	Description
RF_IN/OUT+	I/O	Positive RF input and output pin.
RF_IN/OUT-	I/O	Negative RF input and output pin.
EXT_PA_CNTL	O	Power control to external power amplifier. This output provides a variable current source that can be used to control the external power amp.
TX_RX_SWITCH	O	Output to select external transmit/receive switch circuit for external PA (20 dBm) configurations. High = Receive Low = Transmit

Table 1: Signal Description

5.2. Modem Interface

The modem interface transfers the Bluetooth data between the SiW1502 and an external controller such as the SiW1601 IC. The programmable interface on the SiW1502 can be set to various operating modes, depending on the desired interface usage. Programming of the interface is done through internal registers. For reference purposes, Table 2 provides a brief description of typical interface modes.

Name	Direction	Description
MODEM_TX_DATA	I	Transmit Data.
MODEM_RX_DATA	I/O	This pin has three possible programmable mode settings (through internal registers): 1. Symbol synchronized received data at 1 MHz. 2. Sliced receive data at 8 MHz (sliced output). 3. Both transmit and receive data for low pin-count mode.
MODEM_CD/TXEN	I/O	Dual function carrier detect and transmit enable. This bi-directional signal can be enabled through internal registers. During transmit, this pin can be used as an INPUT to indicate valid transmit data (TXEN). During receive, this pin can be used as OUTPUT to indicate carrier detect (CD).

Table 2: Modem Interface Signal Description

Name	Direction	Description
MODEM_RX_CLK	O	Receive clock output that is based on the Bluetooth packet data recovered timing of 1 MHz. The output can be optionally disabled.
ENABLE_RM	I	Enables 32-MHz oscillator.
HOP_STRB	I	Signal generated by the SiW1601 IC to indicate the start of TX or RX ramp-up.
BB_CLK	O	Clock output to baseband circuits. Clock is programmable to 1/1, 1/2, 1/3, or 1/4 of the 32-MHz input clock.
/RESET_RM	I	Reset for digital circuits only. State machines and internal registers reset to their default state. This signal is asynchronous input with a minimum pulse width requirement of 10 µs. **NOTE:** When /RESET_RM is active, BB_CLK will be disabled.

Table 2: Modem Interface Signal Description (continued)

5.2.1. Sample Interface Usage with Timing Recovered Receive Data

The interface is configured with separate transmit and receive data lines with the MODEM_RX_CLK at the timing recovered rate of 1 MHz.

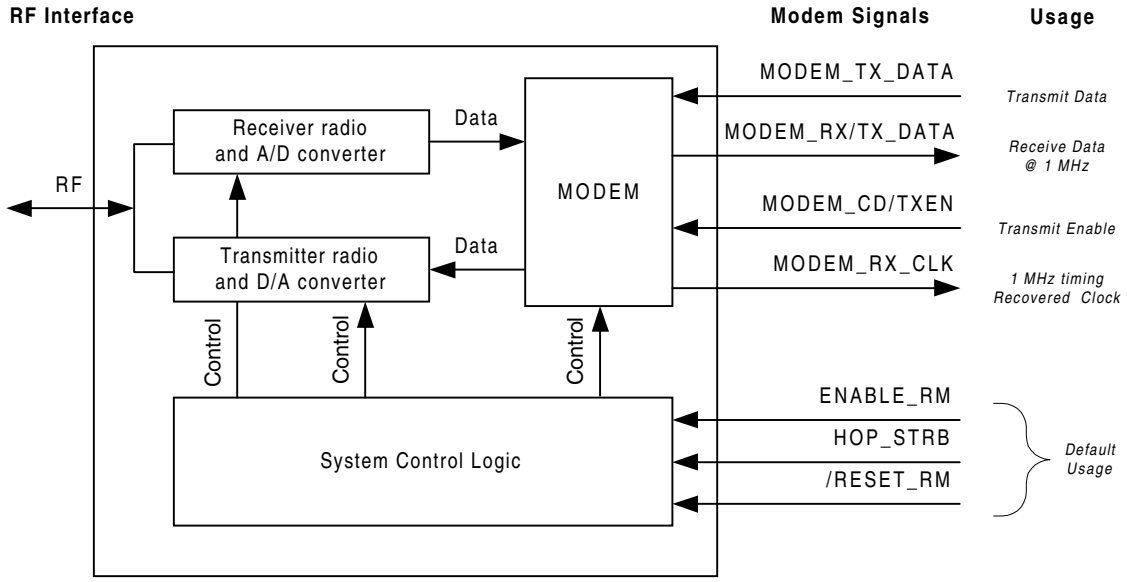


Figure 2: Interface Mode with Separate TX and RX + Symbol Timing

5.2.2. Sample Interface Usage with Minimum I/O

The interface can be configured for bi-directional data on the MODEM_RX/TX_DATA line. During transmit cycles this signal becomes input for TX data. During receive cycles the line becomes an output with receive bit sliced packet data. MODEM_RX_CLK can be disabled and is not required for 8-MHz sliced RX operation.

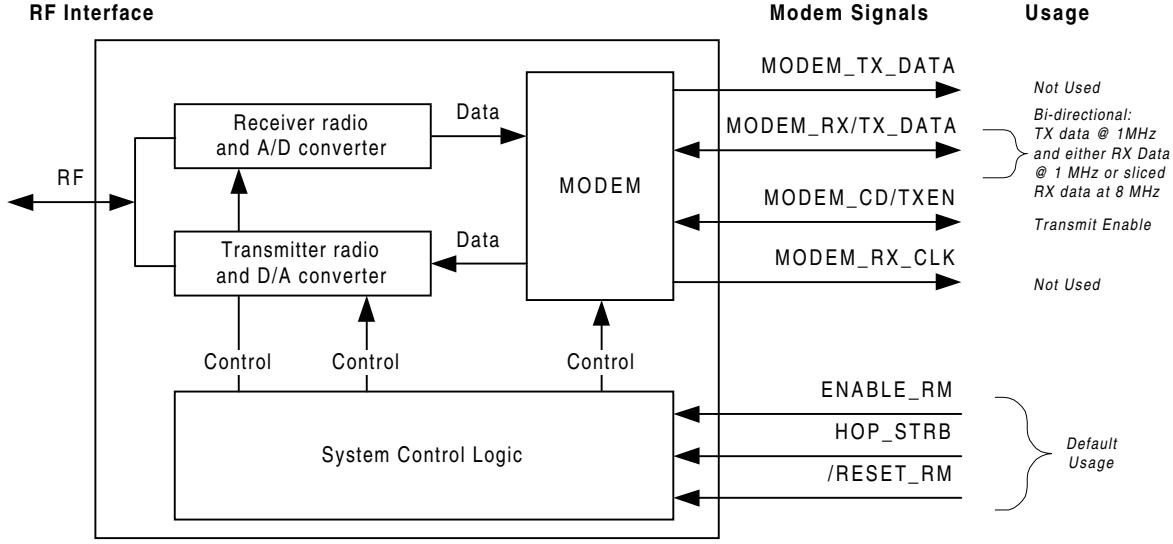


Figure 3: Interface Mode Combined TX and RX with RX Sliced Output

5.3. Clock Signals

The 32-MHz clock is used as a reference for the RF circuits, to synthesize clocks for most of the internal digital circuits, and to supply external processors with timing signals. The 32-kHz clock is used by external circuits during low power modes to conserve system power.

Name	Direction	Description
32KHZ_XTL+	I	32- or 32.768-kHz crystal oscillator out.
32KHZ_XTL-	I	32- or 32.768-kHz crystal oscillator in.
32MHZ_XTL+	I	32-MHz crystal oscillator out.
32MHZ_XTL-	I	32-MHz crystal oscillator in.
32KHZ_CLK	O	32-kHz output.
32M_XTAL_CAP	I	This pin is not currently used. Leave unconnected.
BB_CLK	O	Clock output to baseband circuit. The clock is programmable to 1/1, 1/2, 1/3, or 1/4 of the 32-MHz clock.
BB_CLK_MODE	I	Selects either 8 MHz or 16 MHz for baseband clock (BB_CLK) during system power up and before the internal clock control registers are set by software. “HIGH", the BB_CLK will be set to 16 MHz. “LOW", the BB_CLK will be set to 8 MHz.

Table 3: Clock Signals

5.4. Serial Programming Interface (SPI)

The Serial Programming Interface is used to access the internal registers of the SiW1502 IC. The SPI is a synchronous serial interface that can be clocked to speeds up to 4 MHz. SPI communication uses four signals. /SPI_SS, which selects the SiW1502 for transfer, is active low. Note that /SPI_SS does not have to de-assert and the serial clock does not have to pause after each byte transmission. Figure 4 shows a high-level block diagram of the interface.

Name	Direction	Description
SPI_RXD	I	SPI receive port for write/input.
SPI_TXD	O	SPI transmit port for read/output.
SPI_CLK	I	Clock input used for synchronous data transfers on the SPI bus.
/SPI_SS	I	Slave select input. Selects the SiW1502 IC as the target of a transfer.

Table 4: Programming Interface

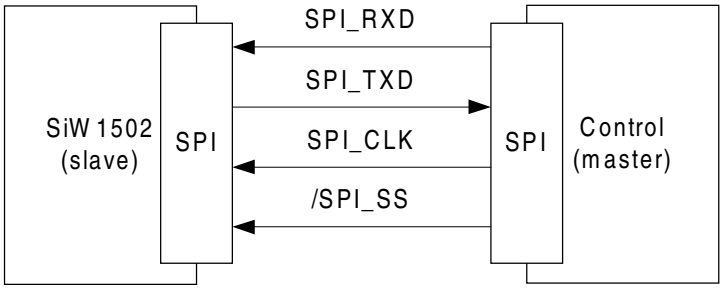


Figure 4: SPI Interface

5.5. Other I/O

The following pins are used by the system for various analog and digital circuits of the radio modem.

Name	Direction	Description
VREFP_CAP	I	Decoupling capacitor for voltage reference for internal A/D converter. Recommended value = 100 nF.
VREFM_CAP	I	Decoupling capacitor for voltage reference for internal A/D converter. Recommended value = 100 nF.
VC_CAP	I	Decoupling capacitor for voltage reference for internal A/D converter. Recommended value = 100 nF.
TUNE_IN	I	Control input for VCO tuning.
CHRG_PUMP	I	PLL charge pump output for external loop filter circuit.
DIGITAL_REG_CAP	I	An external capacitor for the internal digital regulator. Recommended value = 100 nF.
NC	NA	Ground. Used for Manufacturing Test Only.

Table 5: Miscellaneous Signals

5.6. Power and Ground Pins

Separate 3 V supplies are recommended for the digital and analog circuits of the SiW1502.

Name	Direction	Description
VCC	I	Analog 3-V supply inputs.
VDD	I	Digital 3-V supply inputs.
VCC_BATT	I	This input is used to supply the on-chip low-power regulator.
V2.3_OUT	O	Low-power 2.3-V output from internal low power regulator.
GND	I	Ground Pins (3 total). In addition, the package has a ground paddle on the package center to provide better grounding.

Table 6: Power and Ground Pins

5.7. I/O Circuit Configuration

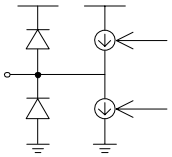
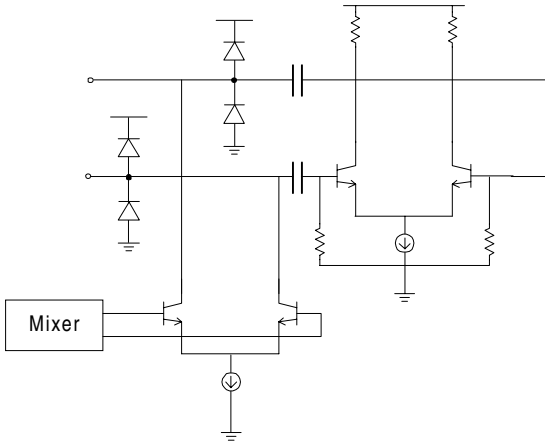
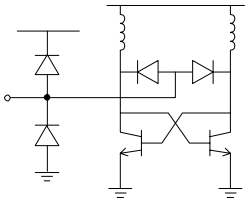
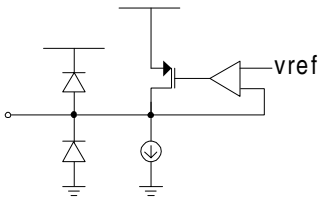
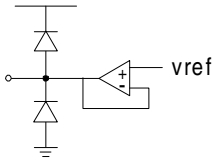
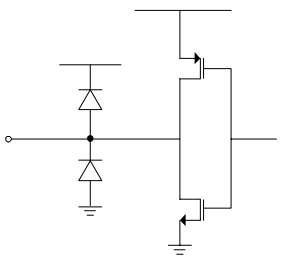
Pin Function	I/O Circuit Configuration	Pin Function	I/O Circuit Configuration
CHRG_PUMP		RF_IN/OUT+ RF_IN/OUT-	
TUNE_IN		V2.3_OUT	
VREFP_CAP		32KHz_CLK	

Figure 5: I/O Circuit Configuration

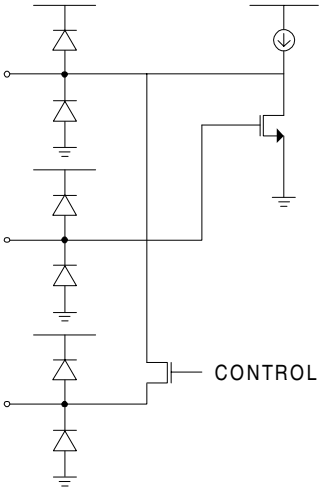
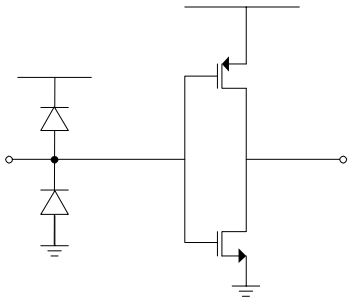
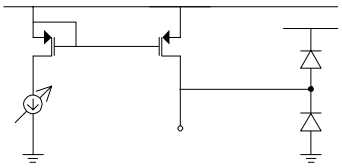
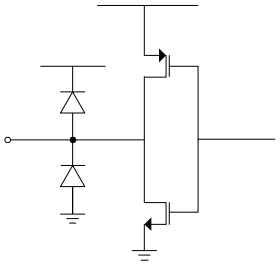
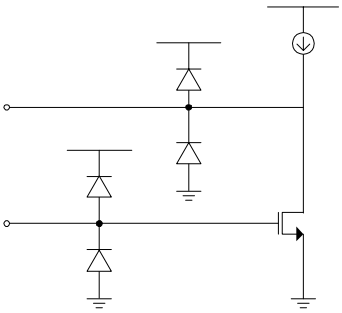
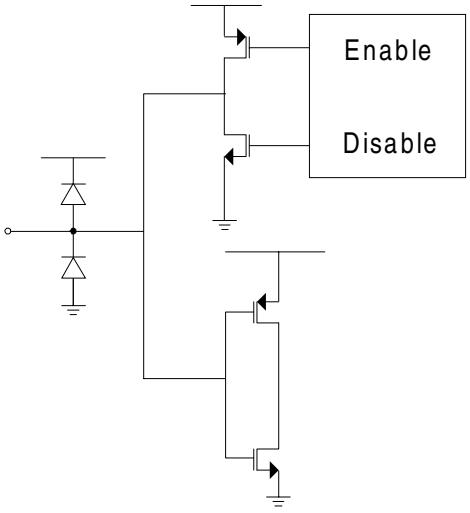
Pin Function	I/O Circuit Configuration	Pin Function	I/O Circuit Configuration
32MHz_XTAL+ 32MHz_XTAL- 32MHz_XTAL_CAP		DIGITAL INPUT	
EXT_PA_CNTL		DIGITAL OUTPUT	
32KHz_XTAL+ 32KHz_XTAL-		DIGITAL I/O	

Figure 5: I/O Circuit Configuration (continued)

6. PIN CONFIGURATION

6.1. 48-Pin MLF Package (SiW1502-NC)

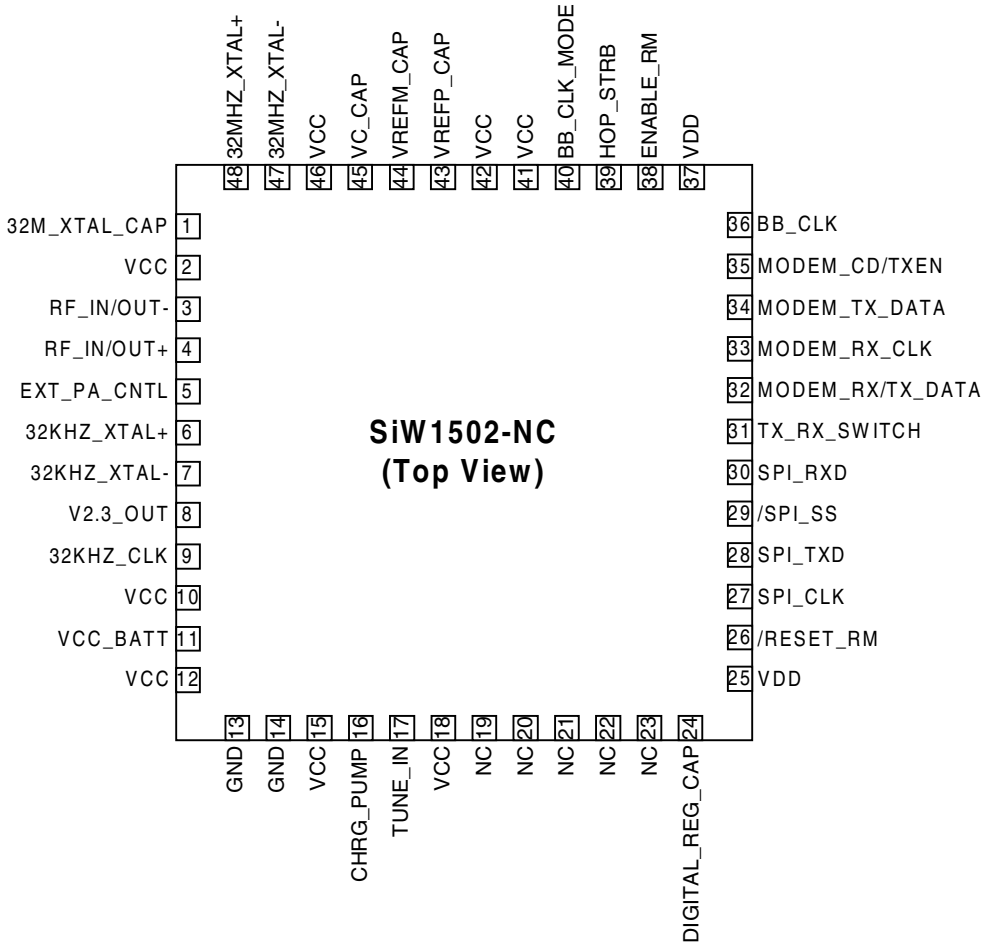


Figure 6: SiW1502-NC Pin Configuration

	Pin Function
1	32M_XTAL_CAP
2	VCC
3	RF_IN/OUT-
4	RF_IN/OUT+
5	EXT_PA_CNTL
6	32KHZ_XTAL+
7	32KHZ_XTAL-
8	V2.3_OUT
9	32KHZ_CLK
10	VCC
11	VCC_BATT
12	VCC
13	GND
14	GND
15	VCC
16	CHRG_PUMP

	Pin Function
17	TUNE_IN
18	VCC
19	NC
20	NC
21	NC
22	NC
23	NC
24	DIGITAL_REG_CAP
25	VDD
26	/RESET_RM
27	SPI_CLK
28	SPI_TXD
29	/SPI_SS
30	SPI_RXD
31	TX_RX_SWITCH
32	MODEM_RX/TX_DATA

	Pin Function
33	MODEM_RX_CLK
34	MODEM_TX_DATA
35	MODEM_CD/TXEN
36	BB_CLK
37	VDD
38	ENABLE_RM
39	HOP_STRB
40	BB_CLK_MODE
41	VCC
42	VCC
43	VREFP_CAP
44	VREFM_CAP
45	VC_CAP
46	VCC
47	32MHZ_XTAL-
48	32MHZ_XTAL+

Table 7: SiW1502-NC Pin Assignment

7. SPECIFICATIONS

7.1. ESD Precautions

These devices are electrostatic sensitive. Devices should be transported and stored in anti-static containers and handled in accordance with MIL-STD-1686. Equipment and personnel contacting the devices need to be properly grounded. Cover workbenches with grounded conductive mats.

7.2. Absolute Maximum Rating

Parameter	Description	Min	Max	Units
T_{ST}	Storage Temperature	-55	+125	°C
VCC, VDD	Supply Voltage (**NOTE:** other than VCC_BATT)	-0.3	3.6	V
ESD	ESD protection – analog/RF pins		500	V
	ESD protection – digital pins		2000	V
Tj	Junction Temperature		125	°C

7.3. Recommended Operating Conditions

Parameter	Description	Min	Max	Units
T_{OP}	Operating Temperature	-20	+85	°C
VCC	VCC analog supply voltage	2.7	3.3	V
VDD	VDD digital supply voltage	2.7	3.3	V
VCC_BATT	Internal voltage regulator supply	2.7	4.8	V

7.4. Electrical Characteristics

7.4.1. DC Specification (T_{op} = 25°C; VDD = 3.0 V)

Parameter	Description	Min	Max	Units
VIL	Input Low Voltage	GND - 0.1	0.2 · VDD	V
VIH	Input High Voltage	0.7 · VDD	VDD	V
VOL	Output Low Voltage	GND	0.1 · VDD	V
VOH	Output High Voltage	0.8 · VDD	VDD	V
IOH	Output High Current		1	mA
IOL	Output Low Current		1	mA
ICC (transmit)	Current consumption during transmit – analog VCC pins		45*	mA
IDD (transmit)	Current consumption during transmit – digital VDD pins		12*	mA
ICC (receive)	Current consumption during receive – analog VCC pins		42*	mA
IDD (receive)	Current consumption during receive – digital VDD pins		18*	mA
ICC (Standby)	Chip current consumption during standby (idle) – analog VCC pins		10*	µA
IDD (standby)	Current consumption during standby (idle) – digital VDD pins		10*	µA

NOTE: * preliminary data.

7.4.2. 2.3 V Regulator Specification (T_{op} = 25°C; VCC_BATT = 2.7 to 4.8 V)

Parameter	Min	Typ	Max	Unit
Output Voltage (IOUT = 10 µA)	2.264	2.3	2.319	V
Line regulation (IOUT = 0 mA; VIN = 2.7 V to 4.8 V)			15	mV
Load regulation (IOUT = 0 µA to 10 µA; VIN = 4.8 V)			8	mV
Dropout voltage (IOUT = 10 µA)		250		mV
Output Absolute Max current			1.0	mA
Quiescent current		2.5		µA
Ripple Rejection at (fRIPPLE = 400 Hz)		-30		dB

7.4.3. EXT_PA_CNTL Output Current for External Power Amplifier Control (T_{op} = 25°C; VCC = 3.0 V)

Internal control register bit setting (register 0x10)	Min	Typ	Max	Unit
111	900	1000	1100	µA
110	577	642	706	µA
101	342	380	418	µA
100	218	242	266	µA
011	131	146	155	µA
010	88	98	108	µA
001	45	50	55	µA
000	23	25	28	µA

7.4.4. Radio specification

Parameter	Description	Min	Max	Unit
Frequency operating range	VCO operating range	2400	2497	MHz

7.4.5. Receiver specification (At Chip RF input; T_{op} = 25°C; VCC = 3.0 V)

Parameter	Description	Min	Typ	Max	Unit
Receiver sensitivity	BER < 0.1%			-80	dBm
Maximum useable signal		-16			dBm
Input IP3	Input 3rd order intercept	-7			dBm
C/I co-channel (0.1% BER)	Co-channel selectivity			11	dB
C/I 1 MHz (0.1% BER)	Adjacent channel selectivity			-3	dB
C/I 2 MHz (0.1% BER)	2nd adjacent channel selectivity			-30	dB
C/I ≥ 3 MHz (0.1% BER)	3rd adjacent channel selectivity			-60	dB
Out-of-band blocking	30 MHz to 2000 MHz	-10			dBm
Out-of-band blocking	2000 MHz to 2399 MHz	-27			dBm
Out-of-band blocking	2498 MHz to 3000 MHz	-27			dBm
Out-of-band blocking	3000 MHz to 12.75 GHz	-10			dBm
Receiver spurious emission	30 MHz to 1 GHz			-57	dBm
	1 GHz to 12.75 GHz			-47	dBm

7.4.6. Transmitter Specification (At Chip RF output; T_{op} = 25°C; VCC = 3.0 V)

Parameter	Description	Min	Typ	Max	Unit
Output RF transmit power	At maximum power output setting	-3	0		dBm
LO leakage	Measured with modulation by all 1's and all 0's		30		dBc
In-band spurious emission (±500 kHz)	Measured in accordance with FCC DA00-705			-20	dBc
In-band spurious emission	2 MHz offset			-20	dBm
In-band spurious emission	> 3 MHz offset			-40	dBm
Out of band spurious	30 MHz to 1 GHz, operating mode			-36	dBm
Out of band spurious	30 MHz to 1 GHz, idle mode			-57	dBm
Out of band spurious	1 to 12.75 GHz, operating mode			-30	dBm
Out of band spurious	1 to 12.75 GHz, idle mode			-47	dBm
Out of band spurious	1.8 GHz to 1.9 GHz			-47	dBm
Out of band spurious	5.15 to 5.3 GHz			-47	dBm

7.4.7. Crystal Requirements — 32 MHz

The 32-MHz crystal should be in fundamental mode and of parallel resonant type.

Parameter	Description	Typ	Unit
Fo	Center Frequency	32	MHz
Frequency tolerance	Worst case over all operating conditions	±20	PPM
ESR	Effective Serial Resistance	<60.	Ω
Co		3	pF
Cl	Load capacitance	12	pF

7.4.8. VCO and PLL Specification

Parameter	Description	Typ	Max	Unit
PLL lock up time			180	µsec
Charge pump output	Charge pump output current	.25		mA
VCO gain	VCO voltage gain	60		MHz/V

7.4.9. Crystal Requirements — 32 kHz

The 32-kHz crystal should be in fundamental mode and of parallel resonant type. Either 32 kHz or 32.768 kHz can be used.

Parameter	Description	Typ	Unit
Fo	Center Frequency.	32 or 32.768	kHz
Frequency tolerance	Worst case over all operating conditions.	±250	ppm
ESR	Effective Serial Resistance	<50	kΩ
Co		1.3	pF
Cl	Load Capacitance	12.5	pF

7.4.10. RF impedance Specification (T_{op} = 25°C; VCC = 3.0 V)

The balanced RF I/O lines of an SiW1502-NCX/NCE were measured using the HP8753 D network analyzer. Figure 7 shows the matching network for the RF I/O port. The network analyzer was connected to pin 3 with pin 4 open and to pin 4 with pin 3 open. Figure 8 and Figure 9 show examples of the measured impedance.

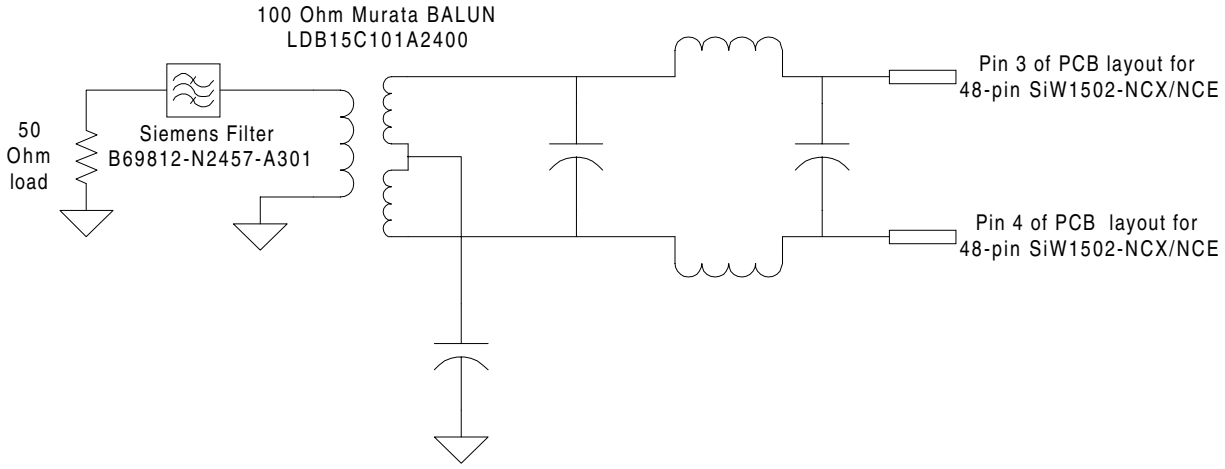


Figure 7: Matching Network for the 48-pin SiW1502-NCX/NCE

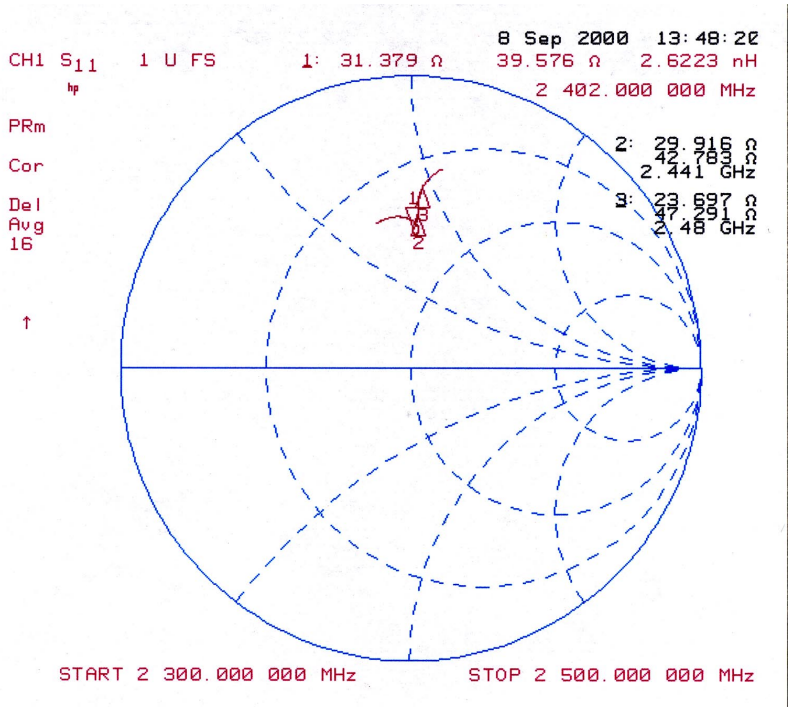


Figure 8: S11 Measurement from Pin 3

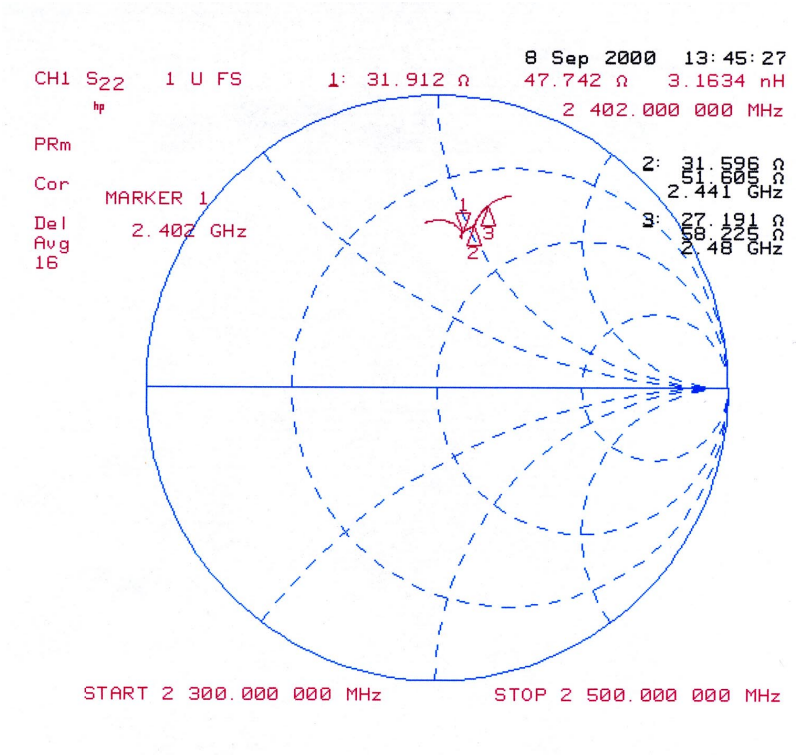


Figure 9: S22 Measurement from Pin 4

8. APPLICATION CIRCUIT

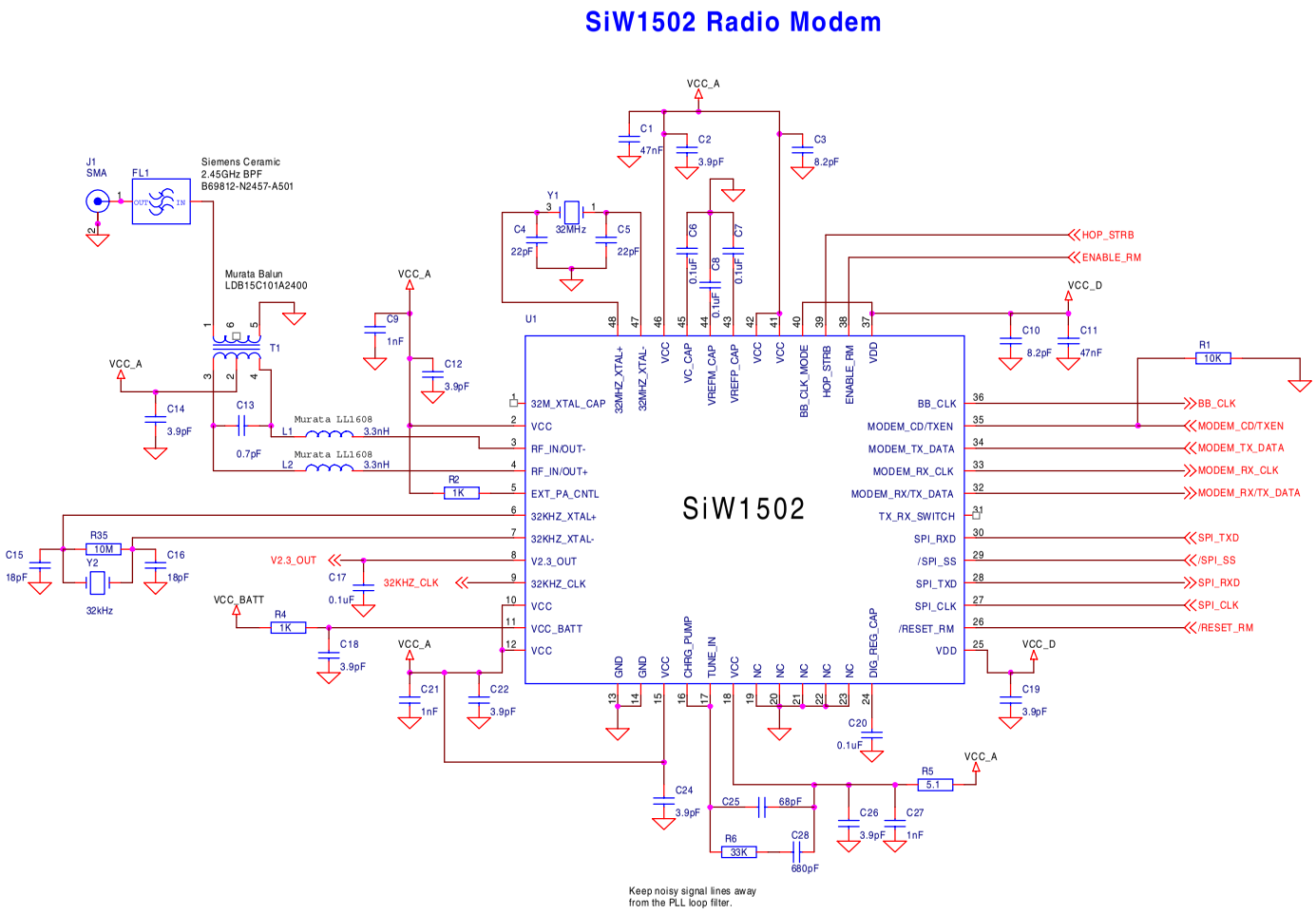
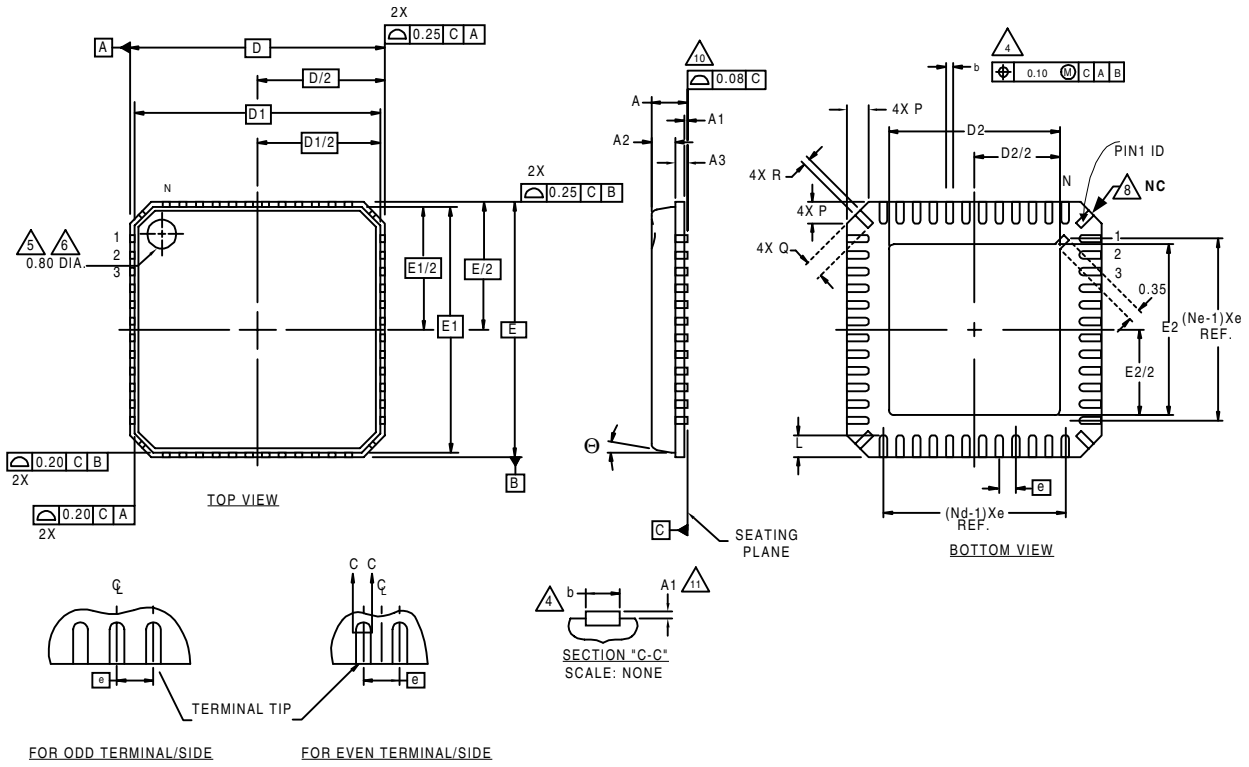


Figure 10: Application of the SiW1502-MC IC

9. PACKAGING AND PRODUCT MARKINGS

Please contact Silicon Wave for the most current packaging and product markings.

9.1. SiW1502 Package: 48 MLF Drawing and Dimensions

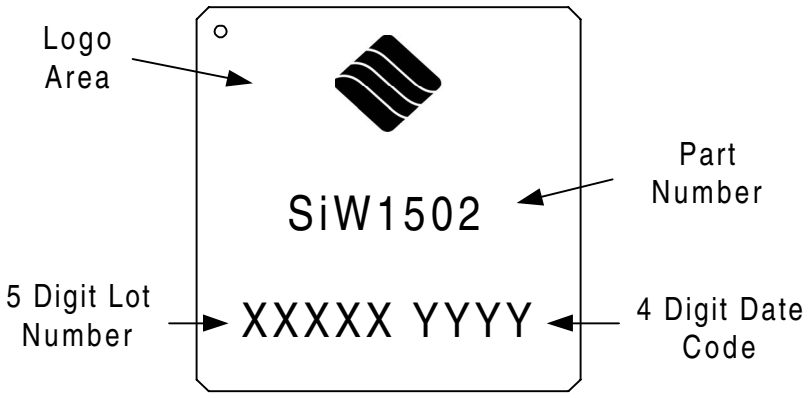


Symbol	Min	Nom	Max	Note
A	-	0.85	1.00	
A1	0.00	0.01	0.05	11
A2	-	0.65	0.80	
A3		0.20 REF.		
B	0.18	0.23	0.30	4
D		7.00 BSC		
D1		6.75 BSC		
D2	4.95	5.10	5.25	
E		7.00 BSC		
E1		6.75 BSC		
E2	4.95	5.10	5.25	
e		0.50 BSC		
L	0.30	0.40	0.45	
N		48		3
Nd		12		3
Ne		12		3
P	0.24	0.42	0.60	
Q	0.00	0.20	0.45	
R	0.13	0.17	0.23	
Θ			12D	

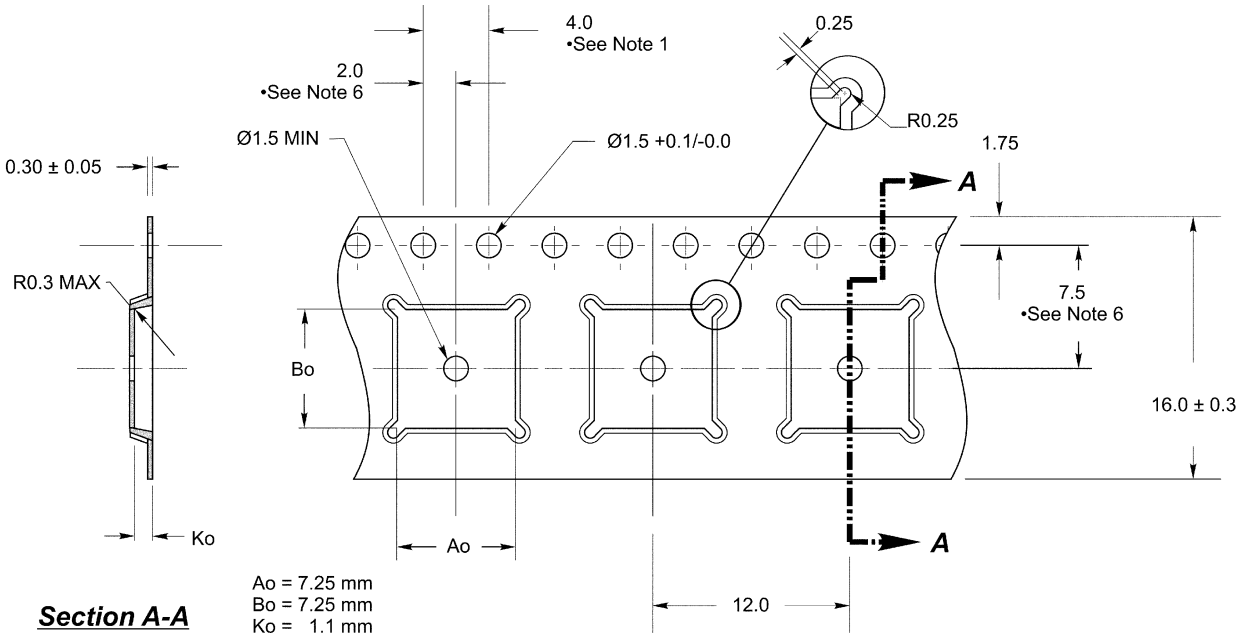
Notes:

1. Die thickness allowable is 0.305 mm (.012 inches) maximum.
2. Dimensioning & tolerances conform to ASME Y14.5M. - 1994.
3. N is the number of terminals.
   Nd is the number of terminals in x-direction and
   Ne is the number of terminals in y-direction.
4. Dimension b applies to plated terminal and is measured between 0.20 and 0.25 mm from terminal tip.
5. The PIN #1 identifier must exist on the top surface of the package by using indentation mark or other feature of package body.
6. Exact shape and size of this feature is optional.
7. All dimensions are in millimeters.
8. The shapes shown on four corners are not actual I/O.
9. Package warpage max 0.08 mm.
10. Applied for exposed pad and terminals. Exclude embedding part of exposed pad from measuring.
11. Applied for terminals only.

9.2. SiW1502 Manufacturing Related Information



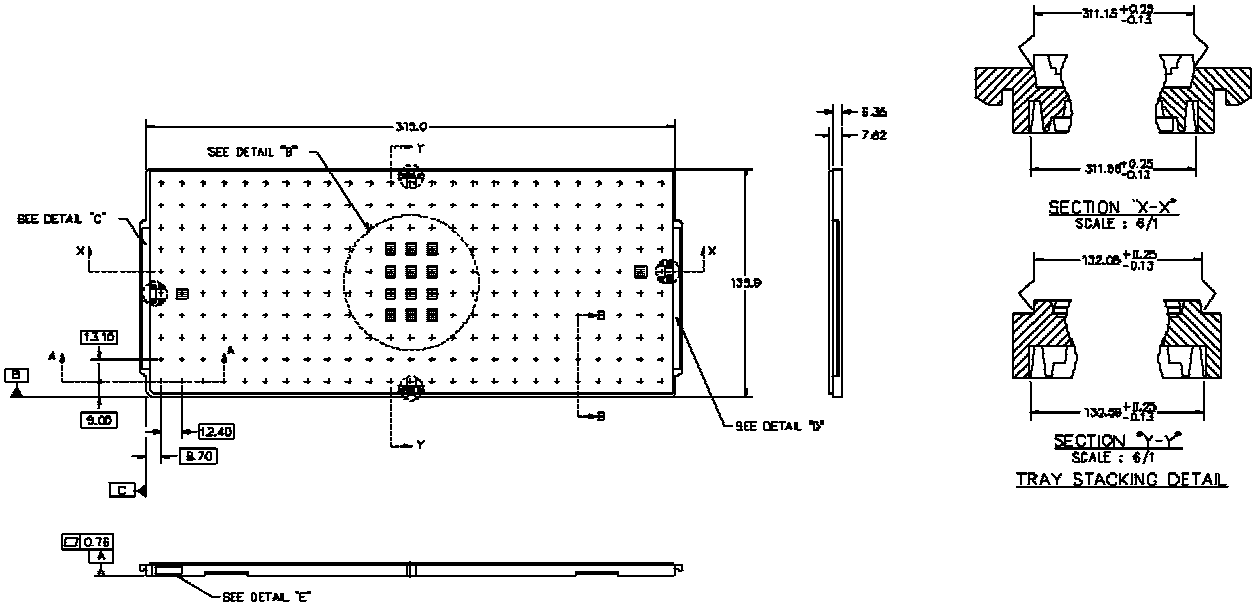
9.3. Tape and Reel Specification

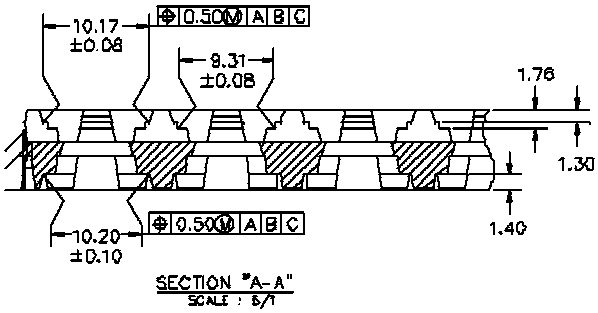


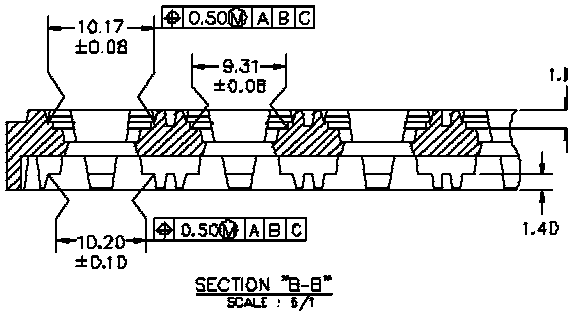
NOTES:

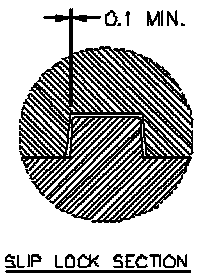
1. 10 sprocket hole pitch cumulative tolerance ±02.
2. Camber not to exceed 1-mm in 100-mm.
3. Material: PS + C.
4. Ao and Bo measured as indicated.
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

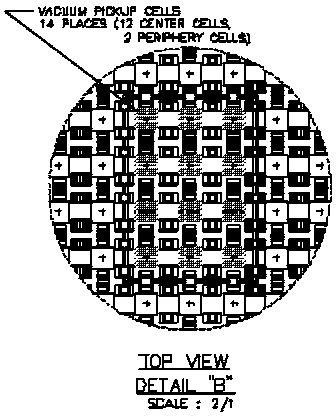
9.4. Taping (Tray) Specification

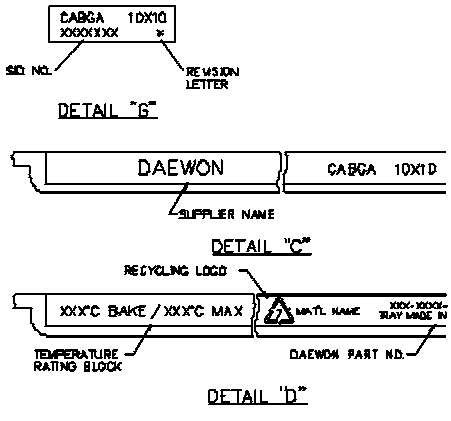




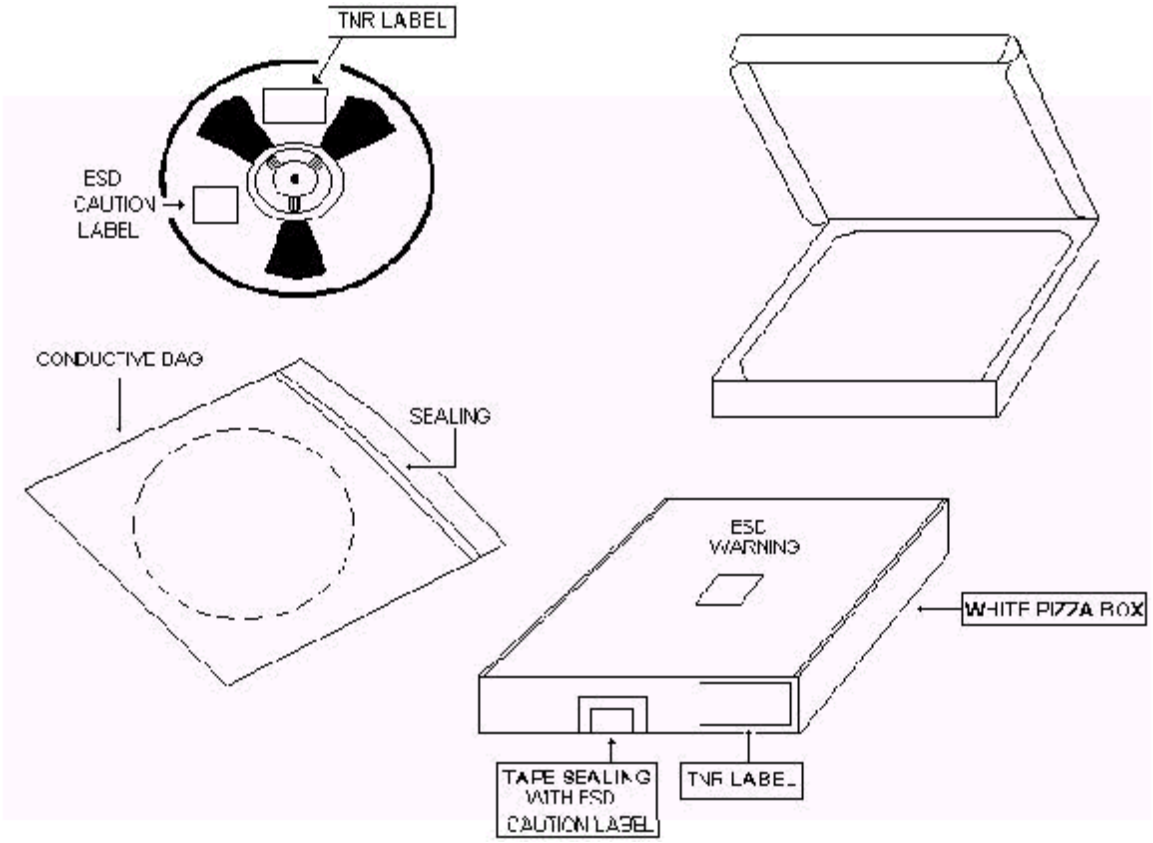




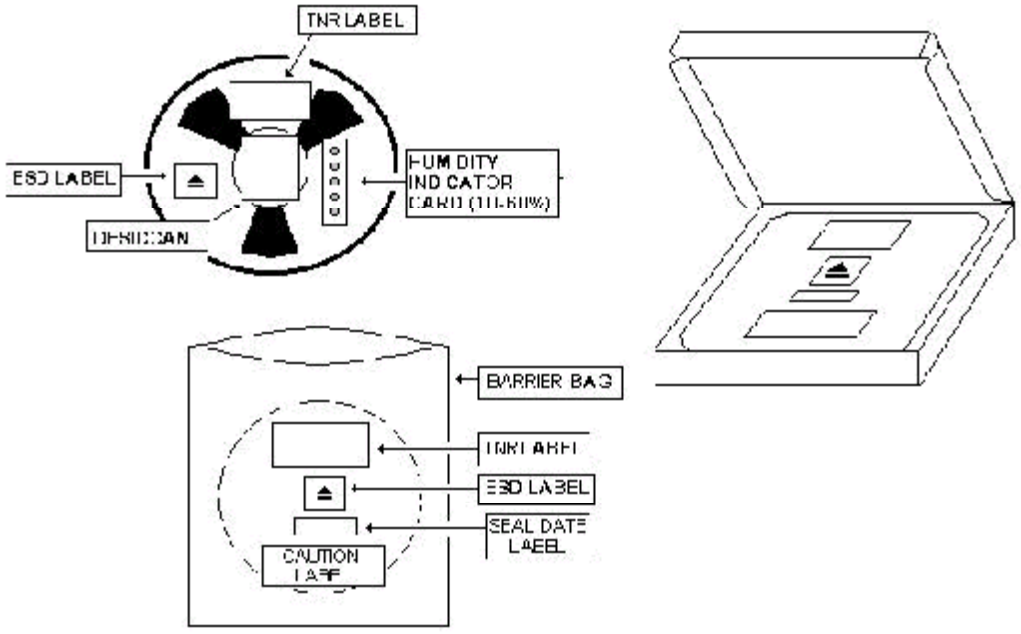




9.5. Packing and Shipping Specification



Dry packing requirement (AWW 001-0531-2247).



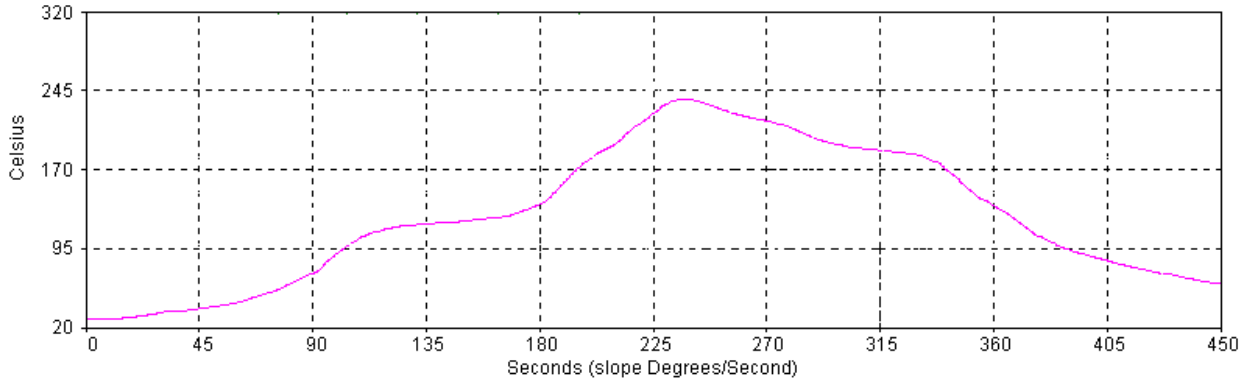
9.6. Manufacturing Locations

Procedure	Location
Wafer	Asia
Assembly	Anam, Korea
Final Test	Anam, Korea
Shipping	Anam, Korea

10. ADDITIONAL INFORMATION

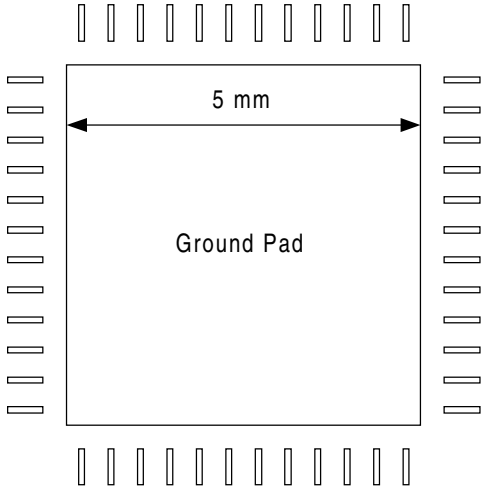
10.1. Recommended Solder Reflow Profile

	Peak	Max Falling Slope	Time Between 100/150	Total Time Above 183	Total Time Above 235
1 MLP64B	237.6	-2.02	81.61	132.80	12.00



10.2. Solder Pad Design

In order to provide better grounding to the SiW1502 IC, a ground pad should be incorporated on the PCB within the footprint of the package corresponding to the exposed metal pad on the package. The area should be at least 5-by-5-mm. An array of via's is recommended in the ground pad to connect the PCB ground.



11. ORDERING INFORMATION

Part Number	Ordering Quantity
SiW1502-NC	476 pcs. per tray
SiW1502-NC-TR	1000 on a 7" reel, 2500 on a 13" reel
SIW1601-PC	360 pcs. per tray

Silicon Wave, Inc.
6165 Greenwich Drive
Suite 200
San Diego, CA 92122

www.siliconwave.com
+1.858.453.9100 *tel*
+1.858.453.3332 *fax*
+1.888.293.6650 *toll free*