APPLICATION NOTE	First Edition 5/21/2008	Written By Engineering DIV Kelley
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Type No **T-55264GD057J-FW- & T-55265GD057J-LW-Series 320RGB x 240TFT Graphic Displays**		Approved By Customer

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REVISION HISTORY

REV	DATE	PAGE	COMMENT

1.0   REFERENCES

(a) T-55264GD057J-FW-ABN LCD Module Technical Specification REV 1 dated 4/25/2008
http://www.optrex.com/SiteImages/PartList/SPEC/55264AB.pdf

(b) T-55265GD057J-LW-ABN LCD Module Technical Specification REV 1 dated 4/15/2008
http://www.optrex.com/SiteImages/PartList/SPEC/55265AB.pdf

2.0   DESCRIPTION

2.1. This application note provides guidance for interfacing, programming, and using the T-55264 and T-55265-series displays. This document, along with the LCD module specification, references (a) and (b), provides the application information needed design the display into electronic products. This document IS NOT INTENDED to be the sole source of guidance for using the display.

2.2. The LCD module drawing provides size and information for the connector(s) built in the product. The drawing does not provide the source for flexible printed circuits (FPC) that mate to the zero-insertion force (ZIF) connectors since there are many potential sources available. The drawings are provided within references (a) and (b).

2.3. The LCD Module Technical Specification provides electrical and optical performance specifications, cosmetic specifications, and qualification information.

2.4. The T-55264- & T-55265-series displays include the following components:

- 262K Color thin film transistor (TFT) liquid crystal display panel.

- Either a white cold cathode fluorescent lamp (CCFL) backlight [T-55264] or white light emitting diode (LED) backlight [T-55265].

- TFT timing controller, source drivers and gate driver.

- DC-to-DC Boost Circuits to generate gate and source driver voltages. The displays require a single 3.3 VDC source.

2.5. The displays require additional components to integrate into the end unit:

- CCFL backlight inverter (T-55264) or LED power supply / LED driver (T-55265).

- Interconnect flat flex cable or flexible printed circuit.

- Mounting screws

- LCD controller.

3.0   PRINCIPLES OF OPERATION

3.1. A microprocessor writes to an LCD controller to configure it for operation. The configuration data tells the device the polarity and sequencing of control signals and their timing. The microprocessor then writes or ports image data to the LCD controller for storage in RAM. The controller reads the RAM and automatically generates the control signals to write data to the display. There are 18 data bits in RAM for each pixel location (6 red, 6 green, and 6 blue). 18 data bits are latched into the display with each pixel clock.

The controller generates control signals to tell the display when to begin writing a new line (HSYC) and when to start writing a new page (VSYC). The DENA signal controls the horizontal position of the data on the page.

The source driver in the display takes the data and performs a digital to analog voltage conversion on the groups of six bits. The corresponding drive voltage controls the twist of the liquid crystal and thus the light passage through it.

With 6 bits of data, 64 gray shades are generated for each red, green, and blue sub-pixel, within a pixel. There are 262 K combinations or red, green, and blue shades possible.

3.2. TFT displays use TN-mode liquid crystals. Temperature compensation is not required as for passive LCDs.

3.3. LCD controllers are often built-in microprocessors. .This design is often found on ARM-based devices, high end microprocessors, and system on a chip (SOC) designs.

Sources for external LCD controller include:

Seiko Epson LCD Controllers

Fujitsu Graphics Controllers

Toshiba Automotive Graphics Controllers

4.0   MECHANICAL

4.1. The display is attached via 4 screws on the rear side. The screws self-tap into the polycarbonate internal frame.

The recommended screw sizes are:

DISPLAY	THREAD DIAMETER & TYPE	MAX DEPTH	MAX TORQUE
T-55264	M3, self-tapping	4.0 mm	0.5 to 0.56 N-m (4.4 to 5.0 pound-inch)
T-55265	M3, self-tapping	9.3 mm	0.5 to 0.56 N-m (4.4 to 5.0 pound-inch)

4.2. The connection between the display and the customers PCB is via a flexible printed circuit (FPC) or flat flexible cable (FFC). The thickness of of the FPC / FFC is set by the connector mounted to the display. The FPC / FFC must be 0.3 mm thick at the contact point stiffener.

CAUTION

THE FPC / FFC MUST NOT TIGHTLY BEND AND PERMANENTLY DEFORM THE COPPER TRACES (FORM A CREASE).

During bending, the inner side of the copper traces are compressed while the outer side is placed in tension; fracturing the trace and electrically opening the circuit. The minimum bend radius should be 10 times the thickness of the FPC / FFC to prevent permanent deformation.

Typical FPC are rated 0.3 mm thick at the contact point stiffener. This is not the bending point. Most FPC are thinner away from that point. For an FPC that is 0.120 mm thick in the bend area, the minimum bend radius is 1.2 mm for a 90 degree bend. A 180° bend requires a larger radius to prevent creasing. Small radius bends greater than 90° should be formed ONCE and not unbent.

5.0   ELECTRICAL

5.1. INTERFACE CONNECTION & VOLTAGES

5.1.1. The displays interface via a 33-conductor FPC / FFC to ZIF connector mounted to the display.

Kyocera Elco 08-6210-033-340-800 – 33 pin, zero insertion force (ZIF), right angle, bottom contact, surface mount, 0.5 mm pitch FPC, 0.30 mm thick, with front slide lock.

5.1.2. A major design consideration for the customer's PCB is the contact location in the mating connector. The display ZIF has contacts on the bottom (PCB) side. The designer must take FPC bending and connector location into account and choose the correct contact location when selecting connectors. If the FPC exits straight from the display with no bends, then a top contact connector is required. If a single 180-degree bend is made, then a bottom

contact connector is required. Sources for compatible connectors, in addition to the AVX Elco, are:

Molex 54132-3397 – 33 pin, zero insertion force (ZIF), right angle, bottom contact, surface mount, 0.5 mm pitch FPC, 0.30 mm thick, with front slide lock.

Omron XF2M-3315-1A – 33 pin, zero insertion force (ZIF), right angle, top & bottom contact, surface mount, 0.5 mm pitch FPC, 0.30 mm thick, with rear rotary lock.

These part numbers are presented for information only. Optrex has not tested the performance and reliability of these connectors and makes no warranty to their fitness for use. Please note that any connector matching the FPC pitch characteristics and mating tolerances may be used.

5.1.3. Sources for the FFC / FPC include:

http://www.parlex.com/products/ffc.php

http://www.circoflex.com/

http://www.innovative-circuits.com/index.htm

These manufacturers are presented for information only. Optrex has not tested the performance and reliability of their products and makes no warranty to their fitness for use. Please note that any FPC must match the connector pitch characteristics and mating tolerances.
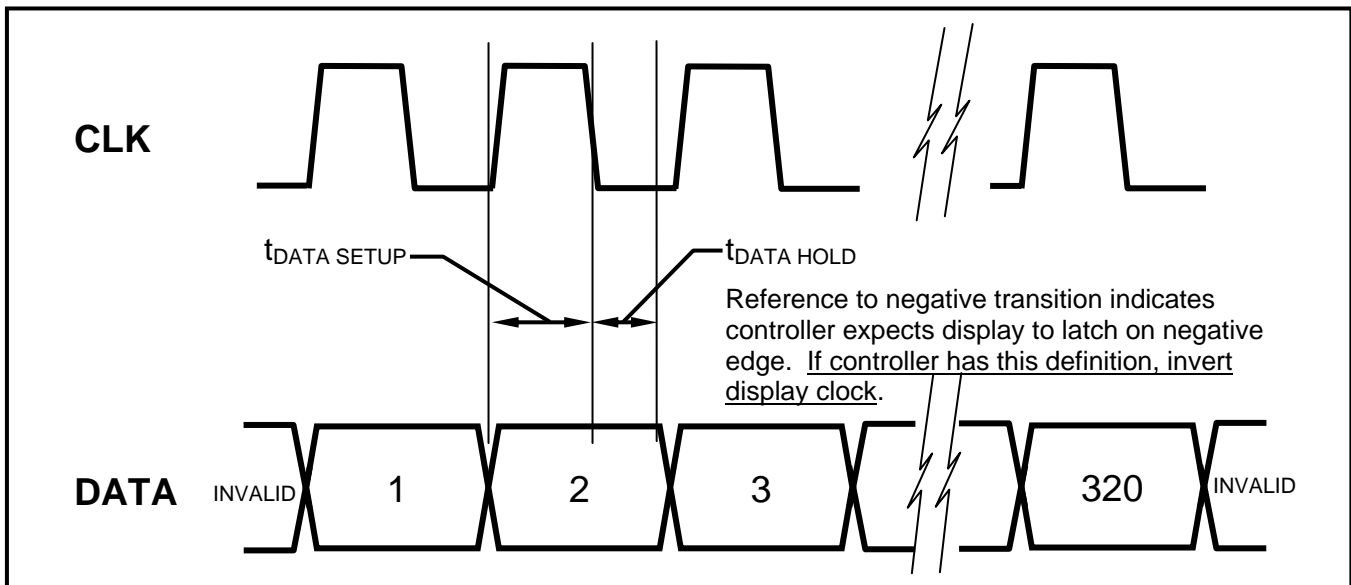
5.2. SIGNAL TIMING

5.2.1. The timing values needed to operate the display are programmed into the LCD controller registers. Please consult references (a) and (b) for the values. Please note timing characteristics are dependent upon the TFT timing controller (TCON) used. This means the timing for a 320RGB x 240 TFT can vary between manufacturers.

5.2.2. T-55264 and T-55265 latch data on the rising edge of the clock. This may differ from the timing output of the LCD controller design.

OPTREX HIGHLY RECOMMENDS CAREFUL STUDY OF THE LCD CONTROLLER SPECIFICATION TO DETERMINE THE TIMING IT EXPECTS THE DISPLAY TO USE.

FIGURE 1 shows a timing diagram from an LCD controller. This definition shows the LCD controller expects the display to latch data on the negative clock edge. With this definition, the clock signal requires inversion to meet the display data setup and hold time requirements. The Seiko Epson S1D13706 controller has this definition.

FIGURE 1 -- CLOCK / DATA REFERENCE

CLK

$t_{DATA\ SETUP}$ $t_{DATA\ HOLD}$

Reference to negative transition indicates controller expects display to latch on negative edge. If controller has this definition, invert display clock.

DATA   INVALID   1   2   3   320   INVALID

Inverter SN74AUPG06 (low-power single inverter buffer/driver with open drain outputs) has been successfully used with the T-55264 & T-55265.

FIGURE 2 shows the timing for a Seiko Epson S1D13706 LCD controller. This controller expects the display to latch the data on the negative clock edge (RED line). Note the clock negative edge occurs in the middle of the data (GREEN line). The vertical dashed lines show the data setup time for the display is about 6 nS which violates the timing and the display cannot sync up to the image data.
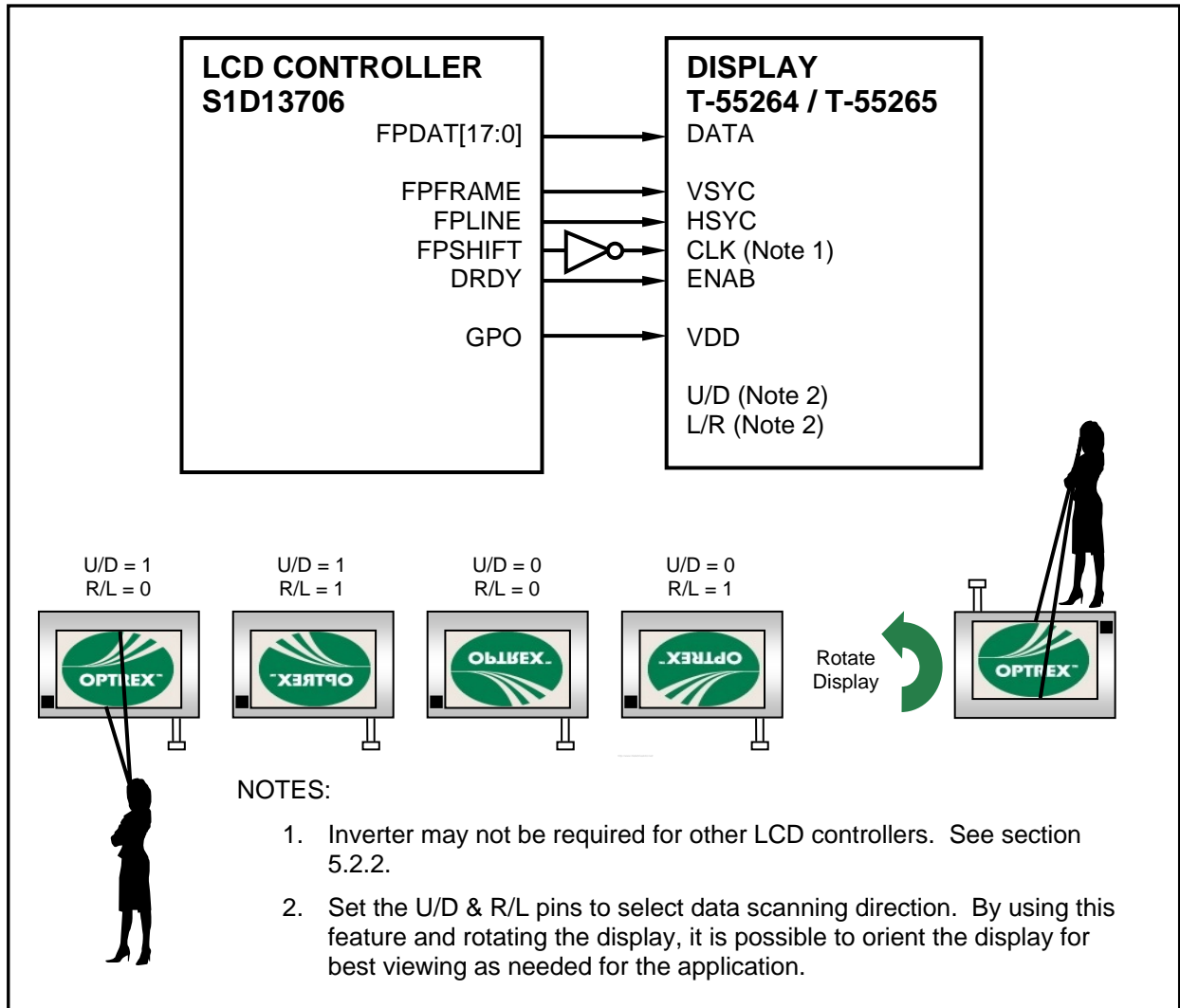
The inverted clock (PURPLE line) has about 75 uS of setup between the positive edge of the clock and data and does operate correctly.

FIGURE 2 -- S1D13706 CLK TO DATA WITH CLOCK & INVERTED CLOCK
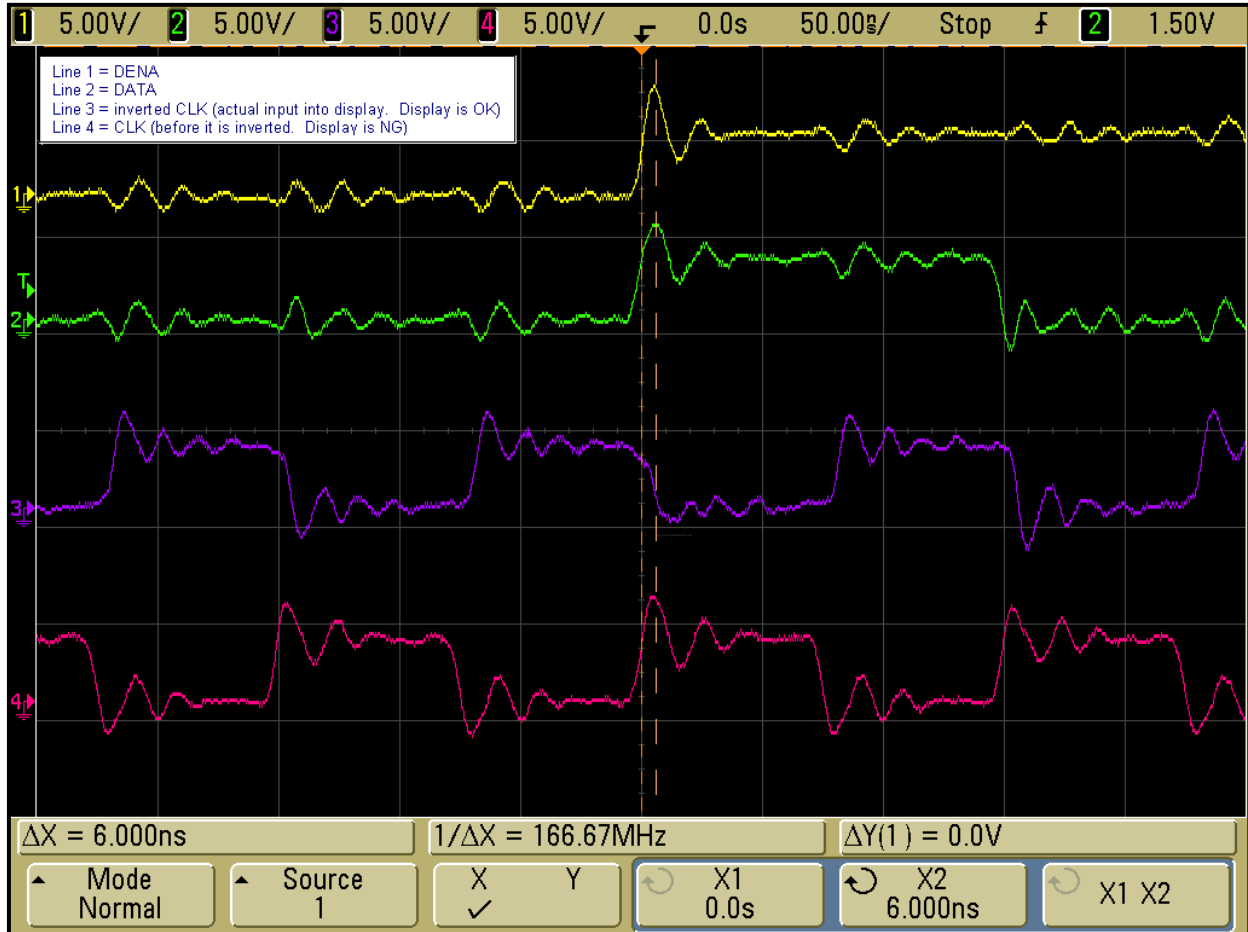
5.3. ELECTRICAL CONNECTIONS TO LCD CONTROLLER

FIGURE 3 -- T-55264 / T-55265 INTERFACE CONNECTIONS

LCD CONTROLLER S1D13706

FPDAT[17:0] → DATA

FPFRAME → VSYC
FPLINE → HSYC
FPSHIFT → CLK (Note 1)
DRDY → ENAB

GPO → VDD

DISPLAY T-55264 / T-55265

U/D (Note 2)
L/R (Note 2)

U/D = 1
R/L = 0

U/D = 1
R/L = 1

U/D = 0
R/L = 0

U/D = 0
R/L = 1

Rotate Display

NOTES:

1. Inverter may not be required for other LCD controllers. See section 5.2.2.

2. Set the U/D & R/L pins to select data scanning direction. By using this feature and rotating the display, it is possible to orient the display for best viewing as needed for the application.

5.4. The display bezel is internally connected to ground. There is no need for a chassis ground.

5.5. T-55264 CCFL BACKLIGHT

5.5.1. The T-55265 backlight uses a JST BHR-03VS-1 connector. This is a wire to board, disconnectable, crimp pin connector using the BH housing with three pins at 4.0 mm pitch. The mating connector is:

JST SM03(4.0)B-BHS-1-TB – a 3-pin surface-mount, right-angle, shrouded pin header with 4.0 mm pitch. The housing is polarized to prevent improper insertion.

The "03" indicates three circuits are populated and the "(4.0)" indicates pin pitch.

5.5.2. The customer must supply an inverter of correct rating to drive the backlight. The following are inverter sources:

TDK CXA-0490 – DC to AC inverter, 12 V input, dimming, with open lamp protection and matching CCFL output connector.

TDK CXA-L10L – DC to AC inverter, board-mount, 5 /12 V input, non-dimming, with pin connections.

Microsemi LXMG1617A-05-41 – DC to AC inverter, 5 V input, dimming, with open lamp & short circuit protection, programmable current limiting and matching CCFL output connector.

Microsemi LXMG1612-12-01 – DC to AC inverter, 12 V input, dimming, with open lamp & short circuit protection, programmable current limiting and matching CCFL output connector.

ERG 8M Class -- DC to AC inverter, 5 or 12 V input, dimming, and matching CCFL output connector. ERG utilizes standard inverter designs and customizes the magnetics to the desired output characteristics.

5.5.3.   The backlight drive voltage should be energized after the LCD is configured and placed in operation to hide optical effects caused by startup with undefined data in the RAM. Likewise, the backlight should be powered OFF before the the display during shutdown.

5.6. T-55265 LED BACKLIGHT

5.6.1.   The T-55265 backlight uses a JST SHL connector. This is a wire to board, 1 mm pitch, crimp pin connector using the SHLP-6 housing. The mating connector is a 6-pin header.

JST SM06B-SHSL-TF – 6-pin, 1.0 mm pitch top entry, shrouded header.

The mechanical drawing schematic shows resistors; these are populated with zero ohm values. The designer must limit drive current.

5.6.2.   The backlight power supply can be designed to implement fixed luminance or dimming via pulse width modulation techniques. Since there are three individual series LED circuits, it is best to drive each individually with a current controlled source.

DO NOT USE A CONSTANT CURRENT DRIVE SOURCE WITH THE LED STRINGS TIED IN PARALLEL. IF ONE LED FAILS, THE CURRENT SOURCE WILL DRIVE THE REMAINING OPERATIONAL STRINGS WITH EXCESSIVE CURRENT AND FAIL THE BACKLIGHT.

If the designer wishes to tie all three LED strings in parallel, use a constant voltage source.

With a voltage source, the designer must limit drive current to protect the LEDs, the current-limiting resistor must meet the criteria of EQUATION 1 and have adequate power rating.

EQUATION 1 – CURRENT LIMITING RESISTOR CALCULATION

$$\frac{V_{SUPPLY} - V_f}{R} \leq I_f$$

The values of V_f and I_f are found in Section 7 of the LCD Module Technical Specification. PWM techniques may be used to control luminance. The high temperature current derating curve must be followed.

5.6.3.   LED driver ICs are a good option for driving the backlight. These ICs provide DC to DC boost, dimming, and current limiting capability while minimizing external component size and count. There are numerous sources found by searching "White LED driver" on the Internet.

5.6.4.   The backlight drive voltage should be energized after the LCD is configured and placed in operation to hide optical effects caused by startup with undefined data in the RAM. Likewise, the backlight should be powered OFF before the the display during shutdown.

6.0 SOFTWARE

6.1. The T-55264 and T-55265 displays are not programmable. There is no software programming for the display itself.

6.2. An LCD controller is required to drive the display. The following timing definition and register values apply for a Seiko Epson S1D13706 LCD Controller.

FIGURE 4 -- SEIKO EPSON S1D13706 TIMING DEFINITIONS
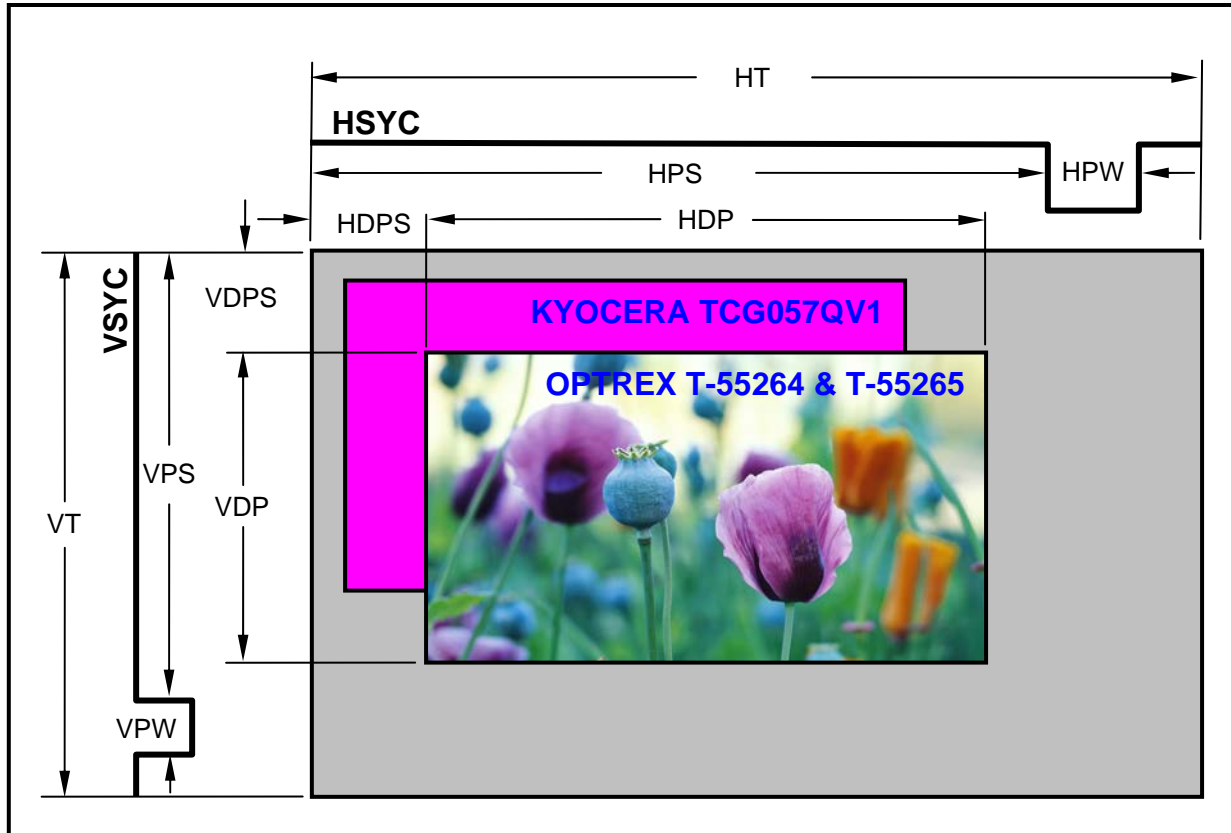
REGISTER NAME	ID	VALUE	COMMENT
MEMORY CLOCK CONFIGURATION	0x04	0x00	Set BCLK to MCLK ratio = 1:1 (20 MHz).
PIXEL CLOCK CONFIGURATION	0x05	0x22	Set PCLK source to CLK1 divided by 3 to obtain (20 MHz / 3 = 6.7 MHz). This gives a 58.8 Hz scan rate.
PANEL TYPE	0x10	0x69	TFT panel, 18-bit data width, color LCD.
HORIZONTAL TOTAL	0x12	50	HT = {[(320 + 68+ 20) / 8] − 1} = 50 (TH from Optrex spec.)
HORIZONTAL DISPLAY PERIOD	0x14	39	HDP = [(320 / 8) − 1] = 39 (TH_D from Optrex spec.)
HORIZONTAL DISPLAY	0x16	68	HDPS = 68

REGISTER NAME	ID	VALUE	COMMENT
PERIOD START POSITION REGISTER 0			(THE from Optrex spec). Bits D0 – D7 are used. Bits D8 and D9 are entered in Register 0x17.
HORIZONTAL DISPLAY PERIOD START POSITION REGISTER 1	0x17	0x00	See above.
VERTICAL TOTAL REGISTER 0	0x18	0x05	VT = [(240 + 18+ 4) – 1] = 261 (0x0105). Bits D0 – D7 are used. Bits D8 and D9 are entered in Register 0x19.
VERTICAL TOTAL REGISTER 1	0x19	0x01	See above.
VERTICAL DISPLAY PERIOD REGISTER 0	0x1c	239	VDP = (240 – 1) = 239. (TV$_D$ from Optrex spec). Bits D0 – D7 are used. Bits D8 and D9 are entered in Register 0x1d.
VERTICAL DISPLAY PERIOD REGISTER 1	0x1d	0	See above.
VERTICAL DISPLAY PERIOD START POSITION REGISTER 0	0x1e	18	VDPS = 18 (TV$_{DS}$ from Optrex spec.). Bits D0 – D7 are used. Bits D8 and D9 are entered in Register 0x1f.
VERTICAL DISPLAY PERIOD START POSITION REGISTER 1	0x1f	0x00	See above.
FPLINE PULSE WIDTH	0x20	0x1D	HPW = (30 – 1) = 29. (TH$_S$ from Optrex spec). HSYC polarity set active low.
FPLINE PULSE START POSITION REGISTER 0	0x22	0x00	HPS = 0. Bits D0 – D7 are used. Bits D8 and D9 are entered in Register 0x23.
FPLINE PULSE START POSITION REGISTER 1	0x23	0x00	See above.
FPFRAME PULSE WIDTH	0x24	0x02	VPW = (3 -1)= 2. (TV$_S$ from Optrex spec). VSYC polarity active low.
FPFRAME PULSE START POSITION REGISTER 0	0x26	0x01	VPS = 1. Bits D0 – D7 are used. Bits D8 and D9 are entered in Register 0x27.
FPFRAME PULSE START POSITION REGISTER 1	0x27	0x00	See above.
DISPLAY MODE	0x70	0xc3	64 Shades per color operation (256 K colors total), normal image display, Dithering ON, Display image blanked. Change to 0x83 to display image.

6.3. REPLACING KYOCERA TCG057QV1 DISPLAY

6.3.1. The clock must be inverted.

6.3.2.   The following software values must be changed to move the image starting position. See **FIGURE 4**.

6.3.2.1. The typical HT periods differ. Increase HT from 400 to 408.

6.3.2.2. Increase HDPS from 7 pixels to 68 pixels.

6.3.2.3. Increase the VDPS from 7 lines to 18 lines.

7.0   HANDLING RECOMMENDATIONS

7.1. FPC & WIRE HANDLING PRECAUTIONS

- DO NOT pick the display up by the FPC tail. This action can break the electrical connection to the ZIF connector or peel the connector from the PCB.

- DO NOT PULL the FPC.

- DO NOT BEND THE FPC TIGHT and form creases. This will fracture the copper traces and cause an open circuit.

- DO NOT pick the dispay up by the CCFL wires or LED cable.

7.2. LCD PROTECTIVE LINER

- The display is manufactured with an optical-grade, clear protective liner attached to the front polarizer. The liner is optical grade to allow inspection through the liner while it is still attached.

- Leave the liner installed until the last possible moment in production to protect the polarizer from impact scratches, fingerprints, and airborne debris.

- Remove the protective liner by placing a small piece of adhesive tape at a corner and press it in place. SLOWLY use the tape to pull the protective liner up and roll off the glass. The protective liner should bend 180° back upon itself as it is slowly pulled. A slow pulling speed reduces electrostatic voltage activating the pixels.

7.3. DO NOT INSERT anything into the holes in the front or rear bezel. These holes are for factory use only.

8.0   SPECIFICATION ERRATA

The following sections provide corrections to the specifications.

END_OF_FILE