First Edition

Jan 1, 2001

LCD Module Technical Specification

Final Revision

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T-51379L035J-FW-P-AA

Checked by (Quality Assurance Div.)

Checked by (Design Engineering Div.)

Prepared by (Production Div.)

Table of Contents

Revision History

Rev.	Date	Page	Comment

1. Application

This target specification applies to 3.5" color TFT-LCD panel. The 3.5” color TFT LCD panel is designed for camcorder, video phone application and other electronic products which require high quality flat panel displays.

2. Features

. Controller IC is not necessary

. Compatible with NTSC or PAL system

. High Resolution : 140,400 Dots (600 × 234)

. High transmittance Ratio : 8.0 %

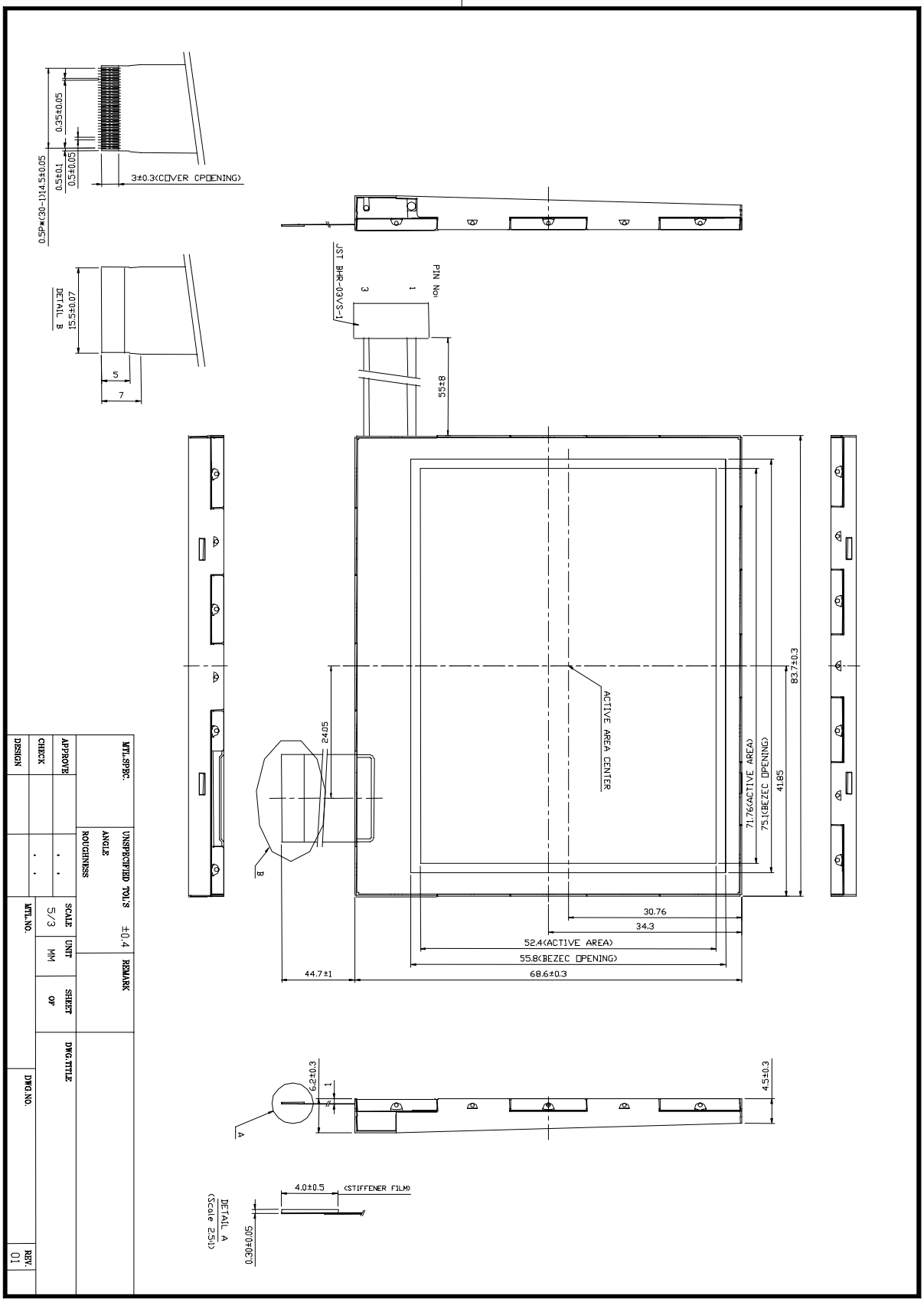
. Optimum Viewing Direction : 6 o’clock

. Up/Down and Left/Right Image Reversion

3. Mechanical Specifications

Parameter	Specifications	Unit
Screen Size	3.5 (diagonal)	inch
Display Format	600×234	dot
Active Area	71.7 (H) X 52.4(V)	mm^2
Dot Pitch	0.119 (H)×0.224 (V)	mm^2
Pixel Configuration	Delta	
Outline Dimension	See Mechanical Drawing	mm^3
Weight	59±3	g

4. Mechanical Drawing of panel:



5.Input / Output Terminals

Pin No	Symbol	I/O	Description	Remark
1	V_{COM}	I	Common Electrode Voltage	Note 5-1
2	V_{BBA}	I	Supply Voltage for Level Shifter (Low Level)	Note 5-2
3	PV_{DD}	I	Supply voltage for panel	Note 5-3
4	V_{BBC}	I	Supply voltage for panel	Note 5-2
5	V_{SS}	I	Ground for panel	
6	V_{CC}	I	Supply Voltage for Level Shifter (High Level)	Note 5-4
7	V_{PIN}	I	Pulse high level for Level Shifter (High Level)	Note 5-5
8	V_{MIN}	I	Pulse low level for Level Shifter (Low Level)	Note 5-5
9	FRP	O	Control Signal for Video Inversion	
10	$\overline{VSY}$	I/O	Vertical Sync.	
11	$\overline{HSY}$	I/O	Horizontal Sync.	
12	C_{SYNC}	I	Composite Sync.	
13	PD	O	Phase Detector	Note 5-6
14	OSC	I	Clock Input for LC Oscillator	Note 5-6
15	V_{DD}	I	Supply Voltage for Logic Circuit	Note 5-3
16	CKC	I	Control Pin for Select I/O Signal	Note 5-12
17	UD	I	Up / Down Control	Note 5-11
18	LR	I	Left / Right Shift Control	Note 5-7
19	NP	I	NTSC / PAL Selector	Note 5-8
20	V_B	I	Video Input B	
21	V_G	I	Video Input G	
22	V_R	I	Video Input R	
23	GND	I	Ground for High voltage logic	
24	GND	I	Ground for logic	
25	DV_{EE}	I	Voltage supply for source driver high logic	Note 5-9
26	C_{COM}	I	Reference for Sample and Hold	Note 5-10
27	AV_{EE}	I	Voltage supply for sample & hold	Note 5-9
28	GND	I	Ground	
29	OV_{EE}	I	Voltage supply for operation amplifier	Note 5-9
30	VP+	I	Pre-charge high level	Note 5-9

Note 5-1 : V_{COM} should be adjusted accurately to get the best contrast ratio.

Note 5-2 : V_{BBA},V_{BBC} = -5V (Typ.)

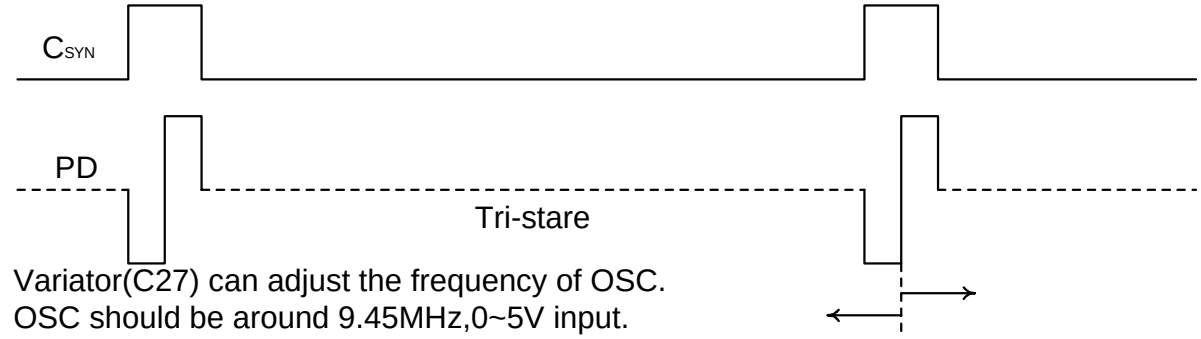
Note 5-3 : V_{DD},PV_{DD} = +5V (Typ.)

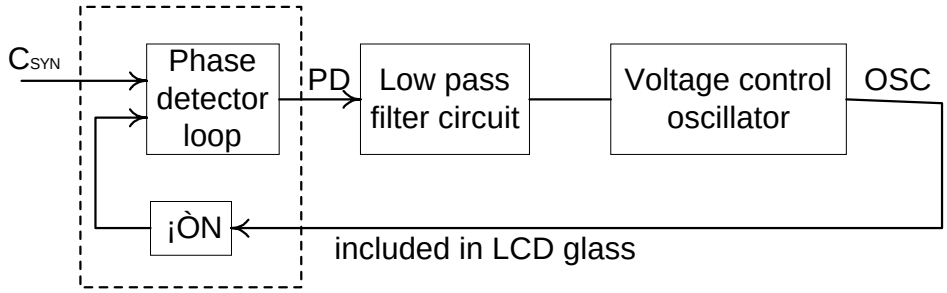
Note 5-4 : V_{CC}=+20V(Typ.)

Note 5-5 : V_{PIN} must be more positive than V_{MIN}.

Pin	Symbol	min	Typ.	Max.	Unit
7	V_{PIN}	12	13	14	V
8	V_{MIN}	5	6	7	V

Note 5-6 : PD output(0~5V range) from phase detector loop which is included in source driver.





Note 5-7 : Left / Right SHIFT .

Note 5-8 : Hi (+5V) for NTSC ; Low (0V) for PAL.

Note 5-9 : DV_{EE},AV_{EE},OV_{EE} and VP+ all equal to +14V

Note 5-10 : C_{COM} +5V (Typ.)

Note 5-11 : UP / Down Shift

Note 5-12 ; Pin 16(CKC) can select the function for Pin 11($\overline{\text{HSY}}$) and Pin 10($\overline{\text{VSY}}$).

CKC	$\overline{\text{HSY}}$	CSY	$\overline{\text{VSY}}$
Hi	$\overline{\text{HSY}}$	CSY Input	$\overline{\text{VSY}}$ Output
Low	External $\overline{\text{HSY}}$ Input	External Clock Input	External $\overline{\text{VSY}}$ Input

6.Absolute Maximum Ratings:

GND = 0 V, Ta = 25 ℃

Parameter		Symbol	MIN.	MAX.	Unit	Remark
Supply Voltage for Source Driver		DV_{EE} ,AV_{EE} OV_{EE} ,VP+	0	+16	V	
Supply Voltage for Gate Driver	H Level	V_{CC}	0	+26	V	
	L Level	V_{BBA}, V_{BBC}	-7	+20	V	
Supply voltage for controller		PV_{DD},V_{DD}	0	+6.5	V	
DC bias voltage of common electrode		Vcom	+2	+6	V	
Analog input signals		V_B,V_R,V_G	0	+12	V	

7. Electrical Characteristics

7-1) Recommended Operating Conditions:

A)Driving for TFT-LCD panel

GND = 0V, Ta = 25 ℃

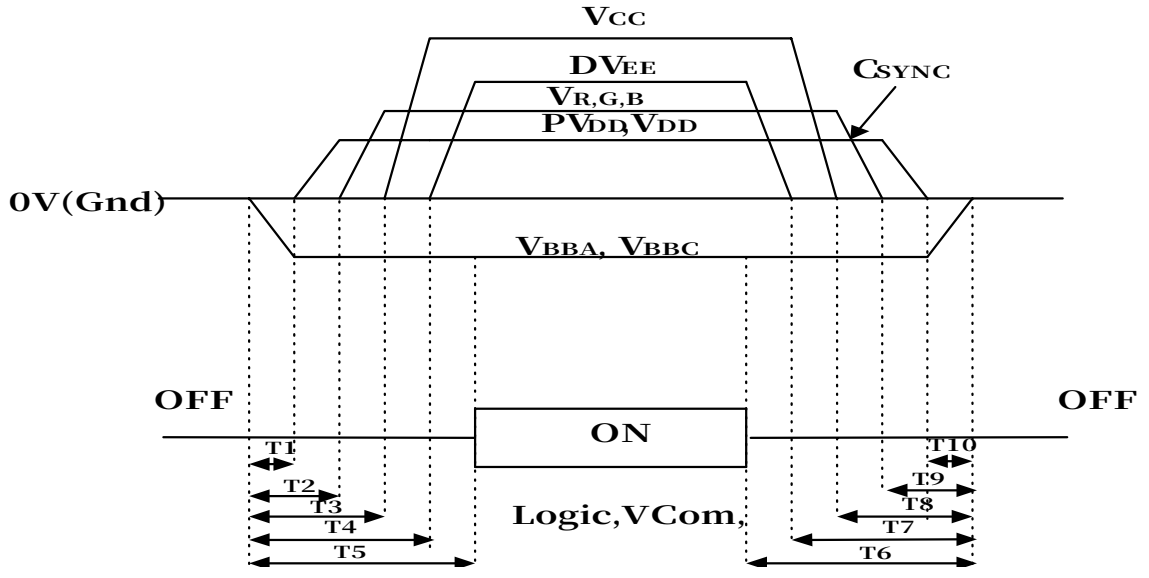
Parameter		Symbol	MIN.	TYP	MAX.	Unit	Remark
Supply voltage for source driver		DV_{EE},AV_{EE} OV_{EE},VP+	+13.5	+14	+14.5	V	
Supply voltage for gate driver	H Level	V_{CC}	+19.5	+20	+20.5	V	
	L level	V_{BBA}, V_{BBC}	-5.5	-5	-4.5	V	
Supply voltage for controller		PV_{DD},V_{DD}	+4.7	+5	+5.3	V	
Analog input Level	Amplitude	V_B,V_R,V_G	+1.1		12	V	
	DC component		+5.8	+6	+6.2	V	
		V_{COM}	+3.6	+3.8	+4.0	V	Note 1

Note 1 : When every value mached above operating conditions, the V_{COM} level also can keep in this range.

B)Power on Sequence(Voltage source)

The Power Sequence only effect by V_{CC},PV_{DD},V_{DD},V_{BBA} and $V_{BBC,}$ the others do not care.

1) 10ms•T1•T2•T3•T4•T5
2) 10ms•T6•T7•T8•T9•T10



C） Driving for Backlight

Ta= 25 ℃

Parameter	Min.	Typ.	Max.	Unit	Remark
Lamp voltage		225		Vrms	
Lamp current		3		mA	
Lamp frequency		35		KHz	

7-2) Power Consumption

Parameter	Conditions	TYP.	Unit	Remark
Current for V_{CC}	V_{CC} = +20V	2.3	mA	
Current for V_{BBA}	V_{BBA} = -5V	2.1	mA	
Current for V_{BBC}	V_{BBC} = -5V	0.05	mA	
Current for DV_{EE}	DV_{EE} = +14V	0.54	mA	
Current for AV_{EE}	AV_{EE} = +14V	3.0	mA	
Current for OV_{EE}	OV_{EE} = +14V	3.7	mA	
Current for V_{DD}	V_{DD} = +5V	5.7	mA	
LCD Panel Power Consumption		0.19	W	
Backlight Power Consumption		0.68	W	

7-3) Input / Output Timing

Parameter		Symbol	MIN.	TYP.	MAX.	Unit	Remarks
Horizontal	Width	T_{HO}	4.2	4.7	5.2	μs	
Sync. Output	Phase Difference	T_{HP}	0	2		μs	
Pulse	Rising Time	T_{HR}	-	-	0.5	μs	
	Falling Time	T_{HF}	-	-	0.5	μs	
Vertical Sync.	Width	T_{VO}	-	4H	-	μs	H=1/15.75K HZ
Output Pulse	Phase Difference	T_{VPO}	-	1H	-	μs	odd field
	Phase Difference	T_{VPE}	-	0.5H	-	μs	even field
	Rising Time	T_{VR}	-	-	2	μs	
	Frequency	f_{FRP}	7.67	7.87	8.07	KH_Z	
Polarity	Delay time	T_{FD}	-	-	4	μs	
Alternating Signal	Falling Time	T_{VF}	-	-	2	μs	

7-4) Display Time Range

A) When sync. signal of NTSC system is applied.

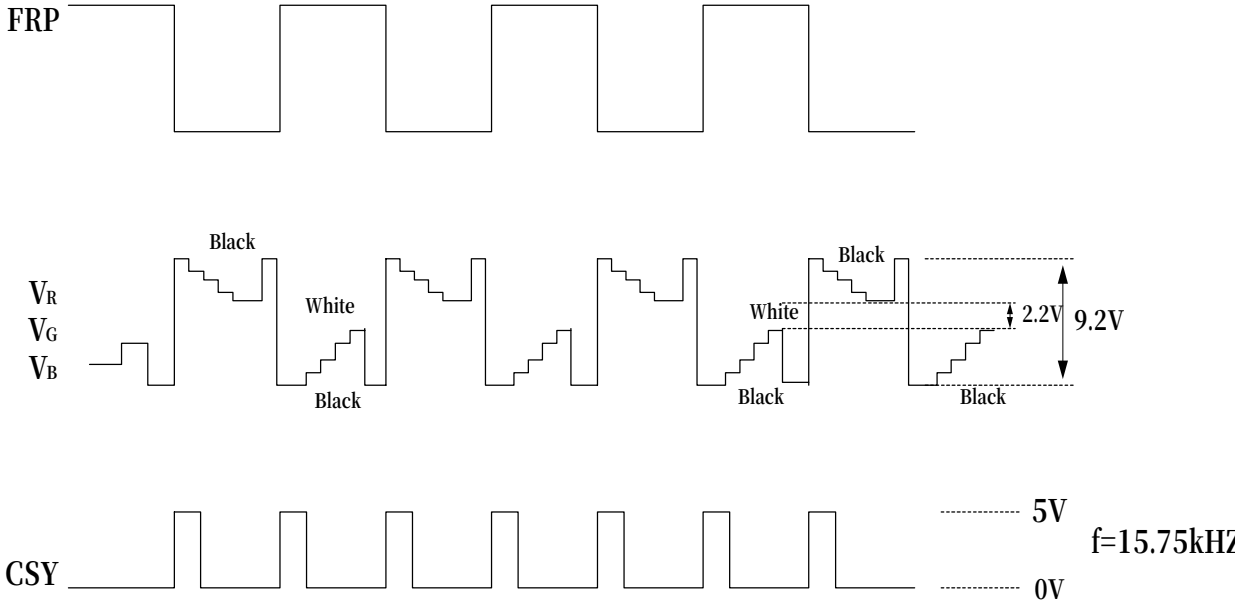
a) Horizontally

12.6 ~ 63.39 μs.

b)Vertical

19 ~ 253 H

B) When sync. signal of PAL system is applied.



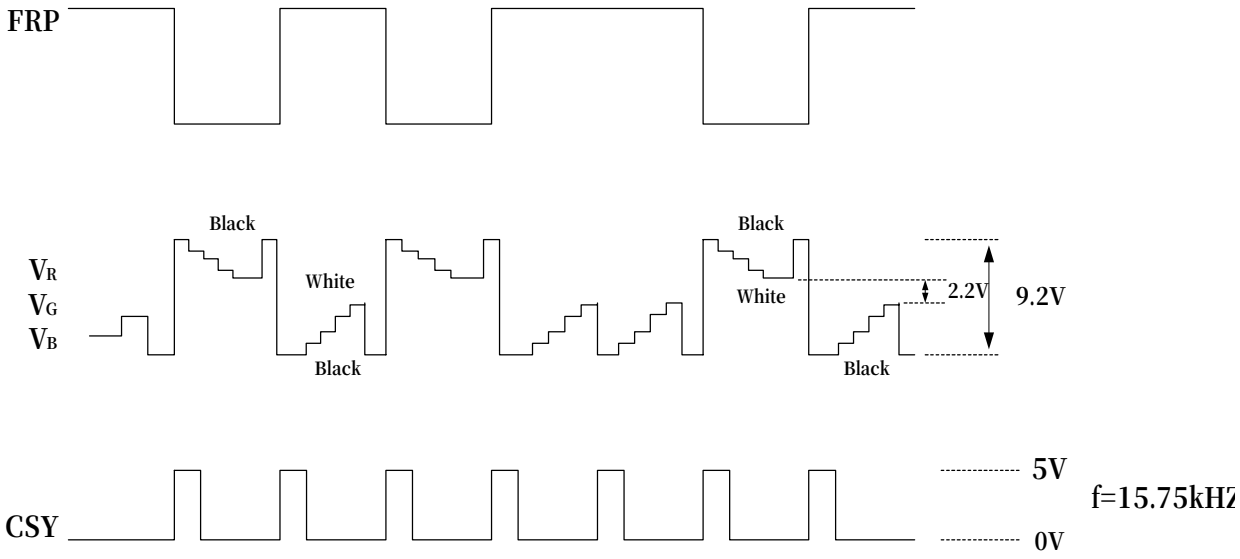
a) Horizontally

13.0 ~ 63.8 μs .

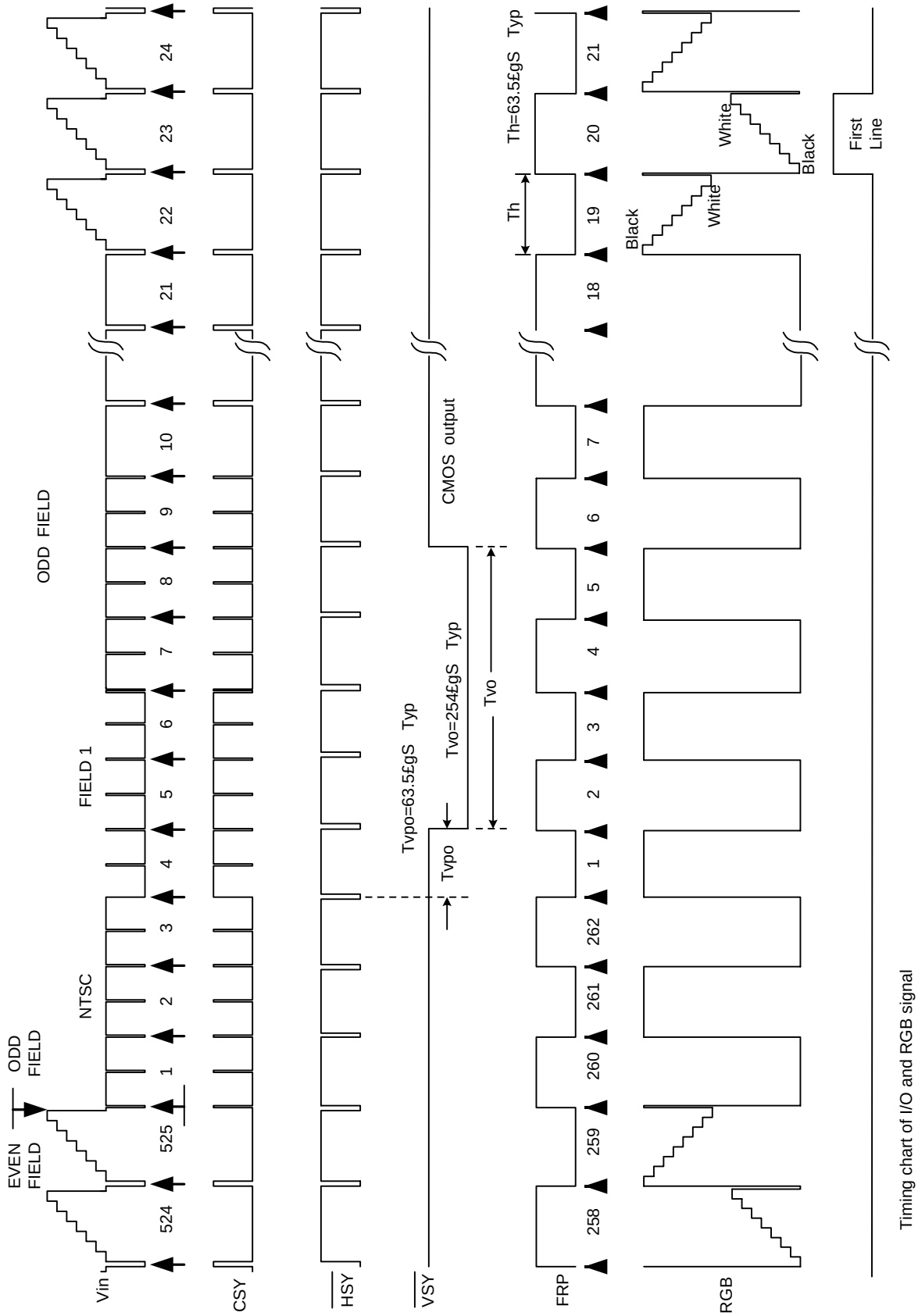
b) Vertical

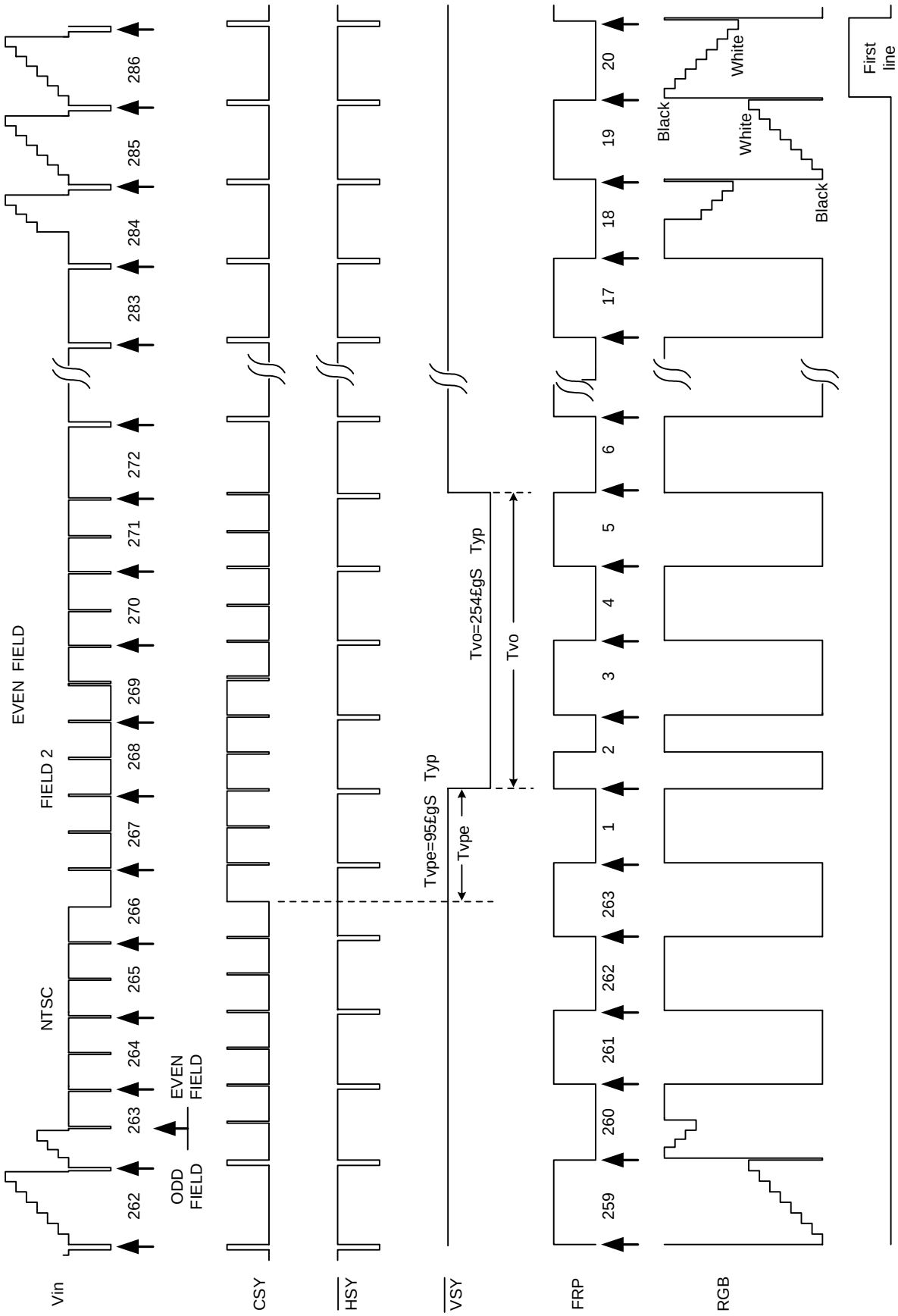
26 ~ 298 H

c) odd field : Scan lines 14n+17 14n+23 (n = 1, 2, 3..) are not displayed.
even field : Scan lines 14n+12 14n+20 (n = 1, 2, 3..) are not displayed.



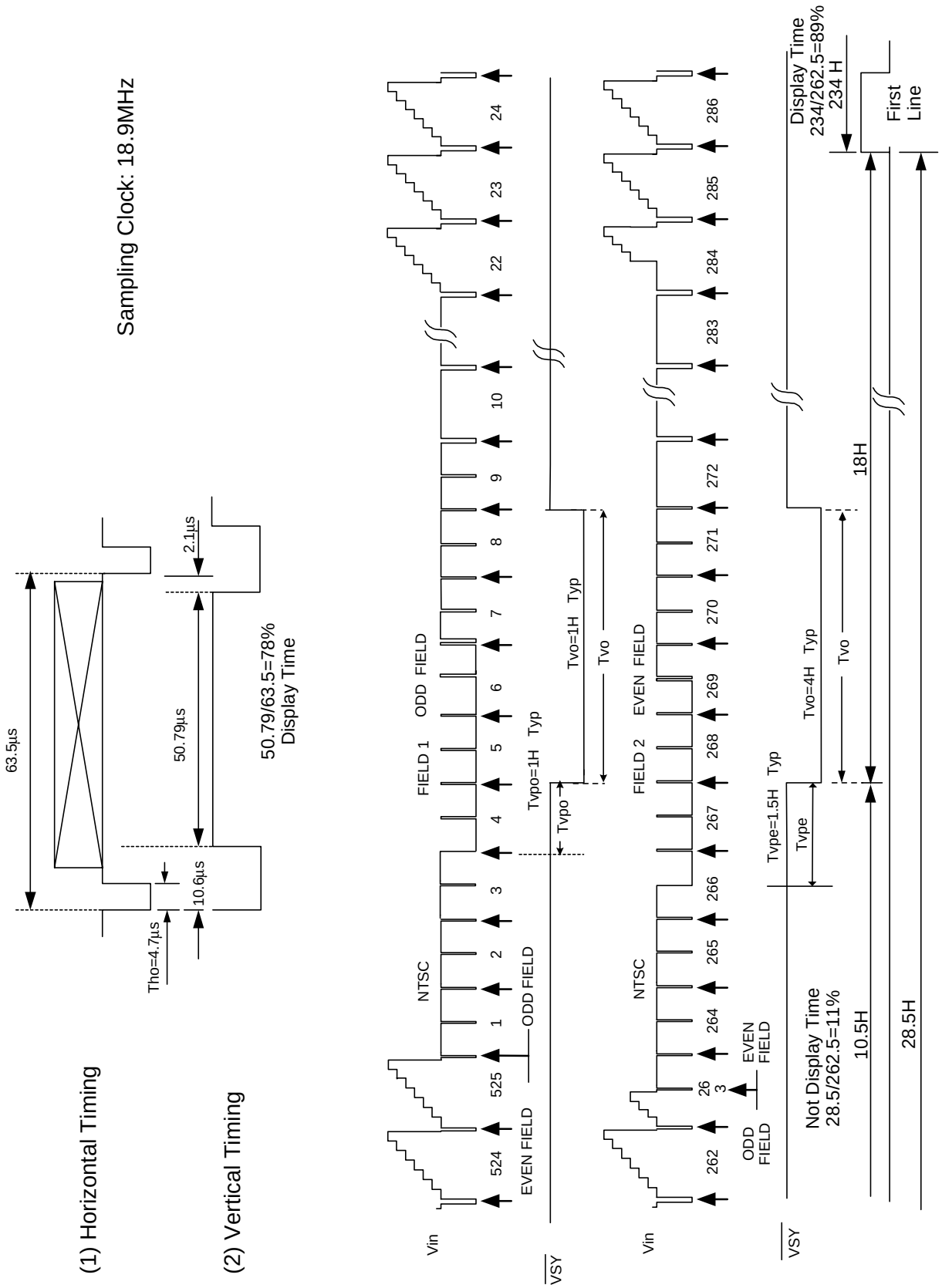
C) NTSC System



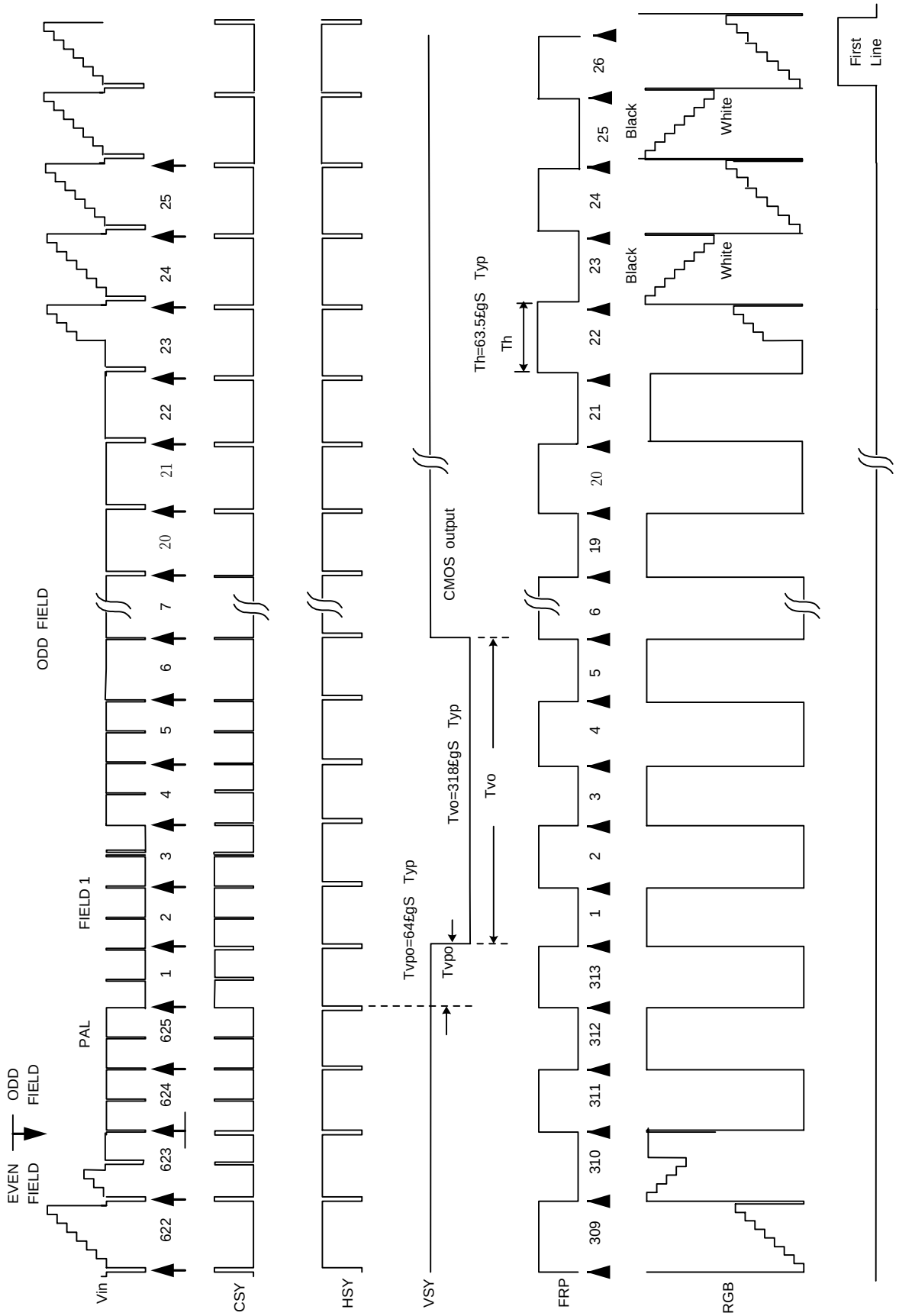


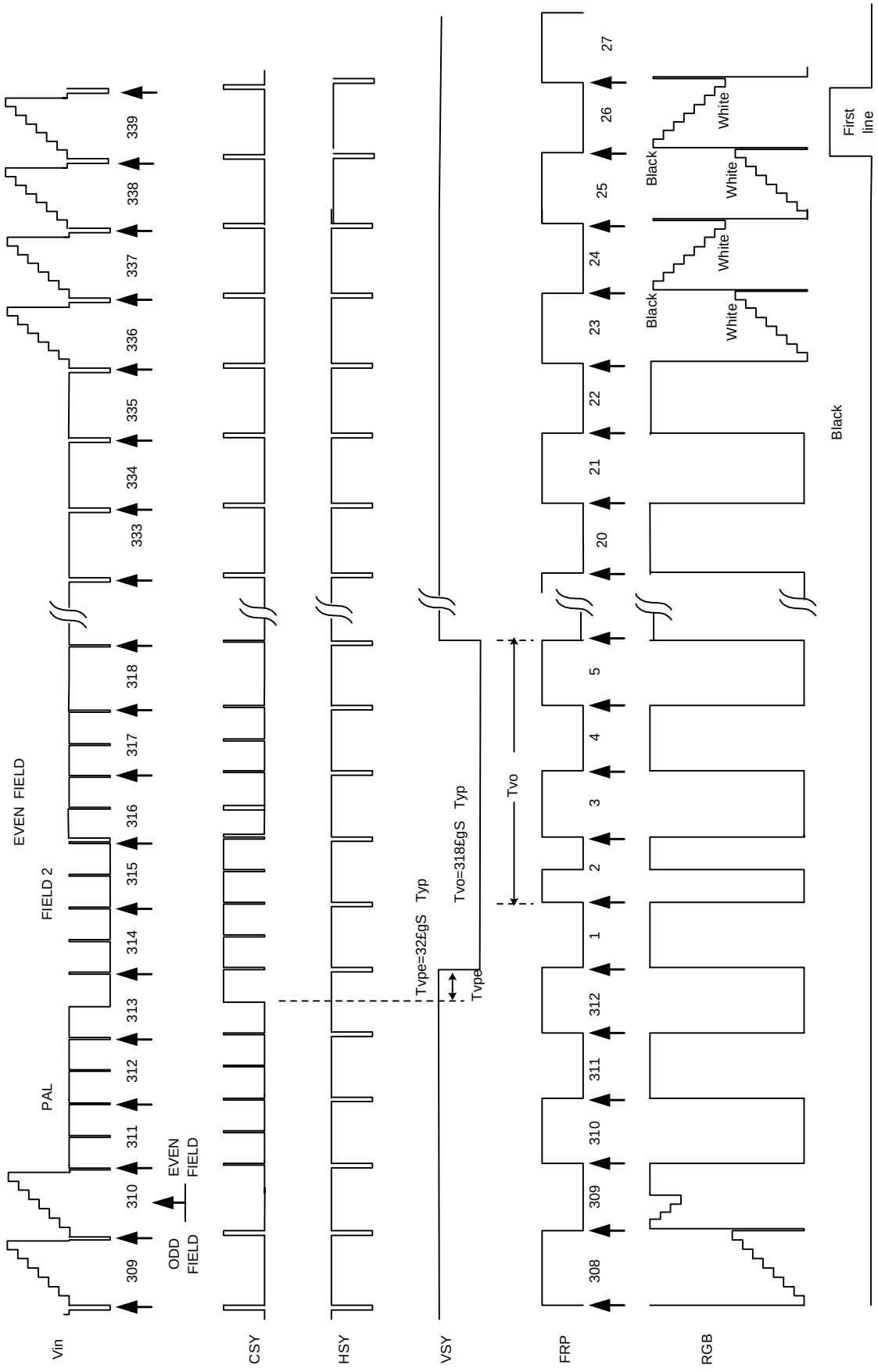
Timing chart of I/O and RGB signal

D) NTSC Display Timing

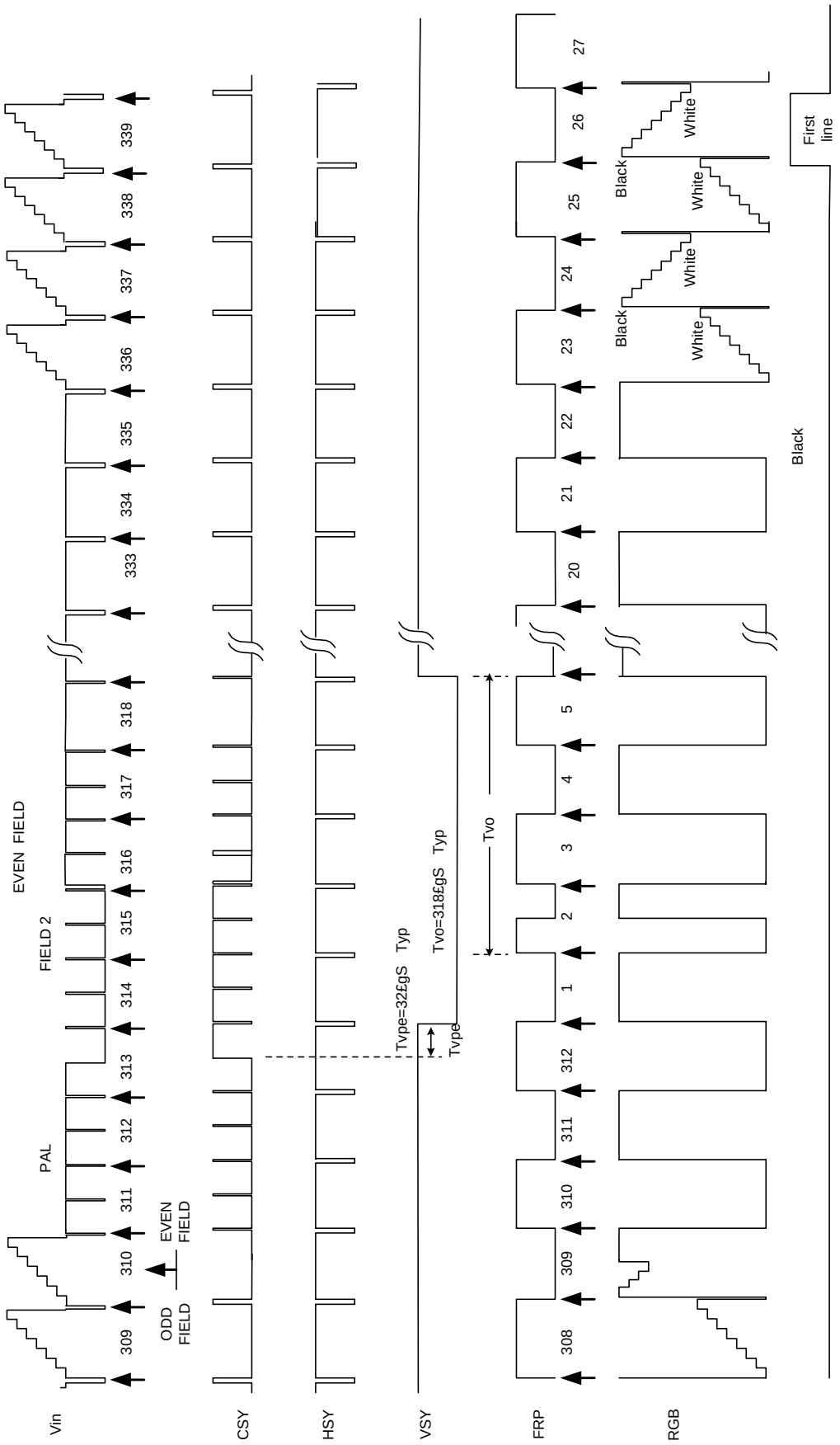


E) PAL System


EVEN FIELD
ODD FIELD
PAL
FIELD 1
ODD FIELD
Vin
CSY
HSY
VSY
FRP
RGB
CMOS output
Tvpo=64£gS Typ
Tvpo
Tvo=318£gS Typ
Tvo
Th=63.5£gS Typ
Th
Black
White
Black
White
First Line
Timing chart of I/O and RGB signal

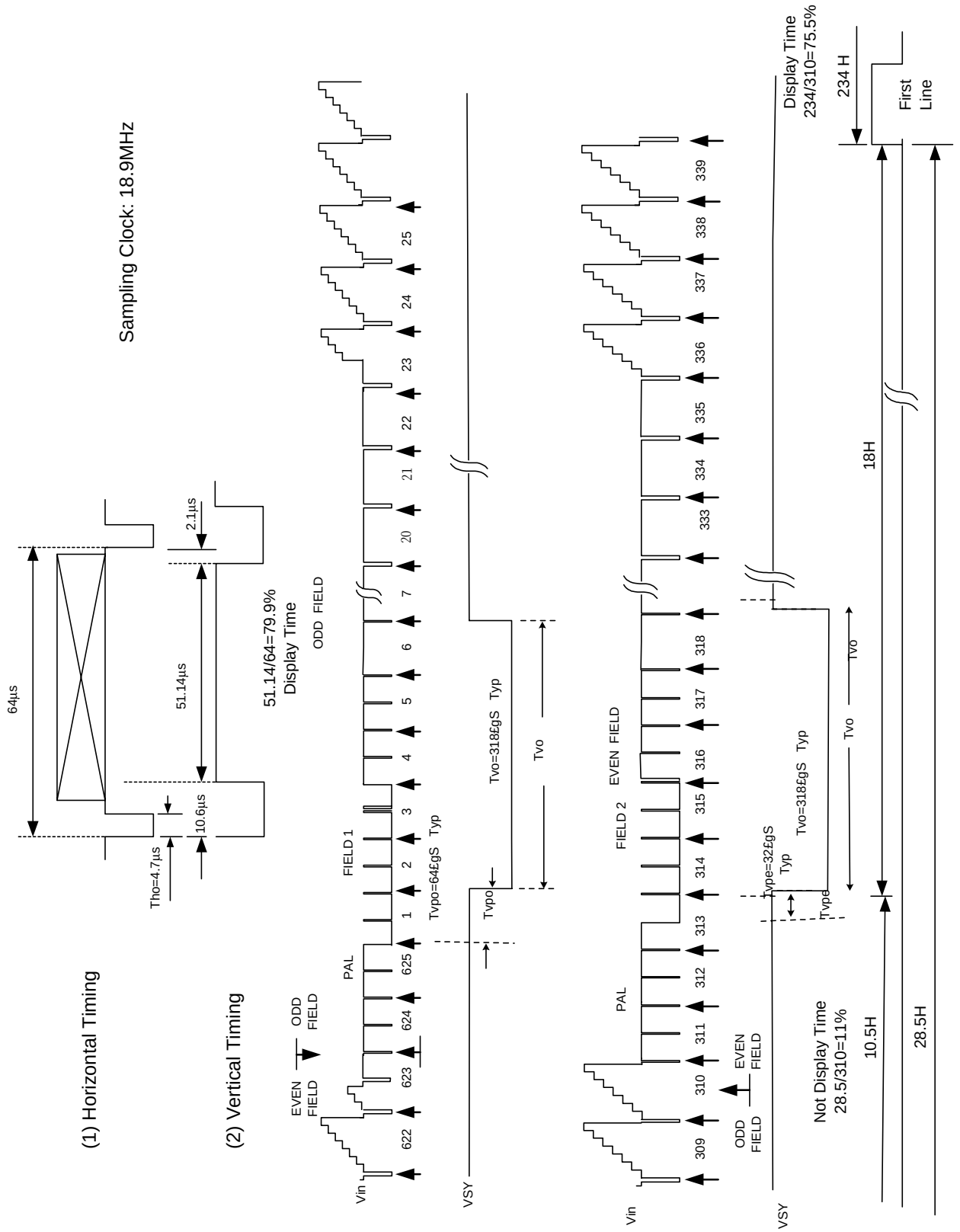


Timing chart of I/O and RGB signal



Timing chart of I/O and RGB signal

F) PAL Display Timing



8.Optical Characteristics
8-1)Specification

Ta = 25℃

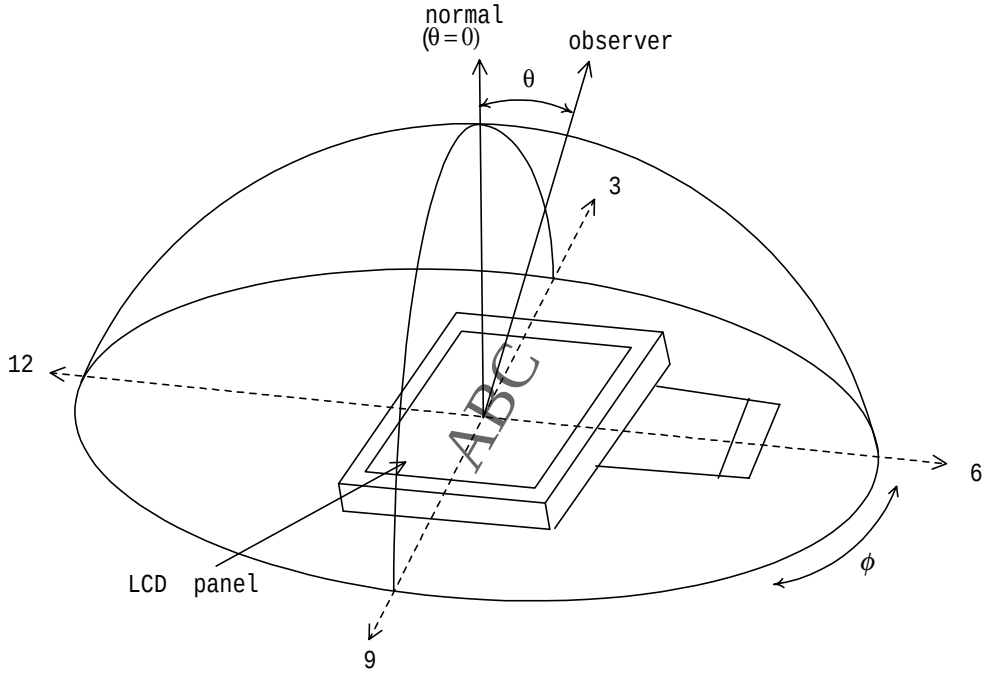
Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	θ	CR≧10	±45	±55		deg	Note 8-3
	Vertical	θ (to 12 o'clock)		10	15		deg	
		θ (to 6 o'clock)		30	35		deg	
Contrast Ratio		CR		80	120			Note 8-1
Response time	Rise	Tr	θ=0°			30	ms	Note 8-4
	Fall	Tf	Φ=0°			50	ms	
Reflectance	Ratio	R			3.0		%	
Brightness				200	250		cd/㎡	Note 8-2
White Chromaticity		X	θ=0°	0.254	0.304	0.354		Note 8-2
		y		0.283	0.333	0.383		
Lamp Life Time	+25℃			10,000			hr	

Note 8-1 : $CR = \frac{\text{Luminance when LCD is White}}{\text{Luminance when LCD is Black}}$

Contrast Ratio is measured in optimum common electrode voltage.
The test configurations of contrast ratio see section 8-2.

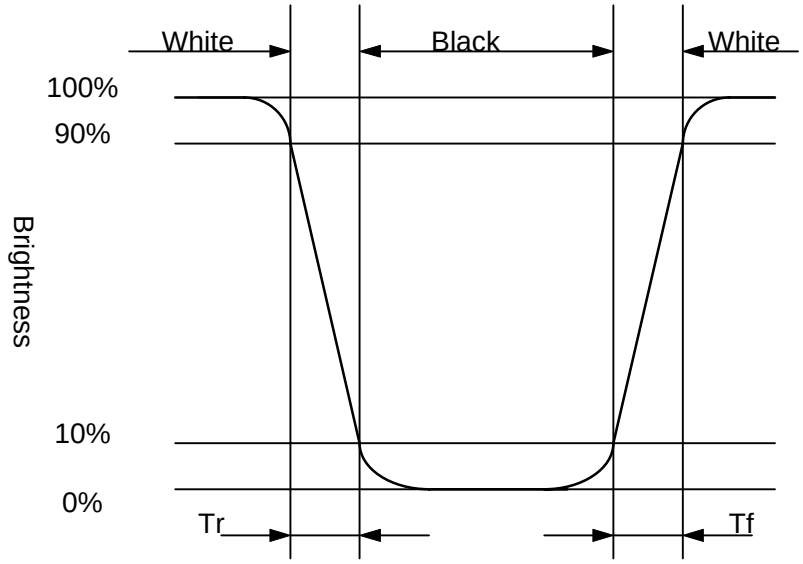
Note 8-2 : 1.Topcon BM-7(fast) luminance meter 1° field of view is used in the testing (after 20~30 minutes operation).
2.Lamp current : 3 mA
3.Inverter model : TDK-347.

Note 8-3 : The definition of viewing angle diagrams :

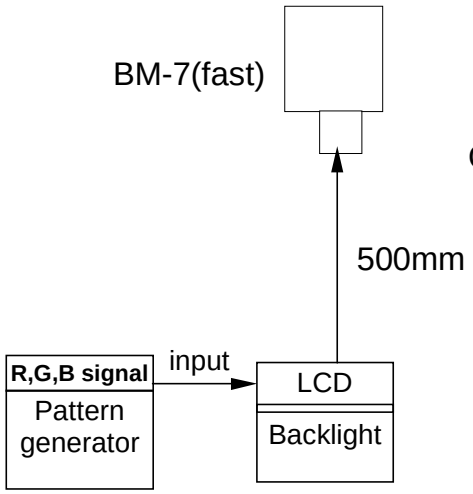


ϕ : Viewing direction
θ : Viewing angle

Note 8-4: The definitions of response time:

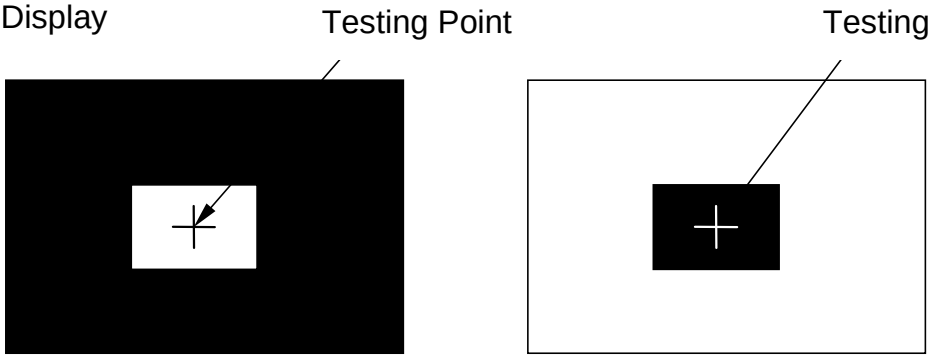


8-2) Test Configuration



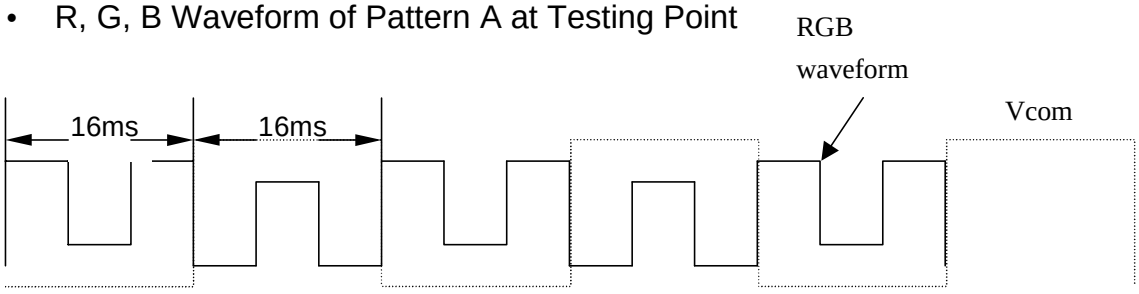
Caution: 1. Environmental illumination≦1 lux
2. Before test CR, Vcom voltage must be adjusted carefully to get the best CR.

- LCD Display



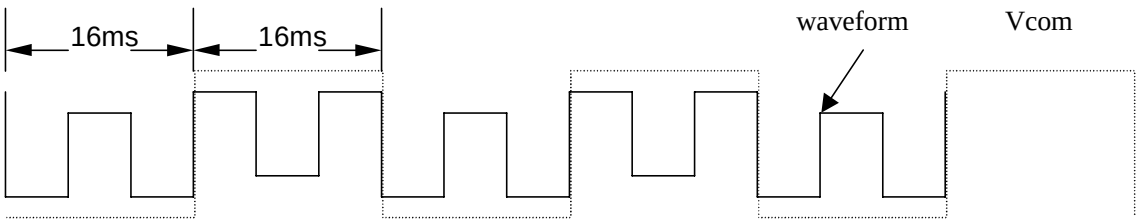
Pattern A Pattern B

- R, G, B Waveform of Pattern A at Testing Point



Vw=1.3V+/-0.2V

- R, G, B Waveform of Pattern B at Testing Point



Vb=4.5+/-0.2V

9. Handling Cautions

9-1) Mounting of module

a) Please power off the module when you connect the input/output connector.

b) Please connect the ground pattern of the inverter circute surely. If the connection is not perfect, some following problems may happen possibly.

1.The noise from the backlight unit will increase.

2.The output from inverter circuit will be unstable.

3.In some cases a part of module will heat.

c) Polarizer which is made of soft material and susceptible to flaw must be handled carefully.

d) Protective film (Laminator) is applied on surface to protect it against scratches and dirts. It is recommended to peel off the laminator before use and taking care of static electricity.

9-2) Precautions in mounting

a) When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth.

b) Wipe off water drops or finger grease immediately.Long contact with water may cause discoloration or spots.

c) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.

d) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

9-3) Adjusting module

a) Adjusting volumes on the rear face of the module have been set optimally before shipment.

b) Therefore, do not change any adjusted values. If adjusted values are changed, the specifications described may not be satisfied.

9-4) Others

a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many Hours.

b) Store the module at a room temperature place.

c) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.

d) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth.When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.

e) Observe all other precautionary requirements in handling general electronic components.

f) Please adjust the voltage of common electrode as material of attachment by 1 module.

10. Reliability

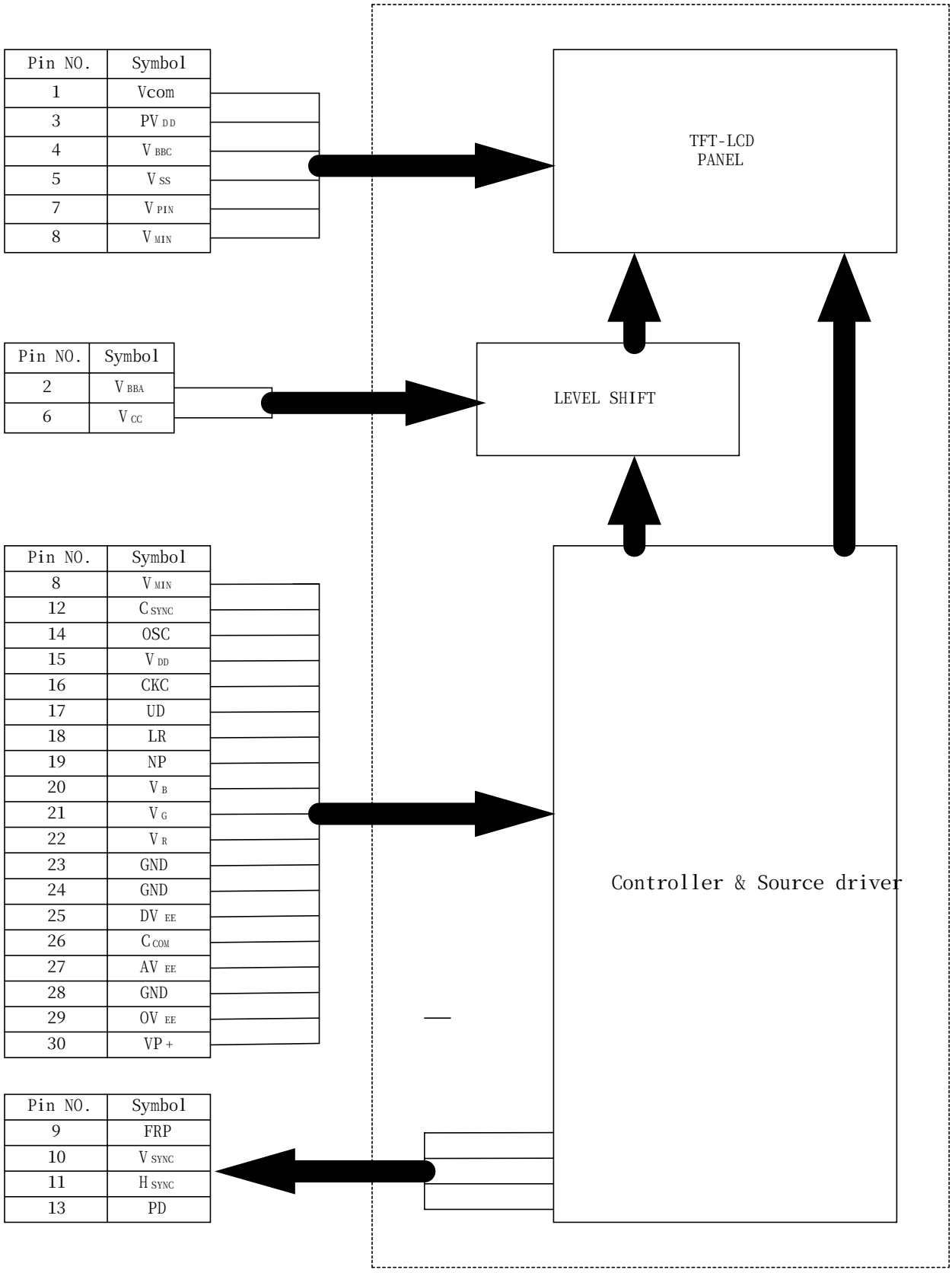
No	Test Item	Test Condition
1	High Temperature Storage Test	Ta = +80 °C, 240 hrs
2	Low Temperature Storage Test	Ta = -30°C, 240 hrs
3	High Temperature Operation Test	Ta = +60 °C, 240 hrs
4	Low Temperature Operation Test	Ta = -10 °C, 240 hrs
5	High Temperature & High Humidity Operation Test	Ta = +60°C, 95%RH, 240 hrs
6	Thermal Cycling Test (non-operating)	-25°C →+25°C→ +70°C, 200 Cycles 30 min 5min 30 min
7	Electrostatic Discharge Test (non-operating)	150pF, 330Ω Air:±15KV; Contact: ±8KV 10 times/point, 4 points/panel face

Ta: ambient temperature

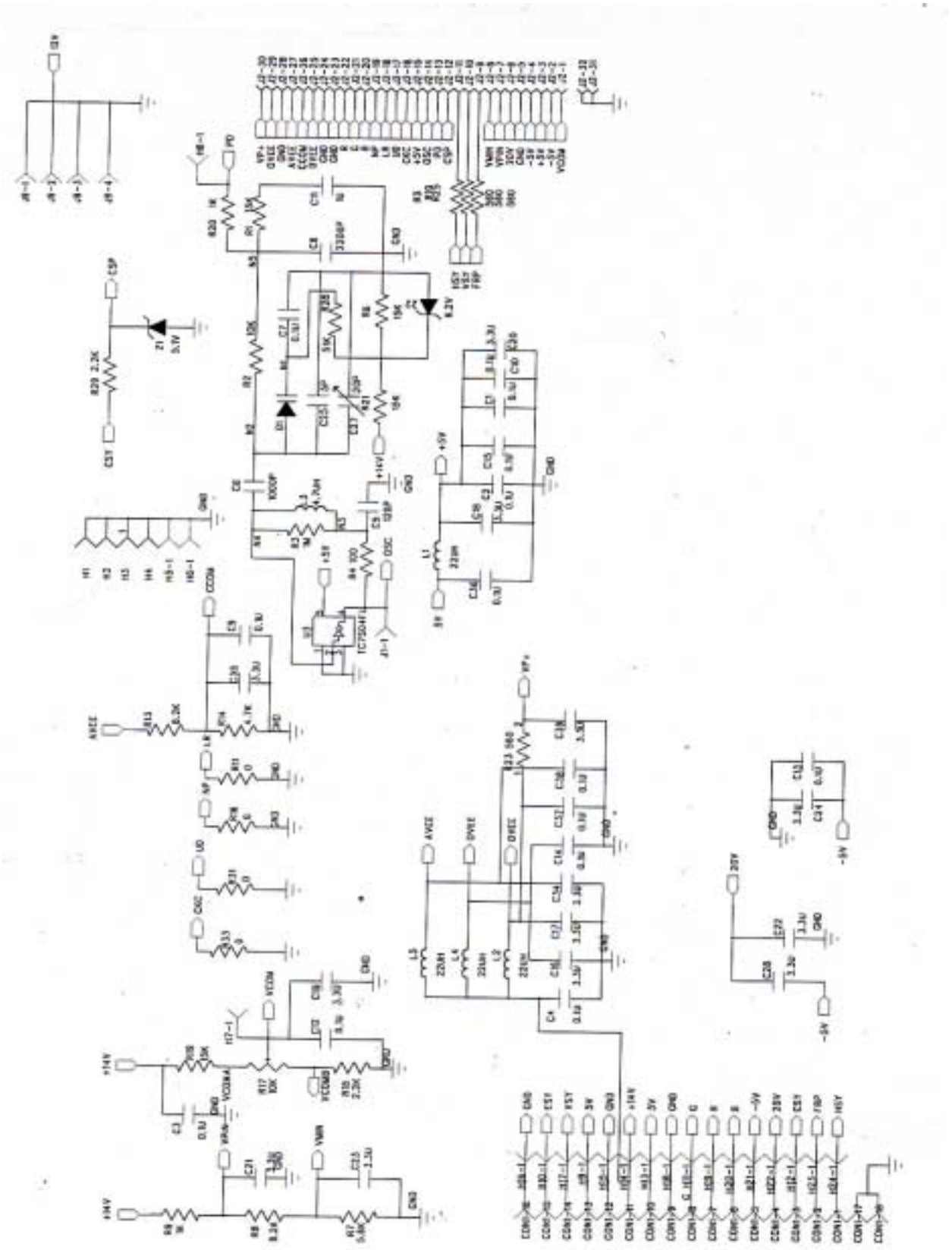
[Criteria]

Under the display quality test conditions with normal operation state, there should be no change which may affect practical display function.

11. Block Diagram



Appendix A: Interface Circuit

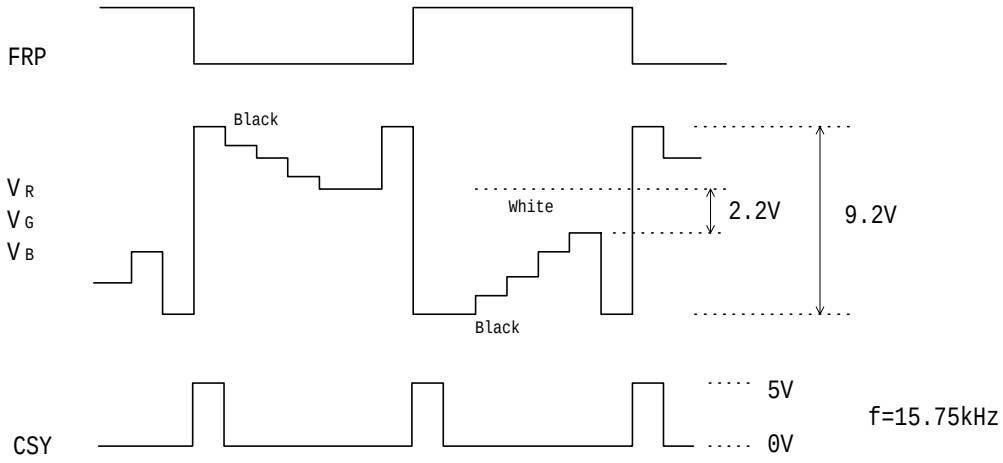


Description of the signal 16 pin connector on interface circuit

1.16 pin description:

Pin No	Symbol	I/O	Description	Remark
1	$\overline{HSY}$	I/O	Horizontal Sync. Input / Output	
2	FRP	O	Video Polarity Alternating Signal	Note 1
3	CSY	I	Composite Sync. Signal	
4	V_{GH}	I	Supply Voltage for Gate Driver (Hi level)	
5	V_{GL}	I	Supply Voltage for Gate Driver (Low level)	
6	V_B	I	Video Signal (Blue)	Note 1
7	V_R	I	Video Signal (Red)	Note 1
8	V_G	I	Video Signal (Green)	Note 1
9	GND	I	Ground	
10	V_{DD}	I	Supply voltage for controller	
11	V_{SH}	I	Supply voltage for source driver	
12	GND	I	Ground	
13	V_{DD}	I	Supply voltage for controller	
14	$\overline{VSY}$	I/O	Vertical Sync. Input/ Output	
15	PSI	O	Synchronize Pulse for Backlight Inverter	
16	GND	O	Ground	

Note 1:



2. Recommended operation condition:

GND = 0V， Ta = 25 ℃

Parameter		Symbol	MIN.	TYP	MAX.	Unit	Remark
Supply voltage for source driver		V_{SH}	+13.5	+14	+14.5	V	
Supply voltage for gate driver	H Level	V_{GH}	+19.5	+20	+20.5	V	
	L Level	V_{GL}	-5.5	-5	-4.5	V	
Supply voltage for controller		V_{DD}	+4.7	+5	+5.3	V	
Digital input Level	H Level		+2.4	-	+5	V	Note 1
	L Level		-0.3	-	+0.8	V	
Digital Output Level	H Level		+2.4	-	+5	V	Note 2
	L Level		0	-	+0.55		

Note 1 : $\overline{\text{HSY}}$, CSY, $\overline{\text{VSY}}$,

Note 2 : $\overline{\text{HSY}}$, FRP, $\overline{\text{VSY}}$, PSI,