

## Features

- Transient protection for high-speed data lines  
IEC 61000-4-2 (ESD) ±25kV (Air)  
±22kV (Contact)
- Protects one high-speed data line
- Low reverse current: < 10nA typical (VR=5V)
- Working voltage: 5V
- Low capacitance: 0.25pF typical
- Dynamic resistance: 0.90 Ohms (Typ)
- Solid-state silicon-avalanche technology

## Description

T0501SA are ultra low capacitance ESD protection devices designed to protect high speed data interfaces. They are designed to replace 0201 size mul- tilayer varistors (MLVs) in portable applications such as cell phones, notebook computers, and other portable electronics. This device offers desirable characteristics for board level protection including fast response time, low operating and clamping voltage, and no device degradation. T0501SA has a typical capacitance of only 0.25pF. This allows it to be used on circuits operating.

T0501SA is in a 2-pin DFN0603 package. It measures 0.6 x 0.3 mm with a nominal height of only 0.25mm. Leads are finished with lead-free NiAu. Each device will protect one line operating at 5 volts. It gives the designer the flexibility to protect single lines in applications where arrays are not practical. The combination of small size and high ESD surge capability makes them ideal for use in portable applications such as cellular phones, digital cameras, and Mp3 players.

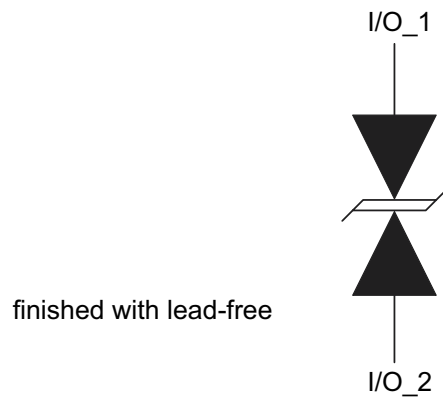
## Applications

- HDMI 1.3/1.4 and HDMI 2.0
- USB 2.0 and USB 3.0
- MHL
- LVDS Interfaces
- FM Antenna
- PCI Express
- eSATA Interfaces

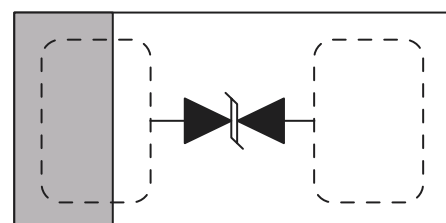
## Mechanical Characteristics

- DFN0603-2L package
- Pb-Free, Halogen Free, RoHS/WEEE Compliant
- Nominal Dimensions: 0.6 x 0.3 x 0.25 mm
- Lead Finish: NiAu
- Molding compound flammability rating: UL 94V-0
- Packaging : Tape and Reel

## Circuit Diagram



## Pin Configuration



DFN0603  
(Top View)

**Absolute Maximum Rating**

Rating	Symbol	Value	Units
Peak Pulse Power ( $t_p = 8/20\mu s$ )	Ppk	100	Watts
Peak Pulse Current ( $t_p = 8/20\mu s$ )	I <sub>PP</sub>	4.5	A
ESD per IEC 61000-4-2 (Air) <sup>1</sup> ESD per IEC 61000-4-2 (Contact) <sup>1</sup>	V <sub>ESD</sub>	±25 ±22	kV
Operating Temperature	T <sub>J</sub>	-55 to +125	°C
Storage Temperature	T <sub>STG</sub>	-55 to +150	°C

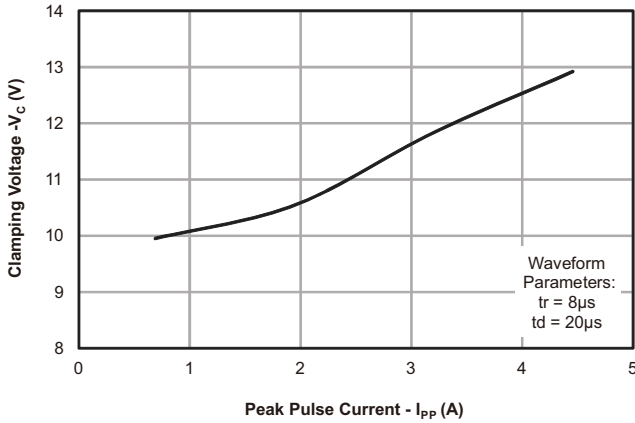
**Electrical Characteristics (T = 25 °C)**

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V <sub>RWM</sub>				5	V
Reverse Breakdown Voltage	V <sub>BR</sub>	I <sub>t</sub> = 1mA	7	9	10	V
Reverse Leakage Current	I <sub>R</sub>	V <sub>RWM</sub> = 5V, T=25°C		0.005	0.100	µA
Clamping Voltage	V <sub>C</sub>	I <sub>PP</sub> = 1A, t <sub>p</sub> = 8/20µs			11	V
Clamping Voltage	V <sub>C</sub>	I <sub>PP</sub> = 4A, t <sub>p</sub> = 8/20µs			15	V
Dynamic Resistance <sup>2, 3, 4</sup>	R <sub>D</sub>	t <sub>p</sub> = 100ns		0.90		Ohms
Junction Capacitance	C <sub>j</sub>	V <sub>R</sub> = 0V, f = 1MHz		0.25	0.4	pF

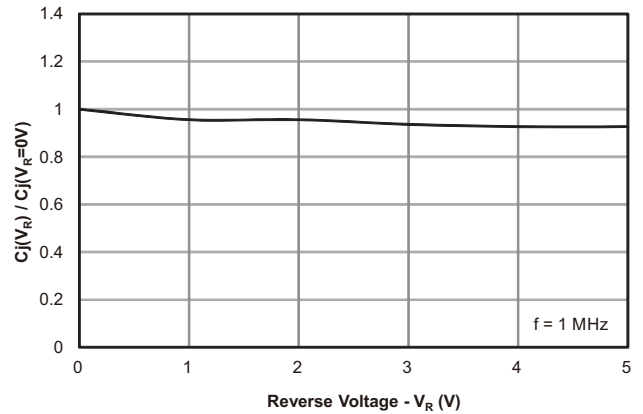
**Notes**

- 1) ESD gun return path connected to ESD ground reference plane.
- 2) Transmission Line Pulse Test (TLP) Settings: t<sub>p</sub> = 100ns, t<sub>r</sub> = 0.2ns, I<sub>TLP</sub> and V<sub>TLP</sub>  
averaging window: t<sub>1</sub> = 70ns to t<sub>2</sub> = 90ns.
- 3) Dynamic resistance calculated from I<sub>TLP</sub> = 4A to I<sub>TLP</sub> = 16A
- 4) Guaranteed by design. Not production tested

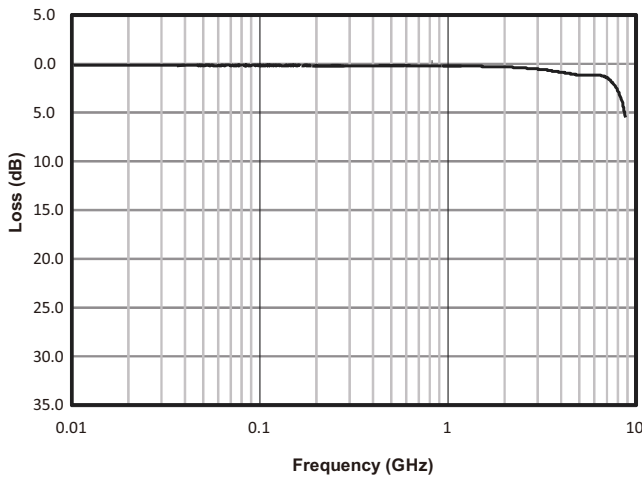
**Clamping Voltage vs. Peak Pulse Current**



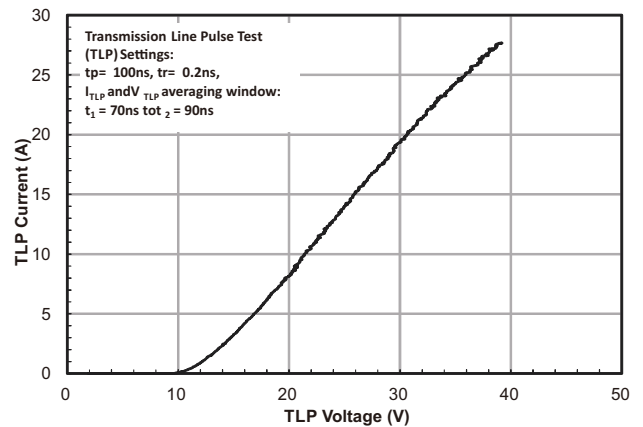
**Typical Capacitance vs. Reverse Voltage**



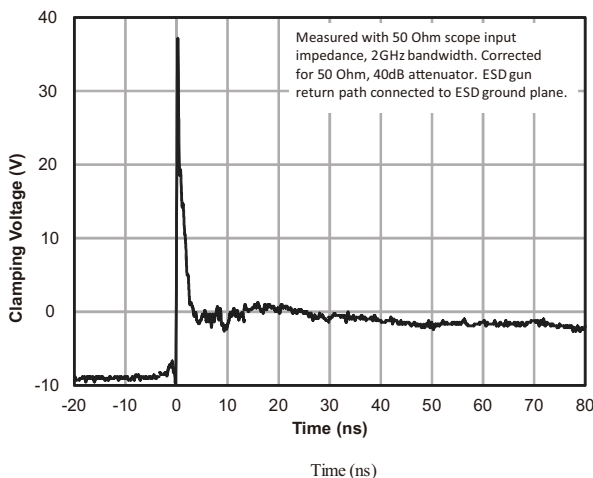
**Typical Insertion Loss (S21)**



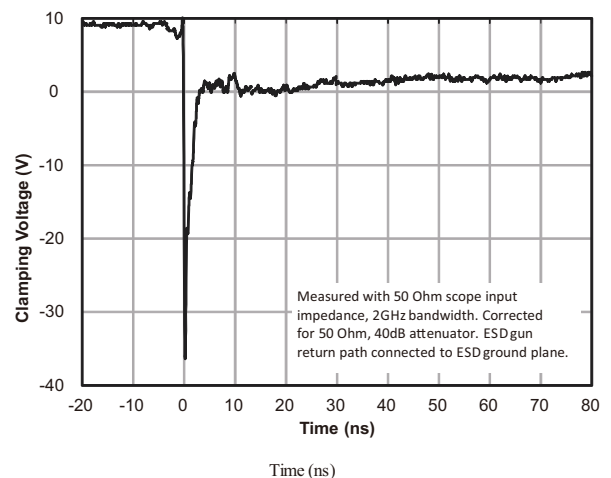
**TLP Characteristic**



**ESD Clamping (+8kV Contact per IEC 61000-4-2)**



**ESD Clamping (-8kV Contact per IEC 61000-4-2)**



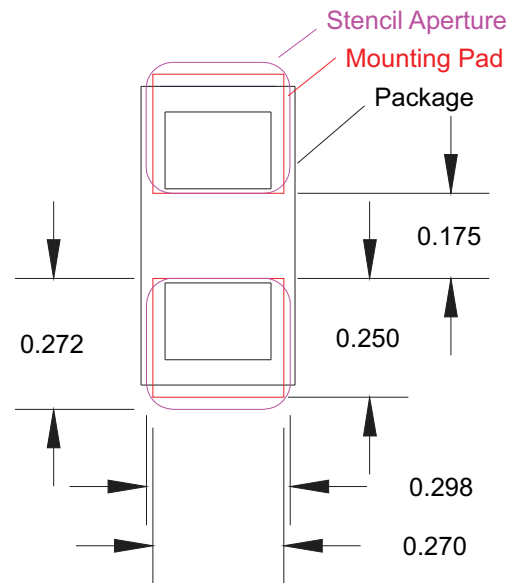
## Application Information

### Assembly Guidelines

The small size of this device means that some care must be taken during the mounting process to insure reliable solder joint. The table below provides CITC recommended assembly guidelines for Mounting this device. The figure at the right details CITC recommended aperture based on the below recommendations. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. The exact manufacturing parameters will require some experimentation to get the desired solder application.

Assembly Parameter	Recommendation
Solder Stencil Design	Laser cut, Electro-polished
Aperture shape	Rectangular with rounded corners
Solder Stencil Thickness	0.100 mm (0.004")
Solder Paste Type	Type 4 size sphere or smaller
Solder Reflow Profile	Per JEDEC J-STD-020
PCB Solder Pad Desig	Non-Solder mask defined
PCB Pad Finish	OSP OR NiAu

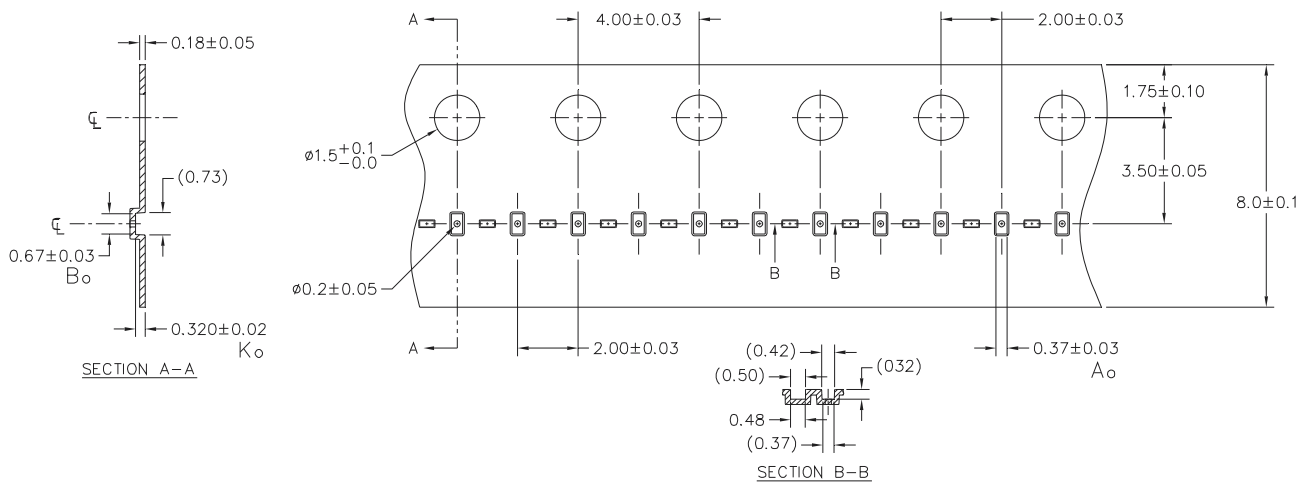
Recommended Mounting Pattern



## Ordering Information

Part Number	Qty per Reel	Reel Size
T0501SA	10,000	7inch

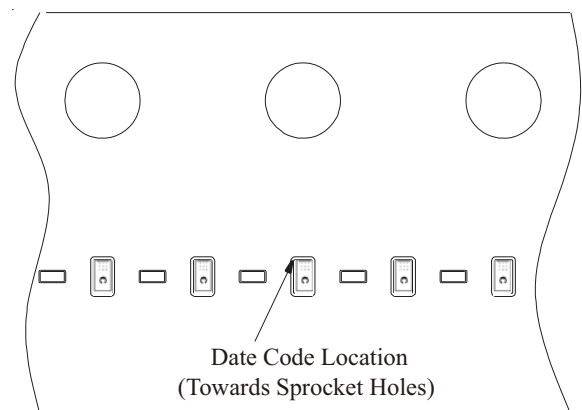
## Carrier Tape Specification



A0	B0	K0
0.37 +/-0.03	0.67 +/-0.03	0.32 +/-0.02 mm

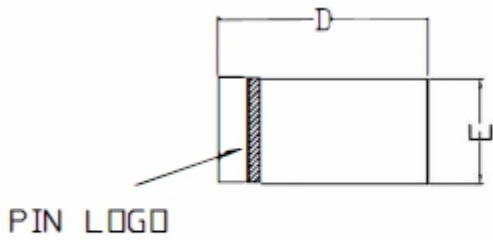
Note: All dimensions in mm unless otherwise specified

## Device Orientation in Tape

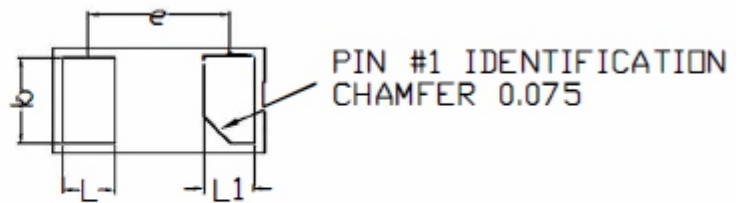


### Package Outline

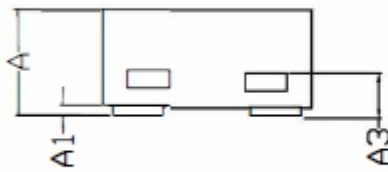
DFN0603-2L package  
 2 leads  
 MSL-1



TOP VIEW



BOTTOM VIEW



SIDE VIEW

COMMON DIMENSIONS(MM)			
PKG.	X3/EXTREME THIN		
REF.	MIN.	NOM.	MAX.
A	>0.23	-	0.33
A1	0.00	-	0.05
A3	0.102REF.		
D	0.55	0.60	0.65
E	0.25	0.30	0.35
b	0.215	0.245	0.275
L	0.115	0.145	0.175
L1	0.115	0.145	0.175
e	0.40BSC		

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