T0502SK

Ultra-Low Capacitance ESD Protection Device

Features

- Transient protection for high-speed data lines
  - IEC 61000-4-2 (ESD) ±25kV (Air)
  - ±17kV (Contact)
  - IEC 61000-4-4 (EFT) 40A (5/50 ns)
  - Cable Discharge Event (CDE)
- Small package (2.9mm u 2.8mm u 1.4mm)
- Protects two data lines
- Low capacitance: 0.3 pF Typical (I/O-GND)
- Low leakage current: 0.1μA @ V_{RWM} (Typical)
- Low clamping voltage
- Each I/O pin can withstand over 1000 ESD strikes for ±8kV contact discharge

Description

T0502SK is an ultra-low capacitance Transient Voltage Suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for high-speed data interfaces. With typical capacitance of 0.3 pF only, T0502SK is designed to protect parasitic-sensitive systems against over-voltage and over-current transient events. It complies with IEC61000-4-2 (ESD), Level 4 (±15kV air,±8kV contact discharge), IEC 61000-4-4 (electrical fast transient - EFT)(40A, 5/50ns), very fast charged device model (CDM) ESD and cable discharge event (CDE), etc.

T0502SK uses small SOT23-3L package. Each T0502SK device can protect two high-speed data lines. The combined features of low capacitance, small size and high ESD robustness make T0502SK ideal for high-speed data ports and high-frequency lines (e.g., USB2.0 & DVI) applications. The low clamping voltage of the T0502SK guarantees a minimum stress on the protected IC.

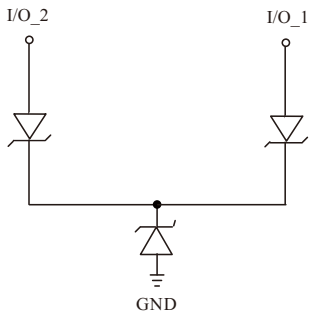
Applications

- Serial ATA
- PCI Express
- Desktops, Servers and Notebooks
- MDDI Ports
- USB2.0 Power and Data Line Protection
- Display Ports
- Digital Visual Interfaces (DVI)

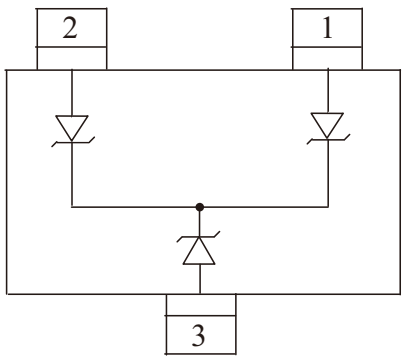
Mechanical Characteristics

- SOT23-3L package
- Flammability Rating: UL 94V-0
- Packaging: Tape and Reel

Circuit Diagram



Pin Configuration



SOT23-3L
(Top View)

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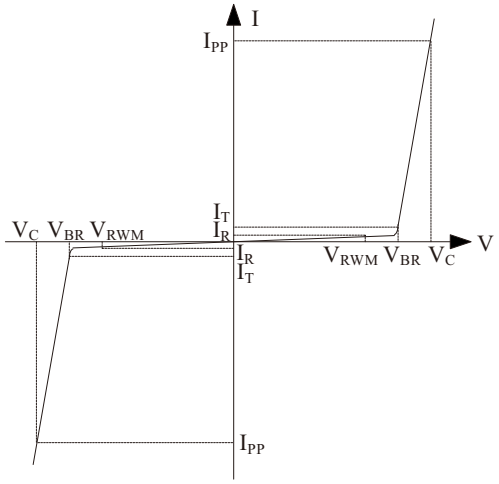
Absolute Maximum Rating

Symbol	Parameter	Value	Units
V_{ESD}	ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	±25 ±17	kV
T_{OPT}	Operating Temperature	-55/+125	°C
T_{STG}	Storage Temperature	-55/+150	°C

Electrical Characteristics (T = 25°C)

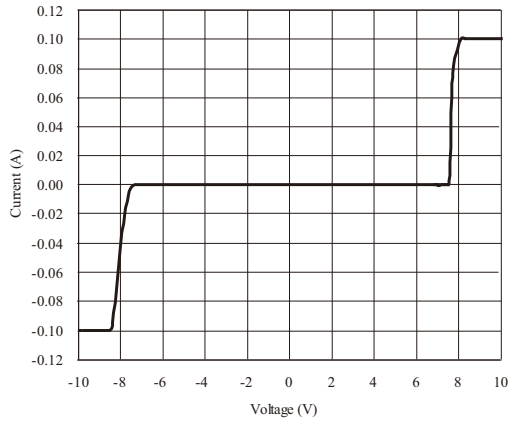
Symbol	Parameter
V_{RWM}	Nominal Reverse Working Voltage
I_R	Reverse Leakage Current @ V_{RWM}
V_{BR}	Reverse Breakdown Voltage @ I_T
I_T	Test Current for Reverse Breakdown
V_C	Clamping Voltage @ I_{PP}
I_{PP}	Maximum Peak Pulse Current
C_{ESD}	Parasitic Capacitance
V_R	Reverse Voltage
f	Small Signal Frequency
I_F	Forward Current
V_F	Forward Voltage @ I_F



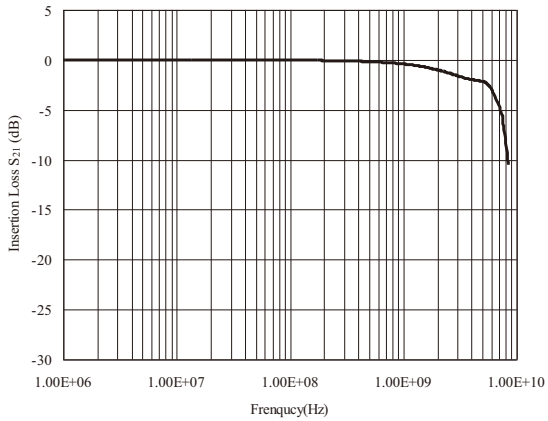
Bi-Directional TVS

Symbol	Test Condition	Minimum	Typical	Maximum	Units
V_{RWM}				5.0	V
I_R	V_{RWM} = 5V, T = 25°C Between I/O and GND		0.1	1.0	μA
V_{BR}	I_T = 1mA Between I/O and GND	7.0	9.0	11.0	V
V_C	I_{PP} = 1A, t_p = 8/20μs Between I/O and GND			12.0	V
C_{ESD}	V_R = 0V, f = 1MHz Between I/O and GND		0.3	0.4	pF
C_{ESD}	V_R = 0V, f = 1MHz Between I/O and I/O		0.3	0.4	pF

Voltage Sweeping of I/O to GND

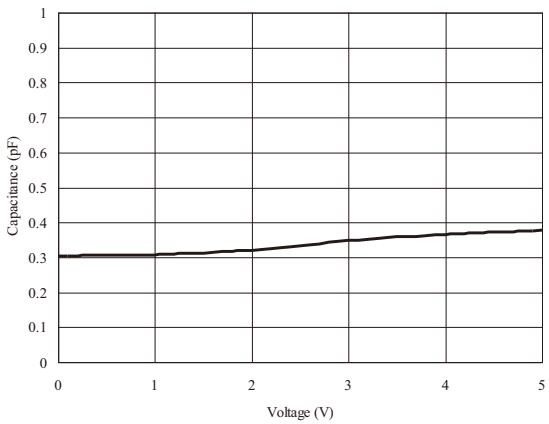


Insertion Loss S21 of I/O to GND

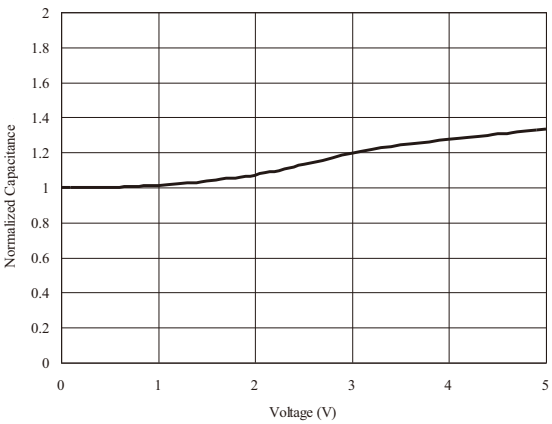


Capacitance *vs.* Voltage of I/O to I/O (f = 1MHz)

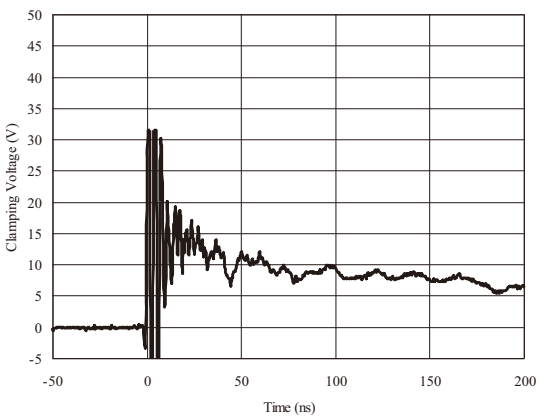
Capacitance *vs.* Reverse Voltage



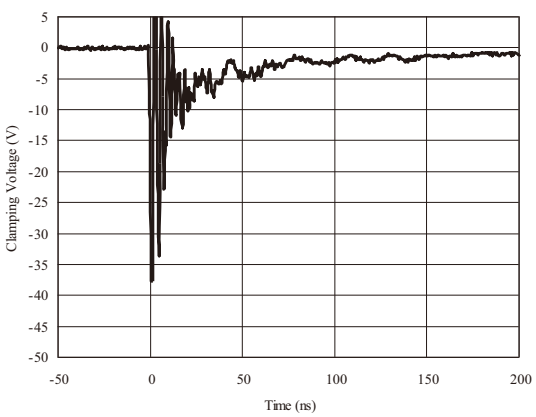
Normalized Capacitance *vs.* Reverse Voltage



ESD Clamping (+8kV Contact per IEC 61000-4-2)



ESD Clamping (-8kV Contact per IEC 61000-4-2)



Application Information

Pin Connection in PCB

T0502SK is capable to provide ESD protection for two data lines simultaneously. The pin connevtion is shown in Figure 1.

Two parallel data lines, from inner IC to I/O port connector, could connect to T0502SK two I/O pins directly. Pin 3 of T0502SK is the negative reference pin, which should connect to the GND of PCB. The connection wires should be as short as possible in order to minimize the parasitic inductance.

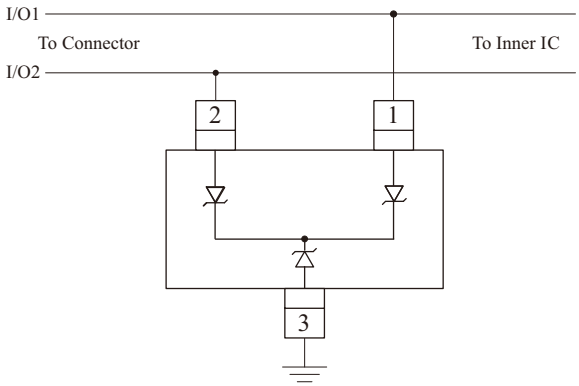


Figure 1 T0502SK pin connection in PCB

PCB Layout Guidelines

For optimum ESD protection and the whole circuit performance, the following PCB layout guidelines are recommended:

T0502SK GND pin to the PCB GND rail path should be as short as possible. It could reduce the ESD transient return path to GND .

The vias connecting T0502SK GND pins to PCB GND should be wide.

Place T0502SK as close to th connector port as possible. It could reduce the parasitic inductance and restrict ESD coupling into adjacent traces.

Avoid running critical signals near board edges.

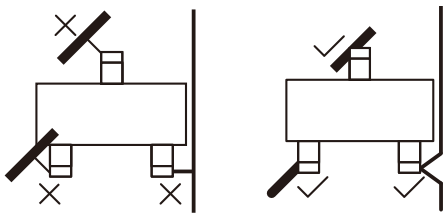


Figure 2 T0502SK Layout Guidelines

Universal Serial Bus ESD Protection

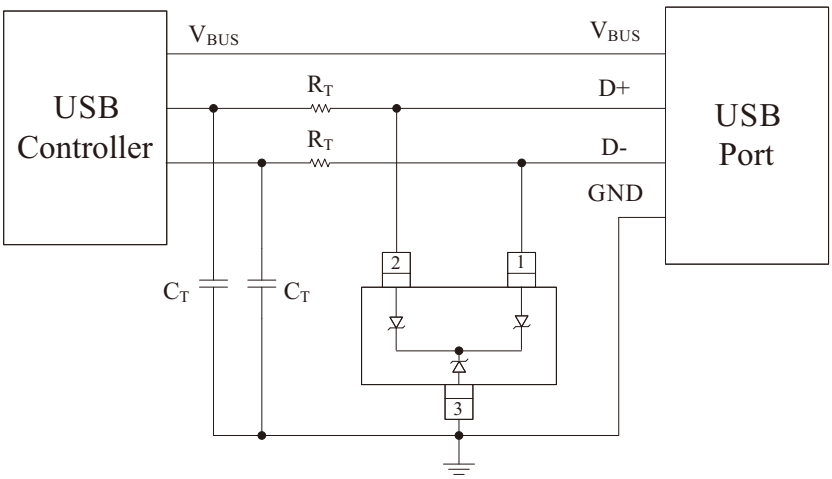


Figure 3 Schematic and Diagram for USB 2.0 Protection using T0502SK

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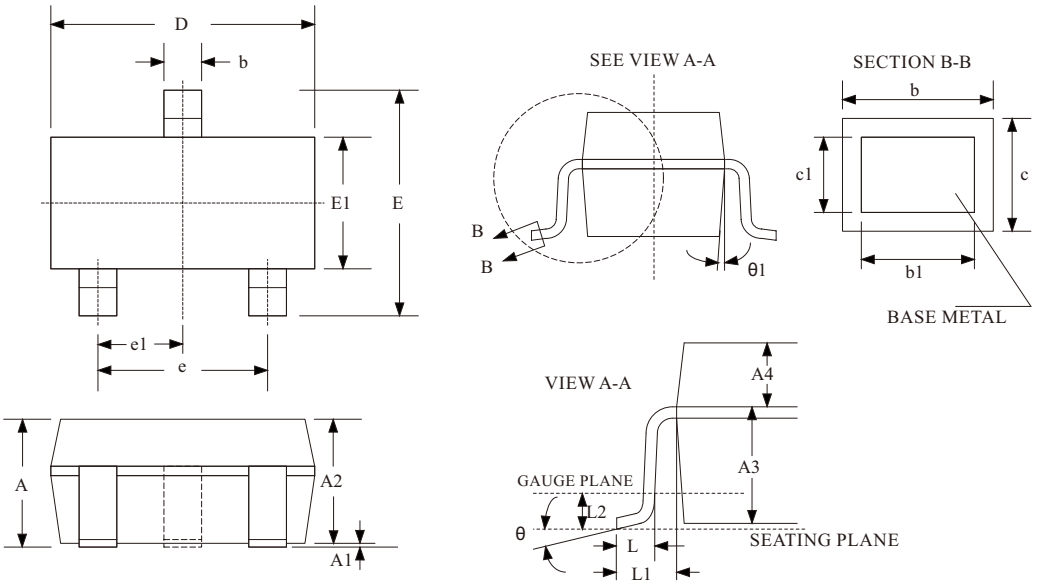
Package Outline

SOT23-3L package



Package Dimensions (Controlling dimensions are in millimeters)

Symbol	Dimensions (mm)			Dimensions (Inches)		
	Minimum	Typical	Maximum	Minimum	Typical	Maximum
A	---	---	1.450	---	---	0.057
A1	0.000	---	0.150	0.000	---	0.006
A2	0.900	1.200	1.300	0.035	0.047	0.012
A3	0.637	0.787	0.837	0.025	0.031	0.033
A4	0.263	0.413	0.463	0.010	0.016	0.018
b	0.300	---	0.500	0.012	---	0.020
b1	0.300	0.400	0.450	0.012	0.016	0.018
c	0.080	---	0.220	0.003	---	0.009
c1	0.080	0.130	0.200	0.003	0.005	0.008
D	2.90 BSC			0.114 BSC		
e	1.90 BSC			0.075 BSC		
e1	0.95 BSC			0.037 BSC		
E	2.80 BSC			0.110 BSC		
E1	1.60 BSC			0.063 BSC		
L	0.300	0.450	0.600	0.012	0.018	0.024
L1	0.600 REF			0.024 REF		
L2	0.250 BSC			0.010 BSC		
θ	0°	4°	8°	0°	4°	8°
θ1	5°	10°	15°	5°	10°	15°

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http://www.citcorp.com.tw/ Tel:886-3-5600628 Fax:886-3-5600636
Add:Rm. 3, 2F., No.32, Taiyuan St., Zhubei City, Hsinchu County 302, Taiwan (R.O.C.)