## Features

- Transient protection for high-speed data lines
  - IEC 61000-4-2 (ESD) ±25kV (Air)
  - ±17kV (Contact)
  - IEC 61000-4-4 (EFT) 40A (5/50 ns)
  - Cable Discharge Event (CDE)
- Package optimized for high-speed lines
- Ultra-small package (2.5mmx1.0mmx0.55mm)
- Protects six data lines
- Low capacitance: 0.2pF Typical(I/O-I/O)
- Low leakage current: 0.1uA@$V_{RWM}$ (Typical)
- Low clamping voltage
- Each I/O pin can with stand over 1000 ESD strikes for ±8kV contact discharge

## Description

T0524SP is an ultra-low capacitance Transient Voltage Suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for high-speed data interfaces. With typical capacitance of 0.2 pF only, T0524SP is designed to protect parasitic-sensitive systems against over-voltage and over-current transient events. It complies with IEC 61000-4-2 (ESD), Level 4 (±15kV air, ±8kV contact discharge), IEC 61000-4-4 (electrical fast transient - EFT) (40A,5/50 ns), very fast charged device model (CDM) ESD and cable discharge event (CDE), etc.

T0524SP uses ultra-small DFN2510-10L package. Each T0524SP device can protect four high-speed data lines The combined features of ultra-low capacitance, ultra-small size and high ESD robustness make T0524SP ideal for high-speed data ports and high-frequency lines (e.g.,HDMI & DVI) applications. The low camping voltage of the T0524SP guarantees a minimum stress on the protected IC.

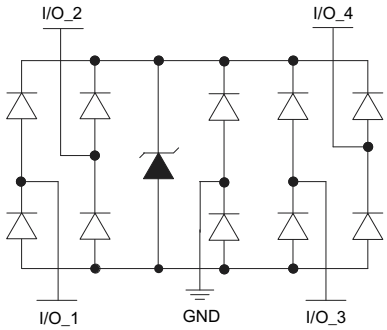
## Applications

- Serial ATA
- PCI Express
- Desktops, Servers and Notebooks
- MDDI Ports
- USB 2.0/3.0/3.1 Power and Data Line Protection
- Display Ports
- High Definition Multi-Media Interface (HDMI1.4/2.0)
- Digital Visual Interfaces (DVI)

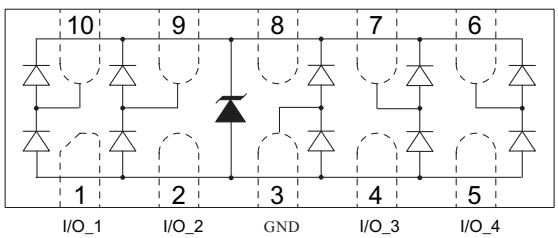
## Mechanical Characteristics

- DFN2510-10L package
- Flammability Rating: UL 94V-0
- Packaging: Tape and Reel

## Circuit Diagram




## Pin Configuration



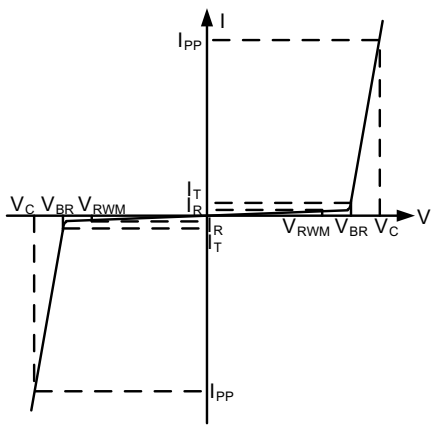

DFN2510-10L
(Top View)

## Absolute Maximum Rating

| Symbol | Parameter | Value | Units |
|---|---|---|---|
| $V_{ESD}$ | ESD per IEC 61000-4-2 (Air)<br>ESD per IEC 61000-4-2 (Contact) | ±25<br>±17 | kV |
| $T_{OPT}$ | Operating Temperature | -55/+125 | ℃ |
| $T_{STG}$ | Storage Temperature | -55/+150 | ℃ |

## Electrical Characteristics (T = 25℃)

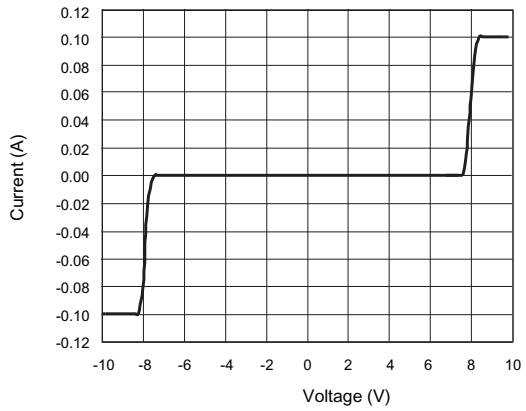
| Symbol | Parameter |
|---|---|
| $V_{RWM}$ | Nominal Reverse Working Voltage |
| $I_R$ | Reverse Leakage Current @$V_{RWM}$ |
| $V_{BR}$ | Reverse Breakdown Voltage @$I_T$ |
| $I_T$ | Test Current for Reverse Breakdown |
| $V_C$ | Clamping Voltage @ $I_{PP}$ |
| $I_{PP}$ | Maximum Peak Pulse Current |
| $C_{ESD}$ | Parasitic Capacitance |
| $V_R$ | Reverse Voltage |
| f | Small Signal Frequency |
| $I_F$ | Forward Current |
| $V_F$ | Forward Voltage @$I_F$ |



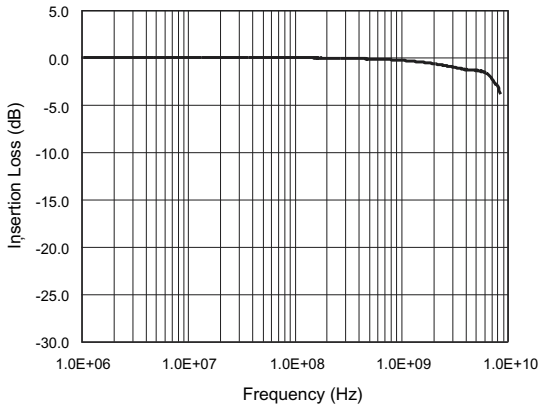
Bi-Directional TVS

| Symbol | Test Condition | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| $V_{RWM}$ | | | | 5.0 | V |
| $I_R$ | $V_{RWM}$ = 5V,T = 25 C<br>Between I/O and GND | | 0.1 | 1.0 | μA |
| $V_{BR}$ | $I_T$ = 1mA<br>Between I/O and GND | 7.0 | 9.0 | 11.0 | V |
| $V_C$ | $I_{PP}$ = 1A, $t_p$ = 8/20μs<br>Between I/O and GND | | | 12 | V |
| $C_{ESD}$ | $V_R$ = 0V, f = 1MHz<br>Between I/O and GND | | 0.2 | 0.3 | pF |
| $C_{ESD}$ | $V_R$ = 0V, f = 1MHz<br>Between I/O and I/O | | 0.2 | 0.3 | pF |

## Voltage Sweeping of I/O to GND

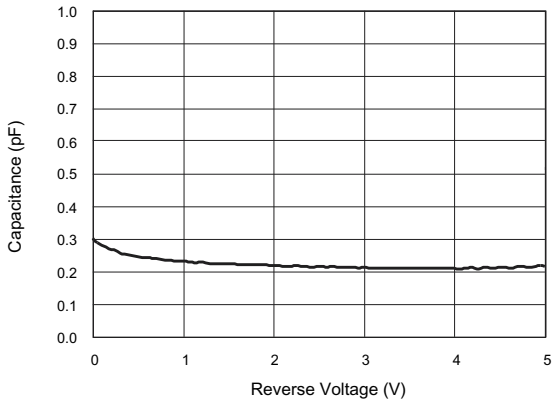



## Insertion Loss S21 of I/O to GND

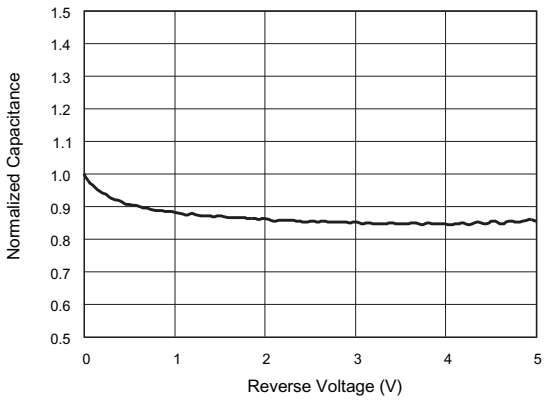



## Capacitance *vs.* Voltage of I/O to GND (f = 1MHz)

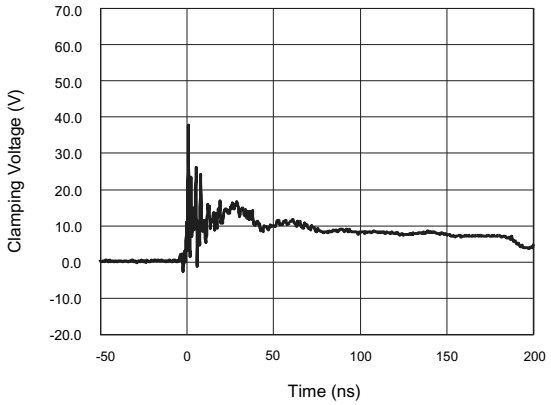
Capacitance *vs.* Reverse Voltage



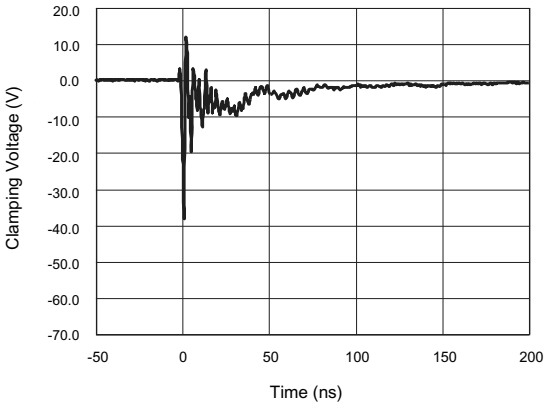

Normalized Capacitance *vs.* Reverse Voltage




## ESD Clamping of I/O to GND (+8kV Contact per IEC 61000-4-2)




## ESD Clamping of I/O to GND (-8kV Contact per IEC 61000-4-2)



## Application Information

### Pin Connection in PCB

T0524SP provides ESD protection for four data lines simultaneously. The pin connection is shown in the figure below.

Four parallel data lines, from inner IC to I/O port connector, coule connect to T0524SP four I/O pins directly. Pin 3 of T0524SP is the GND pin, which should connect to the GND of PCB. The wire should be as short as possible in order to minimize the parasitic inductance.

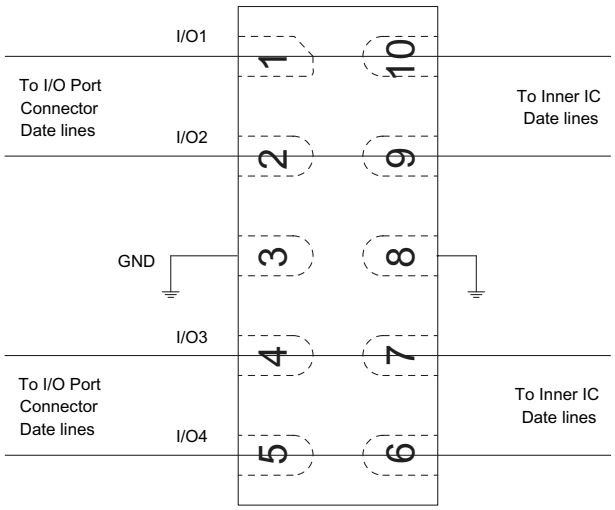



Figure 1 T0524SP pin connection in PCB

### PCB Layout Guidelines

For optimum ESD protection and the whole circuit performance, the following PCB layout guidelines are recommended:

- T0524SP GND pin to the PCB GND rail path should be as short as possible. It could reduce the ESD transient return path to GND.
- The vias connecting T0524SP GND pins to the PCB GND should be wide
- Place T0524SP as close to the connector port as possible. It could reduce the parasitic inductance and restrict ESD coupling into adjacent traces.
- Avoid running critical signals near board edges.

## Application Information

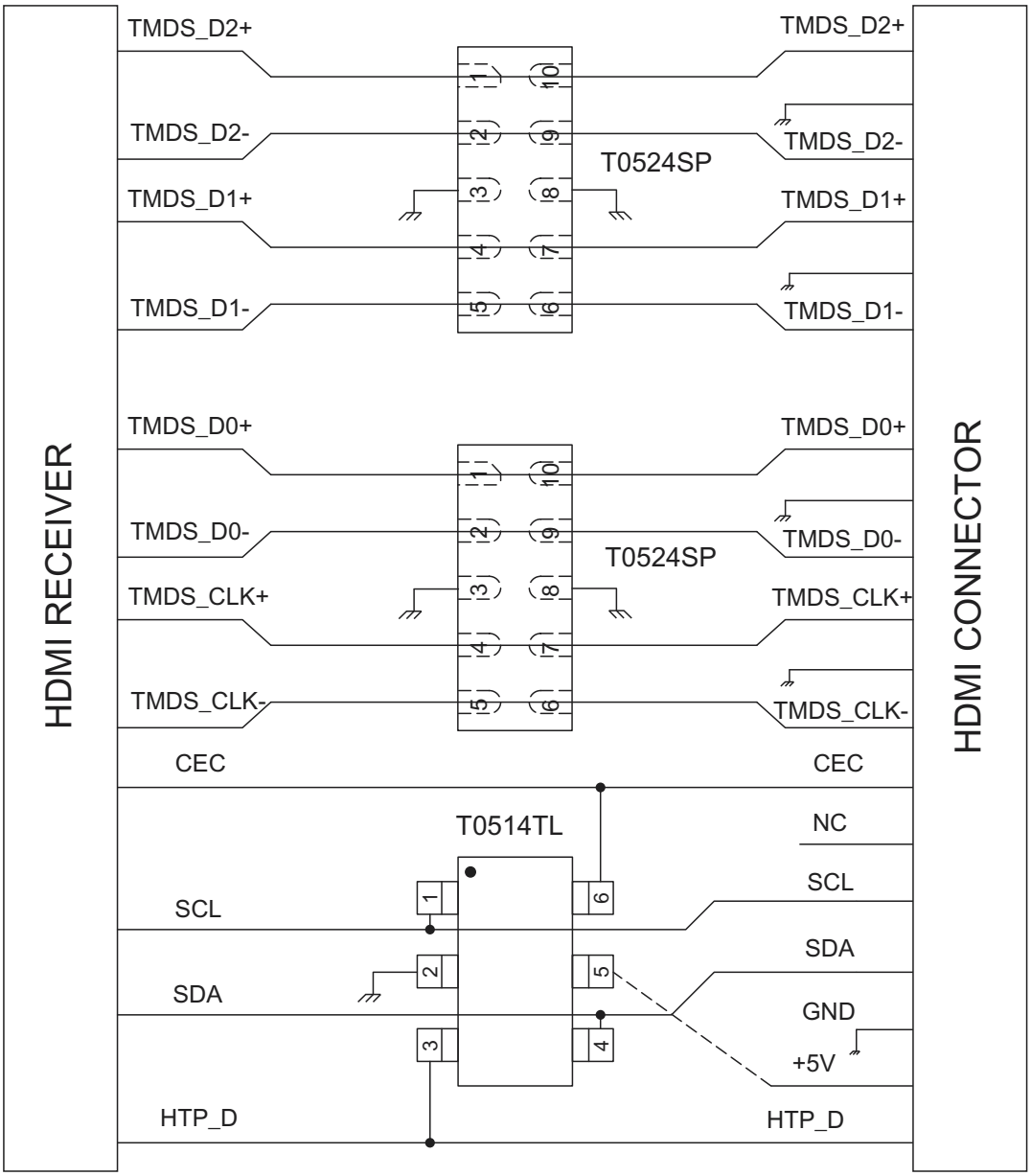
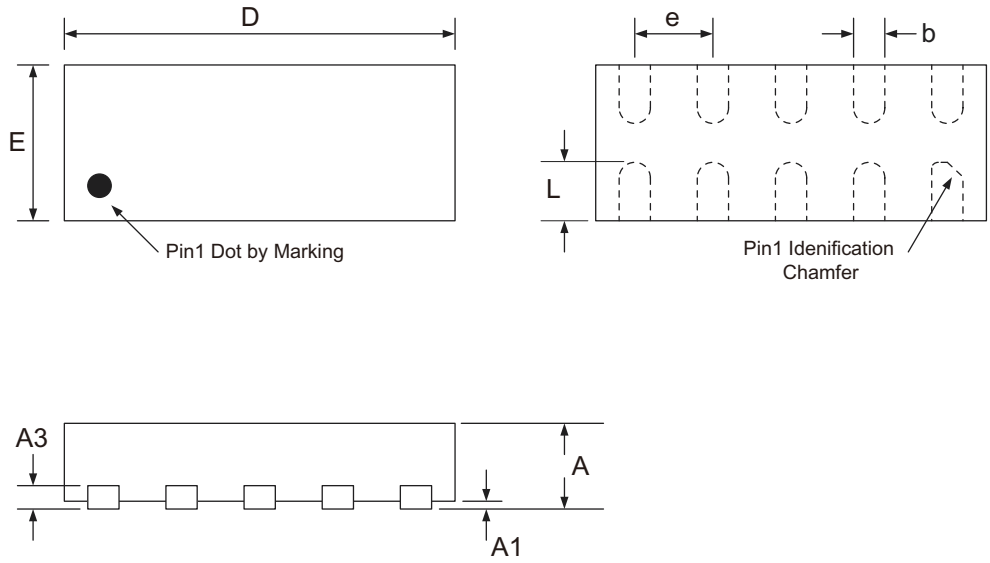



Figure 2 Layout Top View for HDMI Interface With T0524SP & T0514TL

## Package Outline

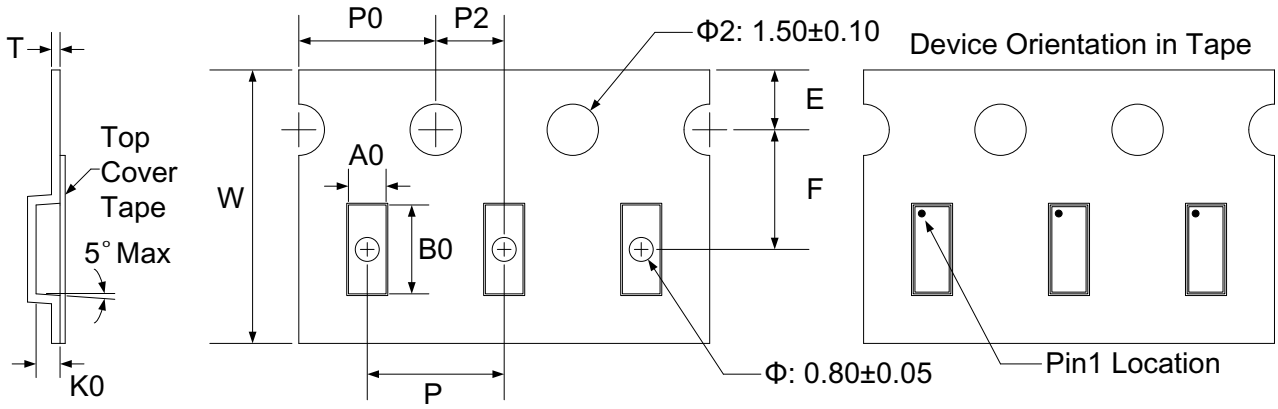
DFN2510-10L package
Thermally-Enhanced
MSL-1 Level




Package Dimensions (Controlling dimensions are in millimetes)

| Symbol | Dimensions (mm) | | Dimensions (inch) | |
|---|---|---|---|---|
| | Minimum | Maximum | Minimum | Maximum |
| A | 0.500 | 0.600 | 0.020 | 0.024 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.150REF. | | 0.006REF. | |
| b | 0.150 | 0.250 | 0.006 | 0.010 |
| D | 2.450 | 2.550 | 0.096 | 0.100 |
| E | 0.950 | 1.050 | 0.037 | 0.041 |
| e | 0.500 BSC | | 0.020 BSC | |
| L | 0.300 | 0.400 | 0.012 | 0.016 |

## Tape and Reel Specification




| Symbol | W | A0 | B0 | K0 | E | F | P | P0 | P2 | T |
|---|---|---|---|---|---|---|---|---|---|---|
| Dimensions (mm) | 8.00+0.3 -0.1 | 1.23±0.05 | 2.7±0.05 | 0.7±0.05 | 1.75±0.1 | 3.5±0.05 | 4.0±0.1 | 4.0±0.1 | 2.0±0.05 | 0.25±0.02 |

## Marking Codes


Note:

(1) "T54SP" is part number, fixed.

## Ordering Information

| Part Number | Working Voltage | Quantity Per Reel | Reel Size |
|---|---|---|---|
| T0524SP | 5V | 3,000 | 7 Inch |

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