

# SRAM

# 128K X 8 LOW POWER CMOS STATIC RAM

## FEATURES

- Low-power consumption
  - Active: 40mA at 55ns
  - Stand-by: (CMOS input/output)
    - 0 ~ +70 °C = 15uA
    - 40 ~ +85 °C = 20uA
- 55/70/100 ns access time
- Equal access and cycle time
- Single +5V (±10%) Power Supply
- TTL compatible , Tri-state output
- Common I/O capability
- Automatic power-down when deselected
- Available in 32-pin SOP ,TSOP-I(8x20mm), TSOP-I(8x13.4mm) and DIP (600 mil) package.

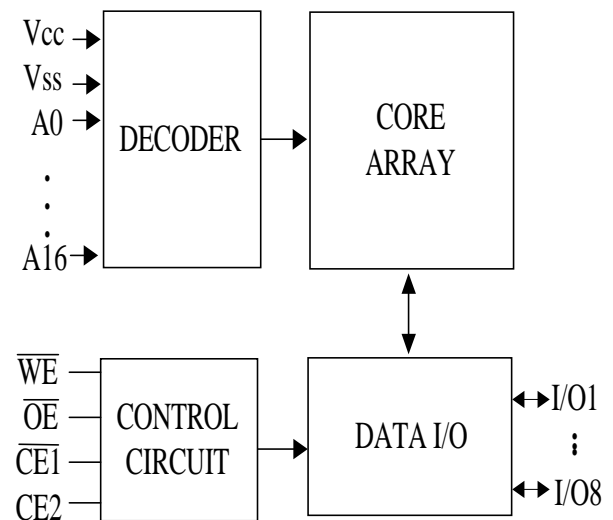
## PART NUMBER EXAMPLES

PART NO.	PACKAGE CODE	Operating Temperature
T15M1024A-55D	D=SOP	0 ~ +70 °C
T15M1024A-70H	H=TSOP-I(8x20)	
T15M1024A-100P	P=TSOP-I(8x13.4)	
T15M1024A-100N	N=DIP (600 mil)	
T15M1024A-55DI	D=SOP	-40 ~ +85 °C
T15M1024A-70HI	H=TSOP-I(8x20)	
T15M1024A-100PI	P=TSOP-I(8x13.4)	
T15M1024A-100NI	N=DIP (600 mil)	

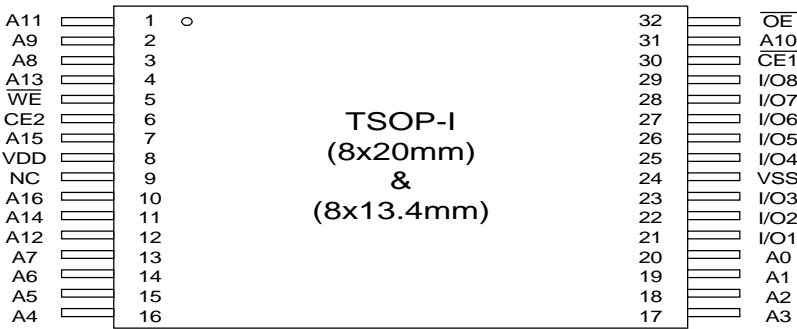
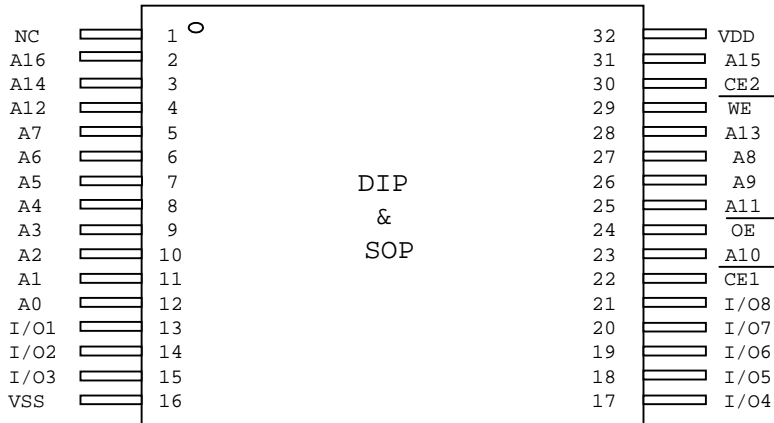
## GENERAL DESCRIPTION

The T15M1024A is a very Low Power CMOS Static RAM organized as 131,072 words by 8 bits. That operates on a wide voltage range from +5V (±10%) power supply, Fabricated using high performance CMOS technology, Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures. Data retention is guaranteed at a power supply voltage as low as 1.5V.

## BLOCK DIAGRAM



**PIN CONFIGURATIONS**



**PIN DESCRIPTIONS**

SYMBOL	DESCRIPTIONS	SYMBOL	DESCRIPTIONS
A0 ~ A16	Address inputs	$\overline{OE}$	Output enable input
I/O1~I/O8	Data inputs/outputs	VDD	Power supply
$\overline{CE1}$ , $\overline{CE2}$	Chip enable	VSS	Ground
$\overline{WE}$	Write enable input	NC	No connection

**ABSOLUTE MAXIMUM RATINGS\***

PARAMETER	SYM	MIN.	MAX.	UNIT
Voltage on Any Pin Relative to Gnd	V <sub>R</sub>	-0.5	+7 V	V
Power Dissipation	P <sub>D</sub>	-	0.7	W
Storage Temperature	T <sub>STG</sub>	-55	+150	°C
Temperature Under Bias	I <sub>BIAS</sub>	0/-40	+70/+85	°C

\*Note: Stresses greater than those listed above Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and function operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**TRUTH TABLE**

CE 1	CE2	WE	OE	DATA	MODE
H	X	X	X	High-Z	Standby
X	L	X	X	High-Z	Standby
L	H	H	L	Data Out	Active, Read
L	H	H	H	High-Z	Active, Output Disable
L	H	L	X	Data In	Active, Write

\*Note: X = Don't Care, L = Low, H = High

**OPERATING CHARACTERISTICS**

 (V<sub>CC</sub> = +5V / ±10%, G<sub>ND</sub> = 0V, T<sub>a</sub> = 0 ~ +70 °C / -40°C ~ 85°C)

PARAMETER	SYM.	TEST CONDITIONS	-55		-70		-100		UNIT	
			Min	Max	Min	Max	Min	Max		
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> = Max, V <sub>IN</sub> = Gnd to V <sub>CC</sub>	-	1	-	1	-	1	uA	
Output Leakage Current	I <sub>LO</sub>	$\overline{CE1} = V_{IH}$ or CE2= V <sub>IL</sub> or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ V <sub>OUT</sub> = Gnd to V <sub>CC</sub>	-	1	-	1	-	1	uA	
Operating Power Supply Current	I <sub>CC</sub>	$\overline{CE1} = V_{IL}$ , CE2= V <sub>IH</sub> , $\overline{WE} = V_{IH}$ , $\overline{OE} = V_{IH}$ , V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OUT</sub> =0mA	-	2	-	2	-	2	mA	
Average Operating Current	I <sub>CC1</sub>	Cycle time=1us, 100% duty, I <sub>OUT</sub> =0mA, $\overline{CE1} \leq 0.2V$ , CE2 ≥ V <sub>CC</sub> -0.2V, V <sub>IN</sub> ≤ 0.2V	-	3	-	3	-	3	mA	
	I <sub>CC2</sub>	Cycle time=min, 100% duty, I <sub>OUT</sub> =0mA, $\overline{CE1} = V_{IL}$ , CE2= V <sub>IH</sub> , V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	-	40	-	35	-	25	mA	
Standby Power Supply Current (TTL Level)	I <sub>SB</sub>	$\overline{CE1} = V_{IH}$ CE2= V <sub>IL</sub>	-	0.5	-	0.5	-	0.5	mA	
Standby Power Supply Current (CMOS Level)	I <sub>SBI</sub>	$\overline{CE1} \geq V_{CC}-0.2V$ , CE2 ≥ V <sub>CC</sub> -0.2V or CE2 ≤ 0.2V V <sub>IN</sub> ≤ 0.2V or V <sub>IN</sub> ≥ V <sub>CC</sub> -0.2V	0°C to 70°C	-	15	-	15	-	15	uA
			-40°C to 85°C	-	20	-	20	-	20	
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.1mA	-	0.4	-	0.4	-	0.4	V	
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1.0 mA	2.4	-	2.4	-	2.4	-	V	

**RECOMMENDED OPERATING CONDITIONS**

(Ta = 0 ~ +70 °C / -40°C to 85°C\*\*)

PARAMETER	SYM	MIN	MAX	UNIT
Supply Voltage	Vcc	4.5	5.5	V
	Gnd	0.0	0.0	V
Input Voltage	V <sub>IH</sub>	0.6Vcc	Vcc+0.3	V
	V <sub>IL</sub>	-0.3	0.4	V

**CAPACITANCE**

(f = 1 MHz, Ta = 25°C,)

PARAMETER	SYMBOL	CONDITION	MAX.	UNIT
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0V	6	pF
Input/ Output Capacitance	C <sub>I/O</sub>	V <sub>IN</sub> = V <sub>OUT</sub> = 0V	8	pF

**Note:** This parameter is guaranteed by device characterization and is not production tested.

**AC TEST CONDITIONS**

PARAMETER	CONDITIONS
Input Pulse Levels	0.4V to 0.6Vcc
Input Rise and Fall Times	5.0 ns
Input and Output Timing Reference Level	1.5V
Output Load	C <sub>L</sub> = 30pF + 1TTL Load (55ns/70ns)
	C <sub>L</sub> = 100pF + 1TTL Load (Load for 100ns)

**AC TEST LOADS AND WAVEFORM**

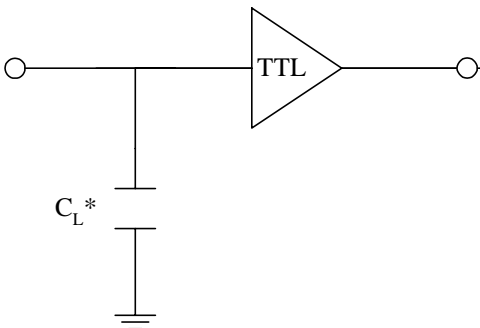


Fig.A \* Including Scope and Jig Capacitance

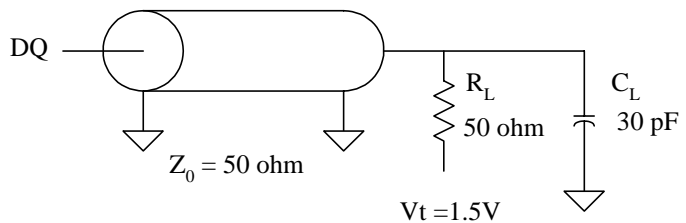


Fig.B Output Load Equivalent

**AC CHARACTERISTICS**

 (V<sub>cc</sub> = +5V / ±10%, Gnd = 0V, Ta = 0 ~ +70 °C / -40°C to 85°C)

**(1) READ CYCLE**

PARAMETER	SYM.	-55		-70		-100		UNIT
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t <sub>RC</sub>	55	-	70	-	100	-	ns
Address Access Time	t <sub>AA</sub>	-	55	-	70	-	100	ns
Chip Enable Access Time	t <sub>ACE</sub>	-	55	-	70	-	100	ns
Output Enable Access Time	t <sub>OE</sub>	-	25	-	35	-	50	ns
Output Hold from Address Change	t <sub>OH</sub>	10	-	10	-	10	-	ns
Chip Enable to Output in Low-Z	t <sub>LZ</sub>	10	-	10	-	10	-	ns
Chip Disable to Output in High-Z	t <sub>HZ</sub>	-	20	-	25	-	30	ns
Output Enable to Output in Low-Z	t <sub>OLZ</sub>	5	-	5	-	5	-	ns
Output Disable to Output in High-Z	t <sub>OHZ</sub>	-	20	-	25	-	30	ns

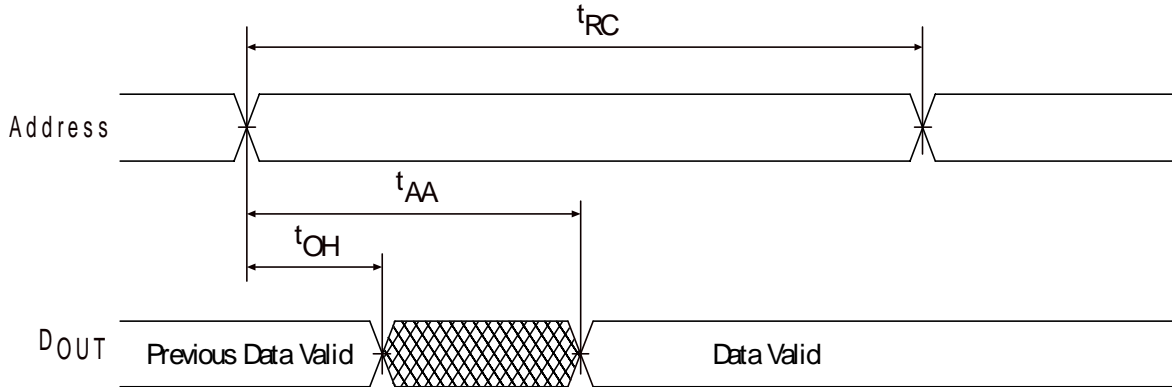
**(2)WRITE CYCLE**

PARAMETER	SYM.	-55		-70		-100		UNIT
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t <sub>WC</sub>	55	-	70	-	100	-	ns
Chip Enable to Write End	t <sub>CW</sub>	50	-	60	-	80	-	ns
Address Valid to Write End	t <sub>AW</sub>	50	-	60	-	80	-	ns
Address Setup Time	t <sub>AS</sub>	0	-	0	-	0	-	ns
Write Pulse Width	t <sub>WP</sub>	45	-	50	-	70	-	ns
Write Recovery Time	t <sub>WR</sub>	0	-	0	-	0	-	ns
Data Valid to Write End	t <sub>DW</sub>	25	-	30	-	40	-	ns
Data Hold Time	t <sub>DH</sub>	0	-	0	-	0	-	ns
Write Enable to Output in High-Z	t <sub>WHZ</sub>	-	25	-	25	-	30	ns
Output Active from Write End	t <sub>OW</sub>	5	-	5	-	5	-	ns

**TIMING WAVEFORMS**

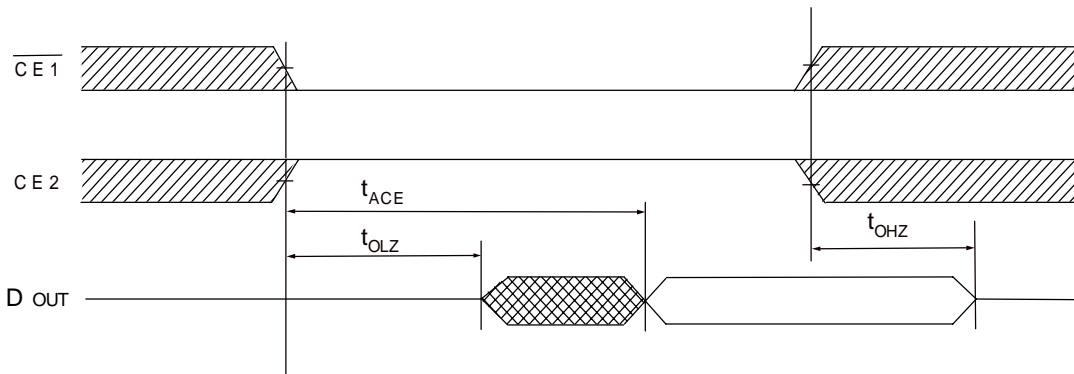
**READ CYCLE 1**



(Address Controlled)



**READ CYCLE 2**

(Chip Enable Controlled)

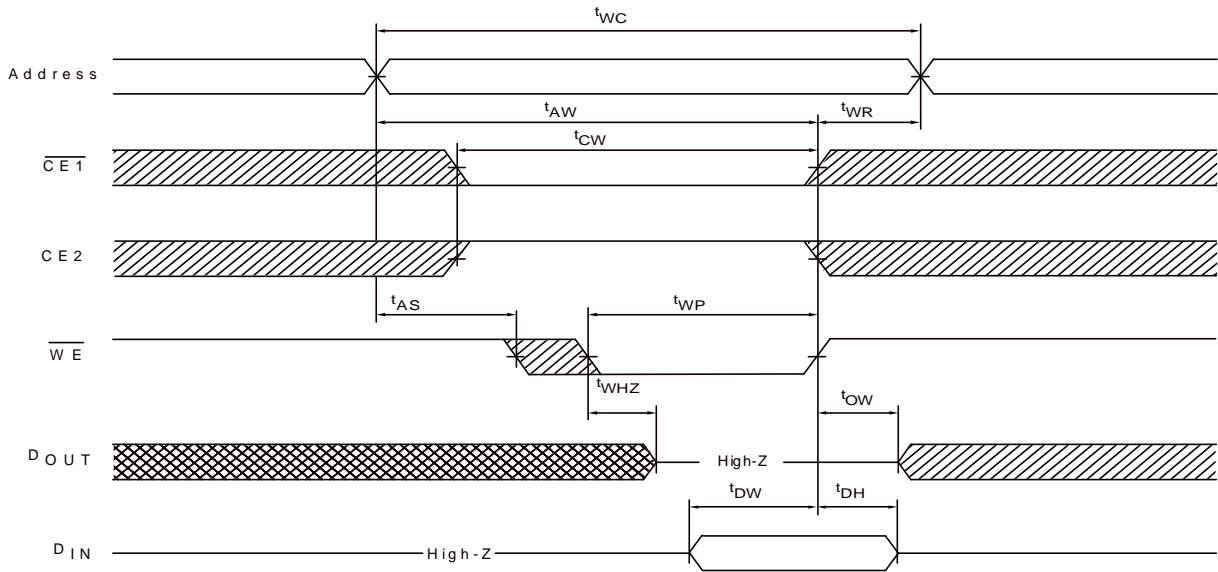


 DON'T CARE  
 UNDEFINED

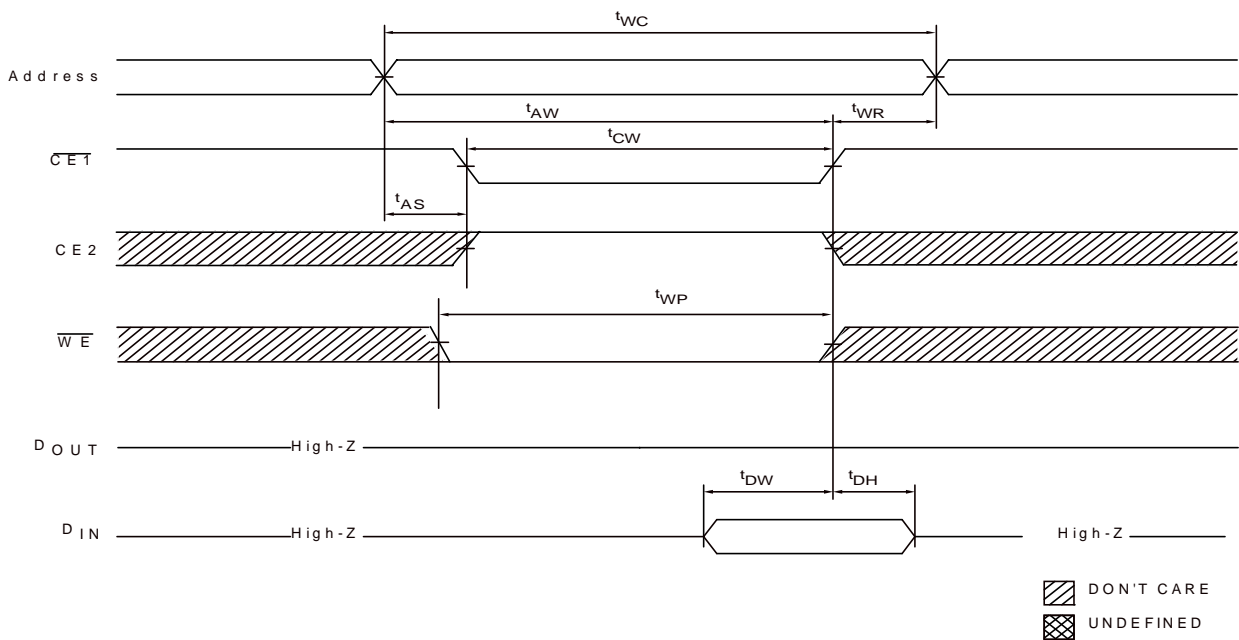
Notes (READ CYCLE) :

1.  $\overline{WE}$  are high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit condition referenced to  $V_{OH}$  or  $V_{OL}$  levels.
4. At any given temperature and voltage condition.  $t_{HZ}$  (max.) is less than  $t_{LZ}$  (min.) both for a given device and from device to device interconnection.
5. Transition is measured  $\pm 200mV$  from steady state voltage with load. This parameter is sampled and not 100% tested.
6. Device is continuously selected with  $\overline{CE1} = V_{IL}$ .

WRITE CYCLE 1 ( $\overline{WE}$  Controlled)



WRITE CYCLE 2 ( $\overline{CE}$  Controlled)



 DON'T CARE  
 UNDEFINED

NOTES ( WRITE CYCLE ) :

1. A write occurs during the overlap of a low  $\overline{CE1}$ , a high  $\overline{CE2}$  and a low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CE1}$  goes low,  $\overline{CE2}$  going high and  $\overline{WE}$  going low. A write ends at the earliest transition among  $\overline{CE1}$  going high,  $\overline{CE2}$  going low and  $\overline{WE}$  going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the later of  $\overline{CE1}$  going low or  $\overline{CE2}$  going high to the end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.



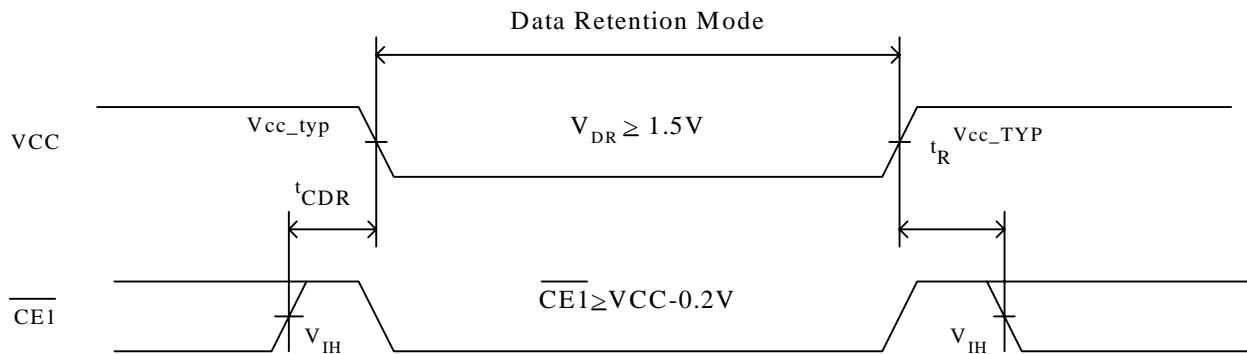
**DATA RETENTION CHARACTERISTICS**

PARAMETER	SYM.	TEST CONDITION	MIN.	MAX.	UNIT
V <sub>CC</sub> for Data Retention	V <sub>DR</sub>	$\overline{CE1} \geq V_{DD} - 0.2V$	1.5	-	V
Data Retention Current	I <sub>CCDR</sub>	$CE2 \leq 0.2V$	-	5*	uA
Chip Deselect to Data Retention Time	t <sub>CDR</sub>	$V_{IN} \geq V_{CC} - 0.2V$ or	0	-	ns
Operation Recovery Time	t <sub>R</sub>	$V_{IN} \leq 0.2V$	t <sub>RC</sub>	-	ns

\* 0 ~ +70 °C / -40 ~ +85 °C, V<sub>CC</sub>=3V

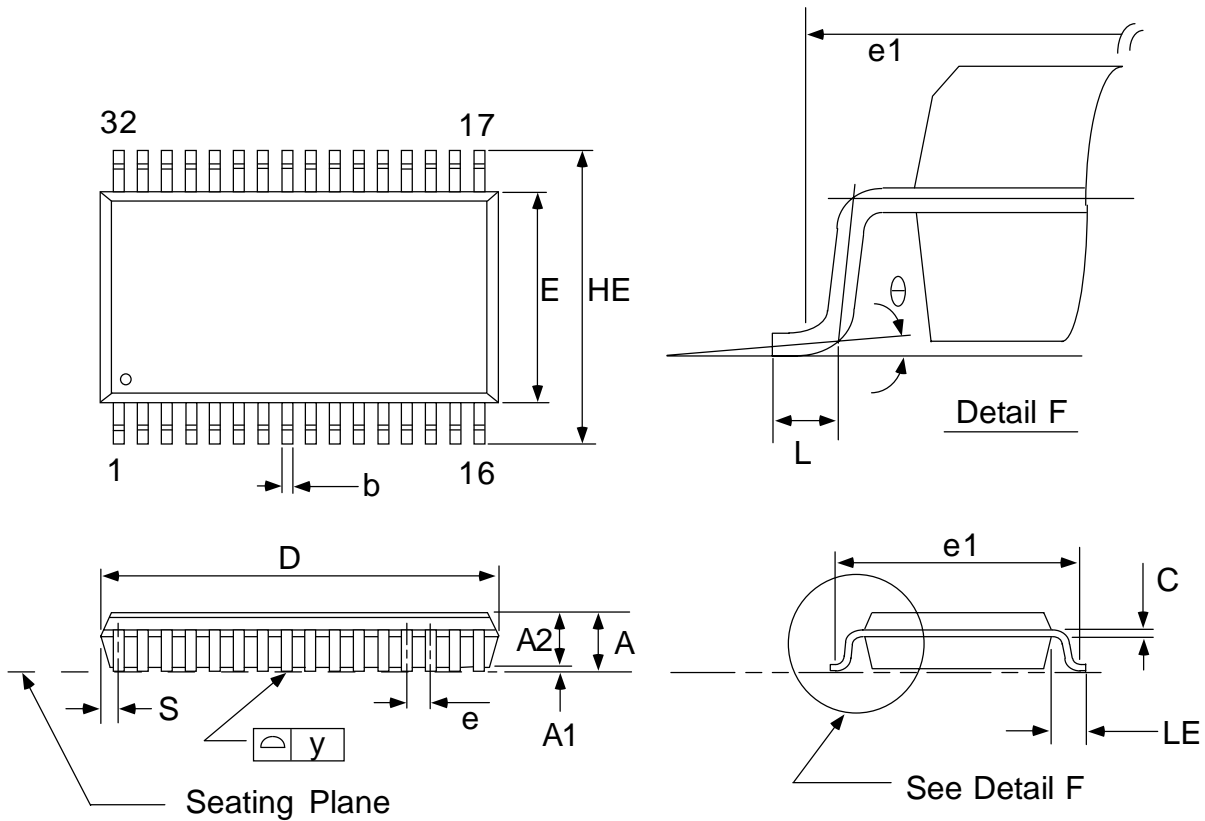
**DATA RETENTION WAVEFORM**

(T<sub>a</sub> = 0 ~ +70 °C / -40°C to 85°C)



**PACKAGE DIMENSIONS**

**32-LEAD SOP**



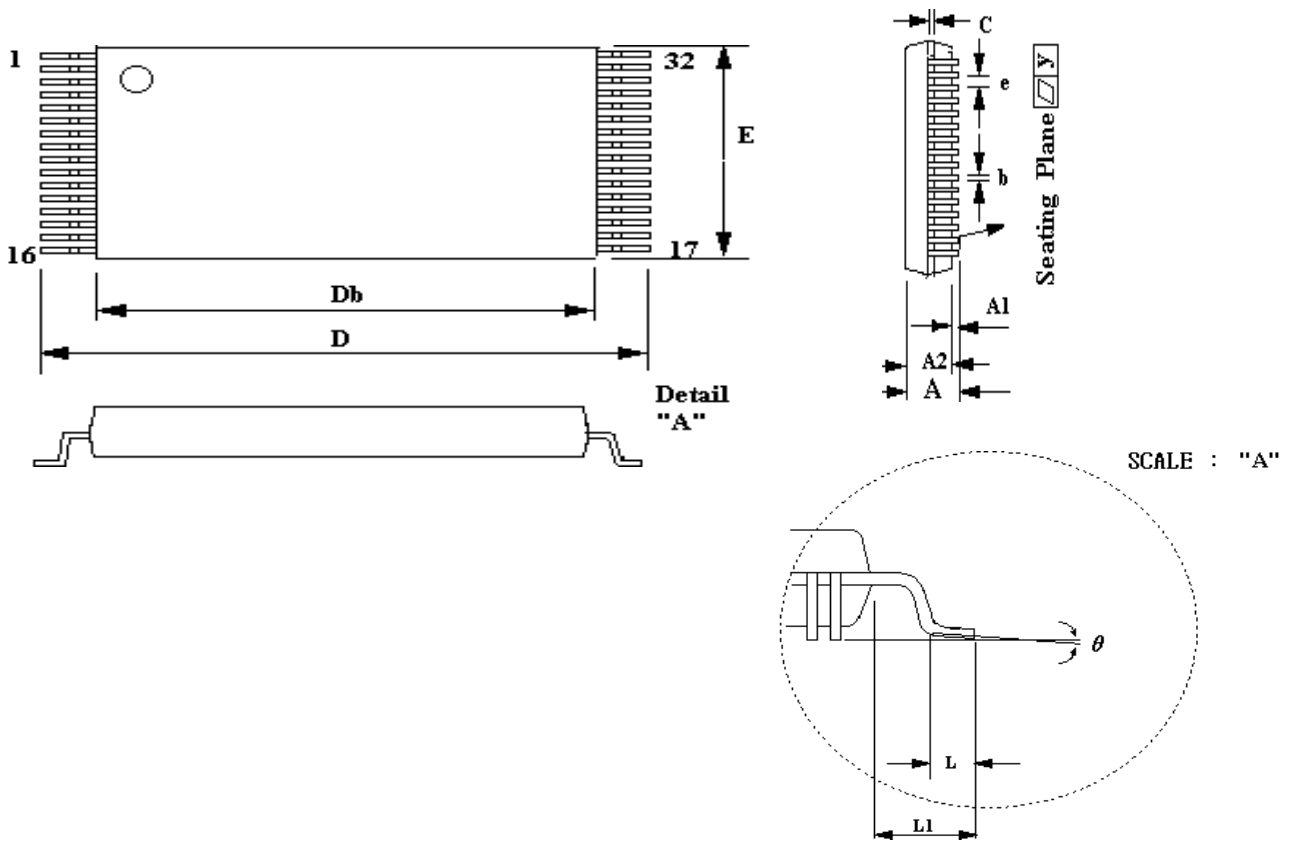
Symbol	Dimension in inches			Dimension in mm		
	min.	typ.	max	min.	typ.	max.
<b>A</b>	-	-	0.118	-	-	3.00
<b>A1</b>	0.004	-	-	0.10	-	-
<b>A2</b>	0.101	0.106	0.111	2.57	2.69	2.82
<b>b</b>	0.014	0.016	0.020	0.36	0.41	0.51
<b>C</b>	0.006	0.008	0.012	0.15	0.20	0.31
<b>D</b>	-	0.805	0.817	-	20.45	20.75
<b>E</b>	0.440	0.445	0.450	11.18	11.30	11.43
<b>e</b>	0.044	0.050	0.056	1.12	1.27	1.42
<b>HE</b>	0.546	0.556	0.556	13.87	14.12	14.38
<b>L</b>	0.023	0.031	0.039	0.58	0.79	0.99
<b>LE</b>	0.047	0.055	0.063	1.19	1.40	1.60
<b>S</b>	-	-	0.036	-	-	0.91
<b>y</b>	-	-	0.004	-	-	0.10
<b>θ</b>	0°	-	10°	0°	-	10°

Notes :

1. Dimensions D max. & S include mold flash or tie bar burrs.
2. Dimension b does not include dambar protrusion / intrusion.
3. Dimensions D & E include mold mismatch and determined at the mold parting line.
4. controlling dimension : inches
5. general appearance spec should be based on final visual inspection spec.

**PACKAGE DIMENSIONS**

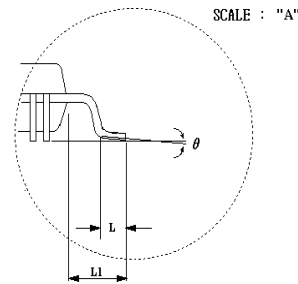
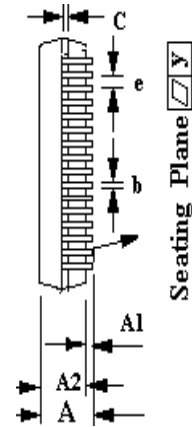
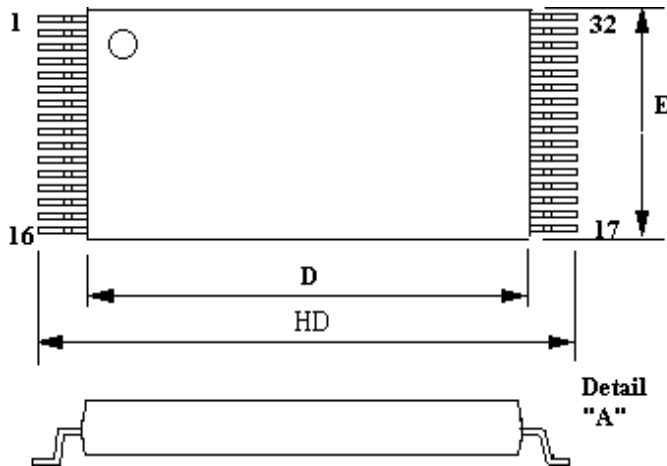
**32-LEAD TSOP (8x20mm)**



SYMBOL	DIMENSIONS IN INCHES			DIMENSIONS IN MM		
	MIN	NOM	MAX	MIN	NOM	MAX
A	--	-	0.047	-	-	1.20
A1	0.002	-	0.006	0.05	-	0.15
A2	0.035	0.040	0.041	0.90	1.00	1.05
b	0.007	0.008	0.011	0.17	0.20	0.27
C	0.004	0.006	0.008	0.10	0.15	0.21
D	0.787 TYP			20.00 TYP		
Db	0.724 TYP			18.40 TYP		
E	0.315 TYP			8.00 TYP		
L	0.020	0.024	0.028	0.598	0.610	0.622
L1	0.032 TYP			0.813 TYP		
$\theta$	0°~12°			0°~12°		

**PACKAGE DIMENSIONS**

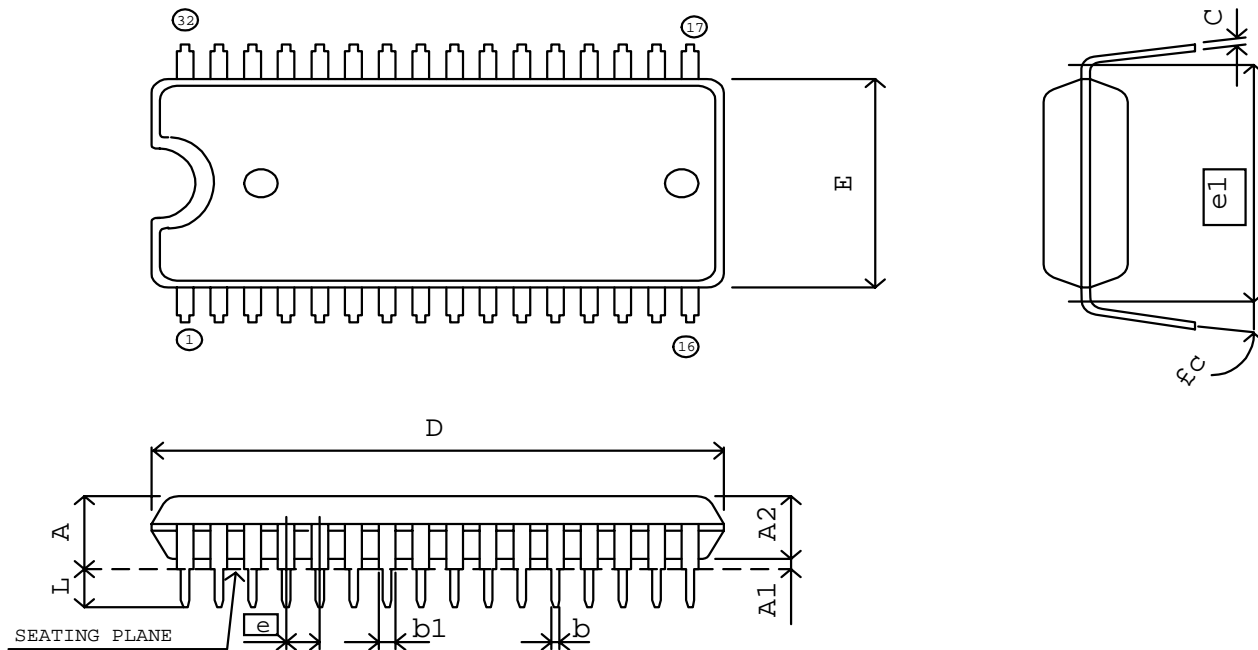
**32-LEAD TSOP-I (8x13.4mm)**



SYMBOL	Dimension in inches	Dimension in mm
A	0.044(MAX)	1.10(MAX)
A1	0.004±0.002	0.05±0.05
A2	0.041(MAX)	1.02(MAX)
b	0.008±0.004	0.20±0.10
C	0.006±0.001	0.15±0.02
D	0.465±0.008	11.8±0.2
E	0.315±0.004	8.0±0.1
HD	0.528±0.008	13.4±0.2
e	0.020(TYP.)	0.5(TYP.)
L	0.020±0.004	0.5±0.1
L1	0.031±0.008	0.8±0.2
y	0.002(MAX)	0.05(MAX)
θ	0° ~ 5°	0° ~ 5°

**PACKAGE DIMENSIONS**

**32-LEAD DIP (600mil)**



Symbol	Dimension in inches			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.200	-	-	5.08
A1	0.015	-	-	0.38	-	-
A2	0.142	0.150	0.158	3.61	3.81	4.01
b	0.014	0.018	0.022	0.36	0.46	0.56
b1	0.056	0.060	0.064	1.42	1.52	1.62
C	0.008	0.010	0.014	0.20	0.25	0.35
D	1.642	1.650	1.658	41.71	41.91	42.11
E	0.527	0.535	0.543	13.40	13.60	13.80
e	-	0.100	-	-	2.54	-
e1	-	0.600	-	-	15.24	-
L	0.118	0.130	0.142	3.00	3.30	3.60
θ	0 ~ 15°					