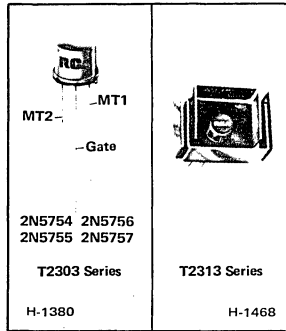




Thyristors

2N5754 - 2N5757

T2303 T2313 Series



2.5-A Silicon Triacs

Features:

- 25/40 mA IGT
- Shorted-Emitter, Center-Gate Design
- Low Switching Losses
- Low On-State Voltage at High Current Levels

Voltage	100 V Types	200 V Types	400 V Types	600 V Types
Package				
Modified TO-5 (T2303 Series)	2N5754	2N5755	2N5756	2N5757
Modified TO-5 with Heat Rad. (T2313-Series)	T2313A (40684)	T2313B (40685)	T2313D (40686)	T2313M (40687)

Numbers in parentheses (e.g. 40684) are former RCA type numbers.

These RCA triacs are gate-controlled full-wave silicon ac switches that are designed to switch from an off-state to an on-state for either polarity of applied voltage with positive or negative gate triggering voltages.

The gate sensitivity of these triacs permits the use of economical transistorized control circuits and enhances their use in low-power phase control and load-switching applications.

MAXIMUM RATINGS, Absolute-Maximum Values:

For operation with sinusoidal supply voltage at frequencies up to 50/60 Hz and with resistive or inductive load.

	2N5754 T2313A	2N5755 T2313B	2N5756 T2313D	2N5757 T2313M	
*REPETITIVE PEAK OFF-STATE VOLTAGE: [○] Gate open, $T_J = -65$ to 100°C	100	200	400	600	V
RMS ON-STATE CURRENT (Conduction angle = 360°): Case temperature $T_C = 70^\circ\text{C}$ (T2303-Series)					2.5
Ambient temperature $T_A = 25^\circ\text{C}$ (T2313-Series)					1.9
For other conditions					See Fig.2,3,4, & 5
PEAK SURGE (NON-REPETITIVE) ON-STATE CURRENT: For one cycle of applied principal voltage, $T_C = 70^\circ\text{C}$					I _{TSM}
60 Hz (sinusoidal)					25
50 Hz (sinusoidal)					21
For more than one cycle of applied principal voltage.					See Fig.6
RATE OF CHANGE OF ON-STATE CURRENT: $V_{DM} = V_{DROM}$, $I_{GT} = 50$ mA, $t_r = 0.1 \mu\text{s}$ (See Fig.13)					di/dt
FUSING CURRENT (for Triac Protection): $T_J = -65$ to 100°C , $t = 1.25$ to 10 ms					100
*PEAK GATE-TRIGGER CURRENT: [■] For $1 \mu\text{s}$ max.					3
*GATE POWER DISSIPATION: PEAK (For $10 \mu\text{s}$ max.)					1
AVERAGE: $T_C = 70^\circ\text{C}$					10
$T_A = 25^\circ\text{C}$					0.15
*TEMPERATURE RANGE: [▲] Storage					0.05
Operating (Case)					-65 to 150
LEAD TEMPERATURE (During soldering): At distance $1/32$ in. (0.8 mm) from seating plane for 10 s max.					-65 to 100
					225

[○] In accordance with JEDEC registration data format (JS-14, RDF-2 filed for the JEDEC (2N-Series) types.
 [■] For either polarity of gate voltage (V_G) with reference to main terminal 1.
[▲] For temperature measurement reference point, see Dimensional Outline.

ELECTRICAL CHARACTERISTICS

At Maximum Ratings and at Indicated Case Temperature (T_C) Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	LIMITS			UNITS																												
		Min.	Typ.	Max.																													
* Peak Off-State Current: ↓ Gate Open, T _J = 100°C and V _{DROM} = Max. rated value	I _{DROM}	-	0.2	0.75	mA																												
Maximum On-State Voltage: ↓ For I _T = 10 A (peak) and T _C = 25°C..... For I _T = 3.5 A (peak) and T _C = 25°C.....	V _{TM}	-	2.2	2.6 1.8	V																												
DC Holding Current: ↓ Gate Open, Initial principal current = 150 mA (DC), V _D = 12 V At T _C = 25°C..... At T _C = -65°C..... For other case temperatures.....	I _{HO}	-	6 20	35 82*	mA																												
Critical Rate of Rise of Commutation Voltage: ↓ For V _D = V _{DROM} , I _{T(RMS)} = 2.5 A, commutating di/dt = 0.95 A/ms, gate unenergized, T _C = 70°C (See Fig. 13).....	dv/dt	0.5	-	-	V/μs																												
* Critical Rate-of-Rise of Off-State Voltage: ↓ For V _D = V _{DROM} , exponential voltage rise, and gate open, T _C = 100°C	dv/dt	10	100	-	V/μs																												
DC Gate-Trigger Current: ↓ † For V _D = 12 V (DC), R _L = 30 Ω, and T _C = 25°C T _C = -65°C For other case temperatures.....	<table border="1"> <thead> <tr> <th>Mode</th> <th>V_{MT2}</th> <th>V_G</th> </tr> </thead> <tbody> <tr> <td>I⁺</td> <td>positive</td> <td>positive</td> </tr> <tr> <td>III⁻</td> <td>negative</td> <td>negative</td> </tr> <tr> <td>I⁻</td> <td>positive</td> <td>negative</td> </tr> <tr> <td>III⁺</td> <td>negative</td> <td>positive</td> </tr> <tr> <td>I⁺</td> <td>positive</td> <td>positive</td> </tr> <tr> <td>III⁻</td> <td>negative</td> <td>negative</td> </tr> <tr> <td>I⁻</td> <td>positive</td> <td>negative</td> </tr> <tr> <td>III⁺</td> <td>negative</td> <td>positive</td> </tr> </tbody> </table>	Mode	V _{MT2}	V _G	I ⁺	positive	positive	III ⁻	negative	negative	I ⁻	positive	negative	III ⁺	negative	positive	I ⁺	positive	positive	III ⁻	negative	negative	I ⁻	positive	negative	III ⁺	negative	positive	I _{GT}	-	5 5 10 10 30 30 40 40	25 25 40 40 60* 60* 100* 100*	mA
Mode	V _{MT2}	V _G																															
I ⁺	positive	positive																															
III ⁻	negative	negative																															
I ⁻	positive	negative																															
III ⁺	negative	positive																															
I ⁺	positive	positive																															
III ⁻	negative	negative																															
I ⁻	positive	negative																															
III ⁺	negative	positive																															
DC Gate-Trigger Voltage: ↓ † For V _D = 12 V (DC) and R _L = 30 Ω At T _C = 25°C..... At T _C = -65°C..... For other case temperatures..... For v _D = V _{DROM} and R _L = 125 Ω At T _C = 100°C.....	V _{GT}	-	0.9 1.5	2.2 3*	V																												
Thermal Resistance: Steady State: * Junction-to-case..... Junction-to-ambient (2N-series types only).....	R _{θ J-C} R _{θ J-A}	-	-	8.5 150	°C/W °C/W																												

← See Fig. 8. →

← See Fig. 11. →

← See Fig. 12. →

↓ For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1. † For either polarity of gate voltage (V_G) with reference to main terminal 1.

* In accordance with JEDEC registration data format (J5-14, RDF-2).

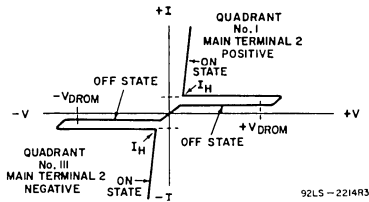


Fig. 1 — Principal voltage-current characteristic.

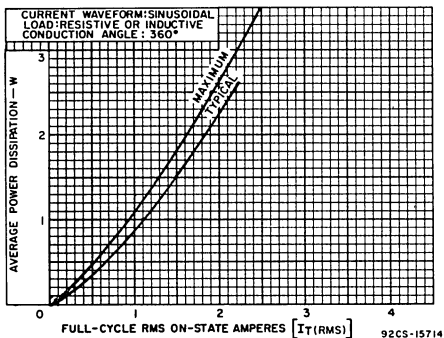


Fig. 2 — Power dissipation vs. on-state current.

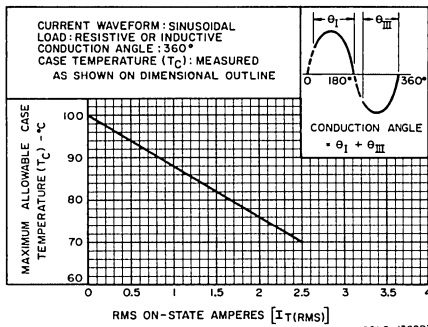


Fig. 3 — Maximum allowable case temperature vs. on-state current.

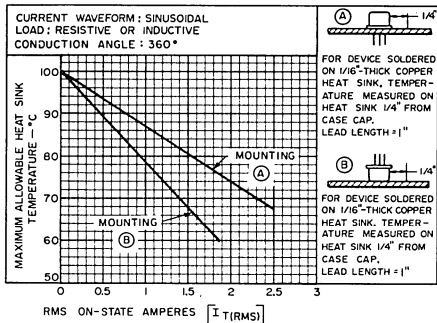


Fig. 4 — Maximum allowable heat-sink temperature vs. on-state current.

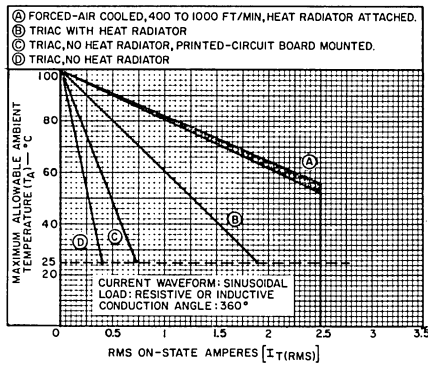


Fig. 5 — Maximum allowable ambient temperature vs. on-state current.

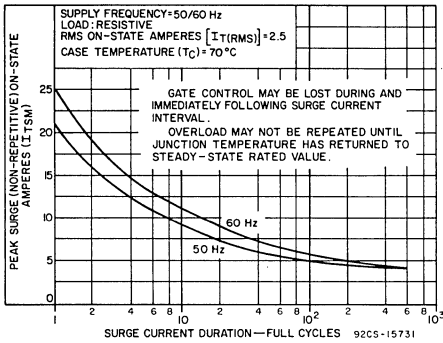


Fig. 6 — Peak surge on-state current vs. surge-current duration.

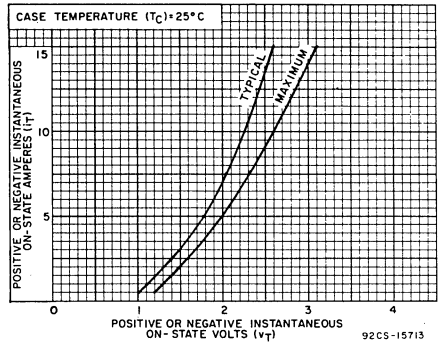


Fig. 7 — On-state current vs. on-state voltage.

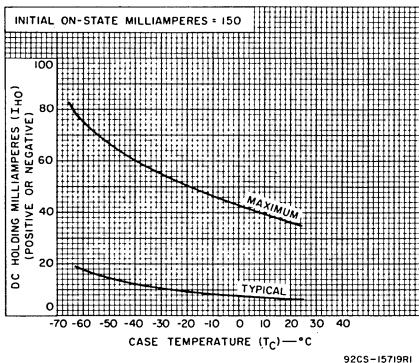


Fig. 8 — DC holding current (positive or negative) vs. case temperature.

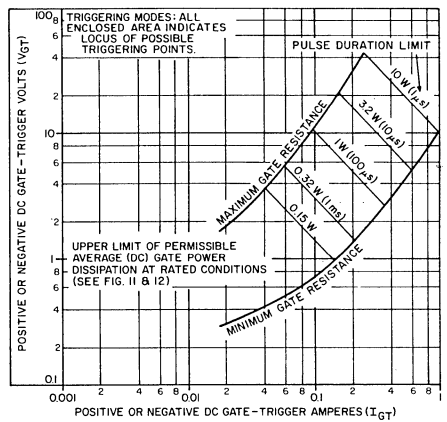
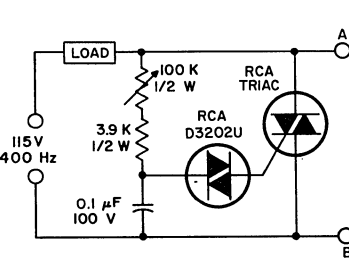
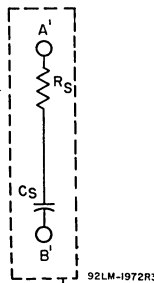


Fig. 9 — Gate trigger characteristics and limiting conditions for determination of permissible gate trigger pulses.



NOTE: For incandescent lamp loads which produce burnout current surges with I^2t values greater than 2.5 ampere² seconds, connect a 10-ohm resistor of appropriate power rating in series with the load. This rating can be determined as follows:
Power Rating of 10-ohm Resistor = $10(\text{rms load current})^2$



AC INPUT VOLTAGE	120 V	240 V
	60 Hz	60 Hz
SNUBBER NETWORK FOR 2.5 A (RMS) INDUCTIVE LOAD	C _S	0.068 μF 200 V
	R _S	0.075 μF 400 V
		2.2 k Ω ½ W
		2.5 k Ω ½ W
RCA TRIACS	2N5755 T2313B	2N5756 T2313D

• For other RMS Current values refer to RCA Application Note AN-4745.

SNUBBER NETWORK FOR INDUCTIVE LOADS. CONNECT POINTS A' AND B' TO TERMINALS A AND B RESPECTIVELY.

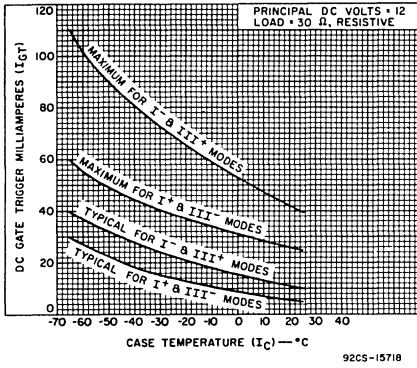


Fig. 11 - DC gate-trigger current vs. case temperature.

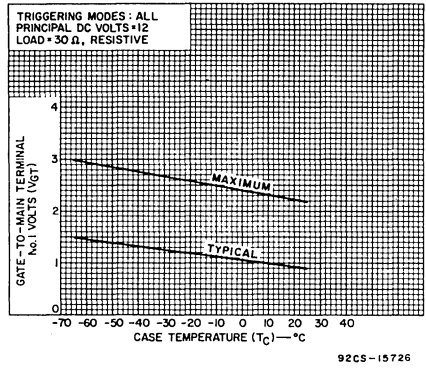


Fig. 12 - DC gate-trigger voltage vs. case temperature.

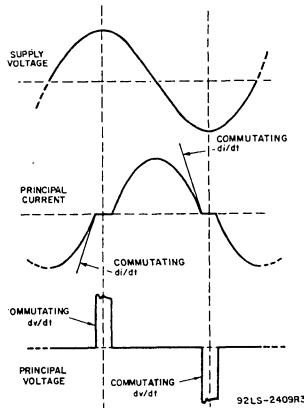


Fig. 13 - Relationship between supply voltage and principle current (inductive load) showing reference points for definition of commutating voltage (dv/dt).

TERMINAL CONNECTIONS

For Types 2N5754, 2N5755, 2N5756, 2N5657

- Lead No. 1 - Main terminal 1
- Lead No. 2 - Gate
- Case, Lead No. 3 - Main terminal 2

For T2313 Series

- Lead No. 1 - Main terminal 1
- Lead No. 2 - Gate
- Heat Rad., Lead No. 3 - Main terminal 2