

T41ZN

Smart Video Application Processor

Data Sheet

Version 0.5

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北京君正集成电路股份有限公司
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Contents

Preface	i
1 Overview	1
1.1 Product Description	1
1.2 Application Scenarios	2
2 Features	4
2.1 CPU	4
2.2 MCU	4
2.3 AI Engine	4
2.4 AI Pre/Post-Processing(AIP)	4
2.5 Video Processor Unit	4
2.6 Image Signal Processor	4
2.7 2D Graphics Engine	5
2.8 Display Process Controller	5
2.9 Video Input	6
2.10 Video Output	6
2.11 Audio System	6
2.12 Memory	6
2.13 System Functions	6
2.14 Peripherals	8
2.15 Boot	9
2.16 Security Engine	9
2.17 RTC with an independent Power Supply	9
2.18 Physical Specifications	9
3 Characteristic	10
4 Package and Pinout	11

4.1 Overview	11
4.2 Solder Process	11
4.3 Moisture Sensitivity Level	11
4.4 T41ZN Package	11
5 Pin Description	15
5.1 Static Memory/DVP/SMB/SSI/DMIC	15
5.2 SFC	16
5.3 MSCx/PWMx/UARTx/SMBx/SSI1/I2S/GMAC	17
5.4 UARTx/PWMx/SMBx/SSI0/SSI_SLV/I2S	20
5.5 SLCD/PWMx/BT656/UARTx	22
5.6 System Boot Select	23
5.7 System Control	23
5.8 Digital IO/CORE Power/Ground	24
5.9 DDR PHY IO and Power Supply	24
5.10 USB 2.0 PHY IO and Power Supply	25
5.11 MIPI-CSI IO and Power Supply	25
5.12 Successive Approximation ADC(SAR-ADC) IO and Power Supply	26
5.13 Audio CODEC IO and Power Supply	26
5.14 OTP IO and Power Supply	26
5.15 OSC and PLL IO and Power Supply	27
5.15.1 Electrical Characteristics	27
5.16 The Ball Assignment of T41ZN	29
6 Electrical Specifications	33
6.1 Power Consumption Parameters	33
6.2 Recommended Operating Conditions	33
6.3 General Purpose Input/Output(GPIO)	35
6.3.1 Power Domain VDDIO18 DC Characteristics	35
6.4 Audio Codec	36
6.4.2 Analog Interface Description	36
6.5 USB 2.0 OTG PHY	37
6.5.1 DC/AC Specifications	37
6.6 Power On, Reset and BOOT	39
6.6.1 Power-On Sequence	39

6.6.2 Reset procedure	40
6.6.3 BOOT	41
7 Thermal Characteristics	44
7.1 Temperature and Thermal Resistance Parameters	44
8 Interface Timings	45
8.1 SFC Interface Timings	45
8.1.1 Propagation Delay	45
8.1.2 AC Timing	45
8.2 Ethernet MAC Port Timings	46
8.2.1 RMIIT Timings	46
8.2.2 MDIO Interface Timings	47
8.3 VI Interface Timing	48
8.3.1 BT/DVP Timings	48
8.3.2 MIPI-CSI Timings	48
8.4 Video Output Interface Timings	49
8.6 I2S Interface Timing	50
8.7 SMB Interface Timing	51
8.8 SSI Timings	52
8.9 SDIO/MMC(MSC) Interface Timings	53
8.10 DMIC Timings	54

Preface

Purpose

This document describes the structures, main features, performance, functions and related address map of each module of T41ZN, it also embraced hardware characteristics such as package, pin usages, electrical specifications, interface timing and so on.


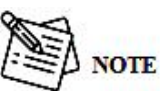
Related Version

The following table lists the product version related to this document.

Product Name	Version
T41ZN	V0.5

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
	Indicates a potentially dangerous situation. If it occurs, it may cause chip damage, data loss, performance impact, etc.
	Interpretation and supplementation of information in the main text.

General Conventions

The general conventions that may be found in this document are defined as follows.

Convention	Description
Times New Roman	Normal paragraphs are in Times New Roman.

Convention	Description
Boldface	Names of files, directories, folders, and users are in boldface .
<i>Italic</i>	Book titles are in <i>italics</i> .

Table Content Conventions

The table content conventions that may be found in this document are defined as follows.

Content	Description
-	The cell is blank.
TBD	The value is to be determined.

Numerical System

The expressions of data capacity, frequency, and data rate are described as follows.

Type	Symbol	Value
Data capacity (such as the RAM capacity)	K	1024
	M	1,048,576
	G	1,073,741,824
Frequency, data rate	k	1000
	M	1,000,000
	G	1,000,000,000

The expressions of addresses and data are described as follows.

Symbol	Example	Description
0x	0xFE04, 0x18	Address or data in hexadecimal
0b	0b000, 0b00 00000000	Data or sequence in binary (register description is excluded.)
X	00X, 1XX	In data expression, X indicates 0 or 1. For example, 00X indicates 000 or 001 and 1XX indicates 100, 101, 110, or 111.

Change History

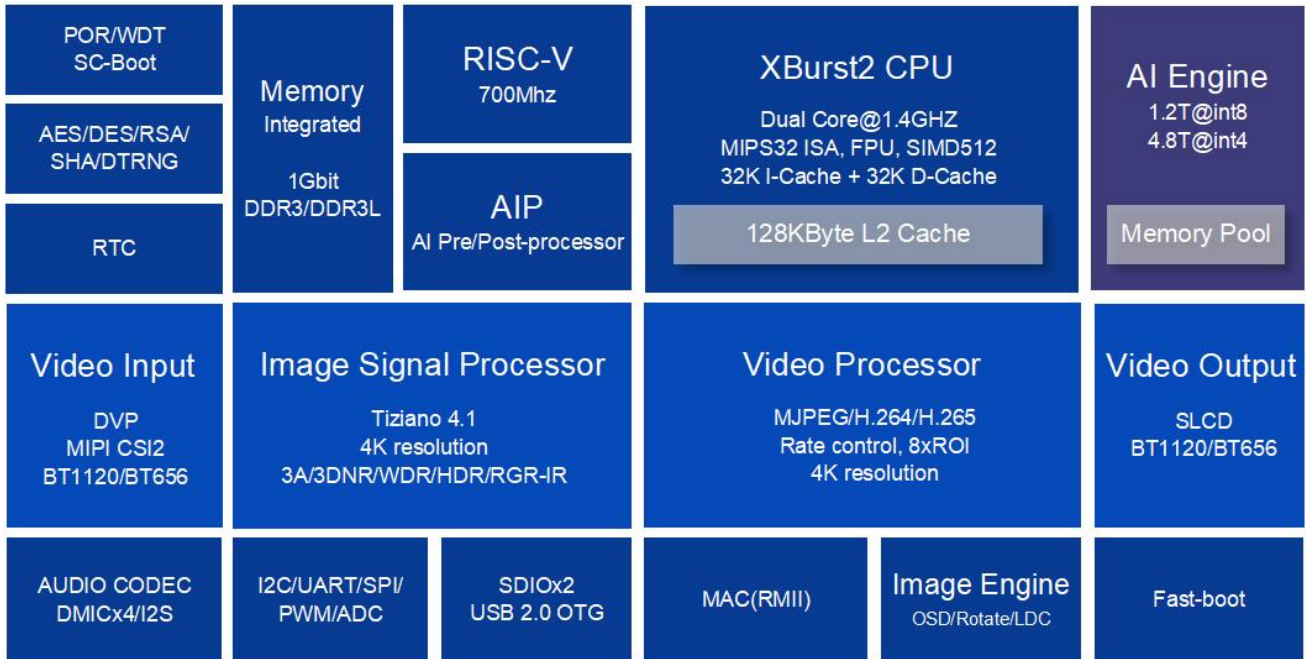
The latest document version contains all changes made in previous versions.

Revision Date	Version	Description
2022-07-11	V0.5	This version is the first draft release.

1 Overview

1.1 Product Description

Figure1- 1 Application block diagram of the T41ZN



T41ZN is a new-generation professional smart video application processor targeting for video devices like mobile camera, security survey, video talking, video analysis and so on. It integrates a new generation 4K resolutions ISP and latest H264/H265/JPEG Comb-Video Compression Encoder to lead the industry in high-quality image and low bit rate. For reducing bandwidth and memory size, on-the-fly mode of ISP and Video Encoder is supported in T41ZN, utilizing this technique, you can easily develop 4M resolution solution using small size DDR.

T41ZN also integrated a low power and high performance AI engine, which has a typical performance of 1.2Tops@int8, it also support 2N bit width, such as 2/4/6/8/10/12/14/16 bits, which can be configured optional.

T41ZN also integrated the RTC, POR, DMIC and Audio Codec to reduce custom’s EBOM cost and simplify the development of custom’s products.

XBurst®-2 processor engine is embedded in T41ZN. XBurst®-2 is an industry leading microprocessor core which delivers superior high performance and best-in-class low power consumption. A hardware floating-point unit which compatible with IEEE754 2008 and MIPS32 ISA R5 SMID plus MIPS SIMD instruction set architecture:512bit MSA also included.

The VPU (Video Processing Unit) core is a video encoder engine designed to process video streams using the HEVC(ISO/IEC 23008-2 High Efficiency Video Coding) and AVC(ISO/IEC 14496-10 Advanced Video Coding) standards. It also supports still picture encoding using the JPEG standard(ITU T.81). The maximum resolution of 3840x2160 in the format of HEVC/AVC/JPEG are supported in encoding. In terms of entropy coding format, AVC supports CAVLC / CABAC, hevc supports CABAC, and JPEG supports Huffman coding.

The ISP core of T41ZN can supports maximum 3840x2160@20fps with excellent image processing including 2D/3D and Chroma denoise, 3A statistical information output, WDR/HDR, lens shading and so on. The input interface can support DVP, MIPI and LVDS interface.

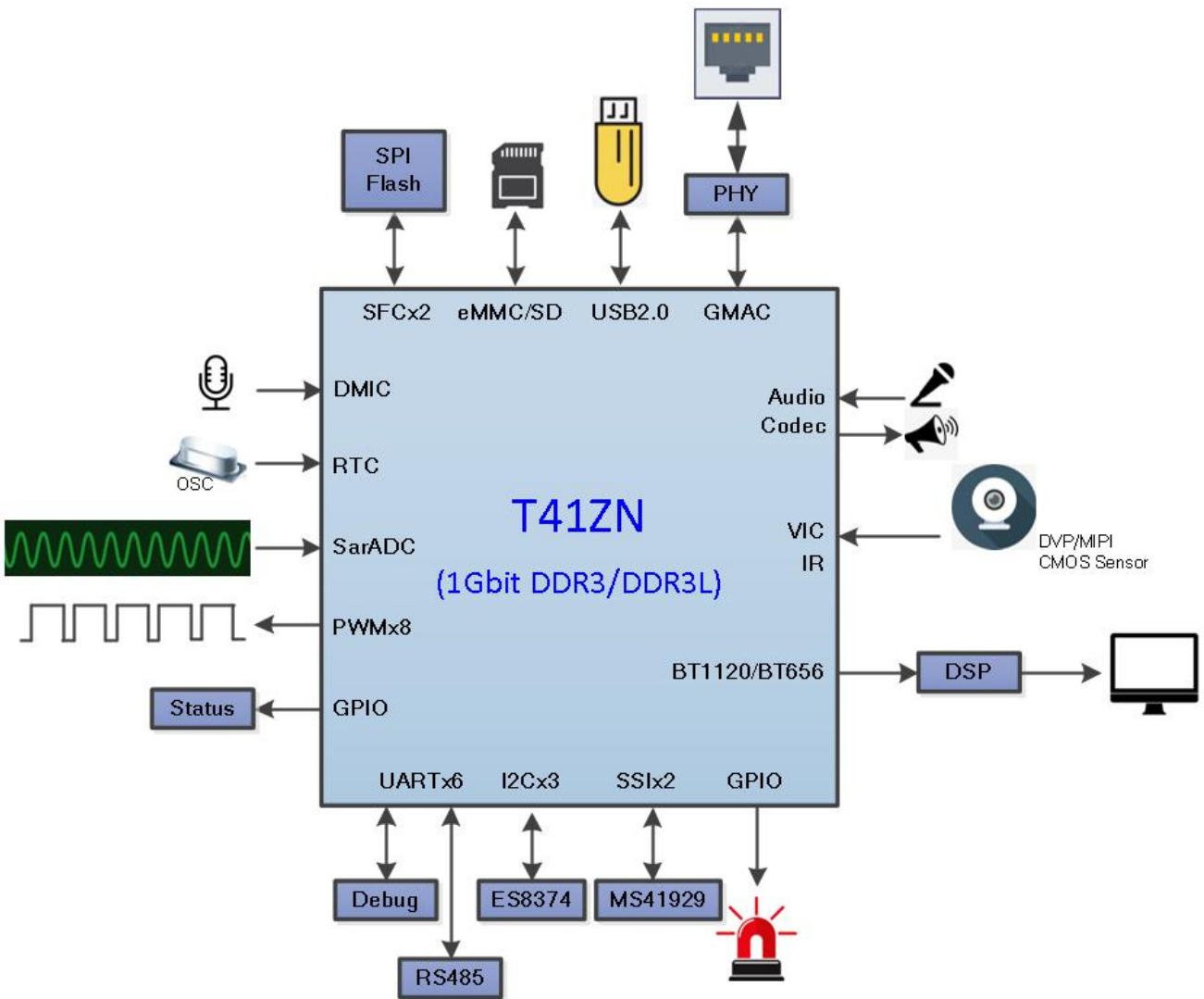
For more quickly and easily to use T41ZN, 1 Gbit DDR3/DDR3L KGD is integrated on chip.

On-chip modules such as audio CODEC, multi-channel SAR_ADC, low power DMIC and camera interface offer designers a economical suite of peripherals for video application. WLAN, Bluetooth and expansion options are supported through high-speed SPI and eMMC/SD/SDIO host controllers. Other peripherals such as USB OTG, MAC, UART and SPI as well as general system resources provide enough computing and connectivity capability for many applications.

1.2 Application Scenarios

Figure 1-2 shows the typical application scenario of the T41ZN.

Figure1- 2 The typical application scenario of the T41ZN



2 Features

2.1 CPU

- X Burst[®]2 frequency range is 1.0GHz ~1.4GHz, Dual Core, Dual-issue, high performance and low power implementation of IPS32 ISA R5
- MIPS32 ISA R5 plus Ingenic SIMD512 ISA
- Dual-issue, superscalar, super pipeline with Simultaneous Multi-Threading(SMT)
- 32K L1 D-cache + 32K L1 I-cache, 128KByte L2 cache
- High-performance Floating-point Unit and SIMD Engine: FSE
- Programmable Memory Management Unit(MMU)

2.2 MCU

- 700MHz RISC-V coprocessor
- RV32IM instruction set

2.3 AI Engine

- 1.2Tops@int8, 4.8Tops@int4
- Support int16/int8/int4/int2 bit width
- Magik AI algorithm develop platform available

2.4 AI Pre/Post-Processing(AIP)

- Color conversion, Resize
- Hardware matrix operations

2.5 Video Processor Unit

- Support profiles AVC/HEVC/JPEG encoding
- 8 bit pixel depth support
- Hevc & AVC supports I/P frames
- Maximum size up to 3840x4096
- Maximum frame rate to 3840x2160@20 fps
- Support CBR/VBR/SVBR control, 8 ROIs

2.6 Image Signal Processor

- Support max 12bit bayer data input, YUV422 8bit input
- Support max in/out image size 3840x2160
- Support min input size 512x256
- Support min output size 128x128

- Support maximum performance 3840x2160@20fps
- Support black level correction
- Support lens shading correction
- Support defect pixel correction
- Support noise reduction in raw domain
- Support 2f-wdr mode
- Support 3A & statistical information output
- Support demosaic processing
- Support purple edge correction
- Support automatic defog
- Support local contrast enhancement
- Support time domain / space domain denoising
- Support sharpen
- Support lens distortion correction in the horizontal direction
- Support image scaler, clip, flip and mirror
- Support 3 different resolution outputs at the same time
- Support IR removal & IR data output

2.7 2D Graphics Engine

- IPU
 - Input data format: NV12
 - Output data format: ARGB/RGB/NV12/NV21/HSV
 - Support 4 layers OSD
- LDC
 - Support lens distortion correction in the horizontal and vertical direction
 - Input and output format is NV12,NV21.
 - Minimum input image size (pixel): 640x480
 - Maximum input image size (pixel): 3840x2160
 - Support crop mode
- Drawbox
 - Support for drawing four types of bounding boxes

2.8 Display Process Controller

- Support input format: RGB888, RGB565, RGB555, NV12, NV21
- Support maximum input and output resolution 800x800

- Support display output 800x600@60Hz,24BPP
- SLCD(Smart LCD) interface supports MIPI_DBI protocol 6800 (type A) and 8080 (type B)
- Support up to 16,777,216(16M) colors

2.9 Video Input

- Input interface: MIPI/DVP/BT656/BT1120 (serial)
- Input format: RAW8/RAW10/RAW12/YUV422 (8bit)
- Support WDR/DOL Sensor input

2.10 Video Output

- Output interface: BT656/BT1120 (serial)
- Support progressive scan only, do not support interlaced scan

2.11 Audio System

- DMIC
 - SNR: 90dB, THD: -90dB @ FS -20dB
 - Support 1/2/3/4 channel digital MIC
 - Support 8K, 16K, or 48K sampling frequency
- Audio Codec
 - 24 bits DAC with 92dB SNR.
 - 24 bits ADC with 90dB SNR.
 - Programmable input and output analog gains
 - Digital interpolation and decimation filter integrated
 - Sampling rate of 8KHz, 12KHz, 16KHz, 24KHz, 32KHz, 44.1KHz, 48KHz and 96KHz
 - Support I2S and MSB-Justified format
 - Support inner codec and external codec connect
 - Support master/slave mode when connect the external codec, but only support slave mode when connect the inner codec
 - Support 4-line/6-line mode when connect the external codec.

2.12 Memory

- SDRAM
 - SIP IN 1Gbit DDR3/DDR3L

2.13 System Functions

- Clock
 - On-Chip 24MHz oscillator circuit

- Three phase-locked loops(PLLs) which can be programmed through configuring registers
- Functional-unit clock gating
- PWM
- Provide 8 separate channels,each channel can work independently
- Support 2 update configuration modes:Register mode and DMA mode
- TCU
- 8 channels in TCU and support following operating modes
- Interrupt controller
- Total 64 interrupt sources
- Each interrupt source can be independently enabled
- Priority mechanism to indicate highest priority interrupt
- Another set of source, mask and pending registers to serve for PDMA
- Watchdog timer
- Generates WDT reset
- PDMA
- Support up to 32 independent DMA channels
- Descriptor or No-Descriptor Transfer mode compatible with previous JZ SoC
- Peripherals related to data transmission
- SFC
- SPI protocol support: Standard, Dual, Quad SPI
- Configurable sampling point for reception
- Configurable flash address wide are supported
- 7 transfer formats: Standard SPI, Dual-Output/Dual-Input SPI, Quad-Output/Quad-Input SPI, Dual-I/O SPI, Quad-I/O SPI, Full Dual-I/O SPI, Full Quad-I/O SPI
- Two data transfer mode: slave mode and DMA mode
- SDR trans mode.
- EFUSE
- 2048bits internal nonvolatile one-time programmable EFUSE storage
- 640 bits reserved for users
- Segmented management with protection bits
- Embedded 4 redundancy bits can be used to repair 4bits of damaged bit
- Configurable programming timing

2.14 Peripherals

- General-Purpose I/O ports
 - Each port can be configured as an input, an output or an alternate function port
 - Each port can be configured as an interrupt source of low/high level of rising/falling edge triggering, and every interrupt source can be masked independently
 - Each port has an internal pull-up and pull-down resistor connected. The pull-up/down resistor can be disabled
- SMB Controller
 - Two-wire SMB serial interface – consists of a serial data line (SDA) and a serial clock line (SCL)
 - Two speeds: Standard mode (100 Kb/s); Fast mode (400 Kb/s)
- SSI
 - 3 protocols support: National’s Microwire, TI’s SSP, and Motorola’s SPI
 - Programmable bit clock frequency between 7.2KHz to 50MHz
- SSI-SLV
 - Only one protocols support: Motorola's SPI
 - Serial bit clock support up to 50MHz
- UART
 - Support Full-duplex transfer
 - Programmable width for data bit and stop bit
 - Support parity check or no parity
 - Support Serial Infrared interface, which confirms to IrDA specification
- MSC Controller
 - Support SD 4.1 memory and SD Input/Output (SDIO) 2.0 digital interface protocol, and compliant with SD HCI specification
 - Support EMMC 5.1 Command Queuing Engine (CQE), compliant with CQ HCI specification
- OTG Interface
 - Complies with the USB 2.0 standard for high-speed (480 Mbps) functions and with the On-The-Go supplement to the USB 2.0 specification
- SAR A/D Interface
 - 12 bit resolution
 - Up to 2MS/s sampling rate
 - DNL<1LSB, INL<2LSB

2.15 Boot

- Boot Option
 - SPI Nor/Nand Flash, SD Card, USB, Uart
- Security Boot
- Fast Boot(200ms)

2.16 Security Engine

- AES, DES , RSA and HASH algorithms implemented by hardware
- Digital True Random Number Generate

2.17 RTC with an independent Power Supply

- Powered by independent power supply,can work in hibernating mode
- Power down control
- Alarm wake up
- External pin wake up with up to 2 seconds glitch filtering

2.18 Physical Specifications

- Power
 - TBD

3 Characteristic

Item	Characteristic
Power supply voltage	General purpose I/O: 1.5~3.3V DDR I/O: 1.5V(DDR3) \pm 0.75V 1.35V(DDR3L)-0.067V/+0.1V EFUSE programming: 1.8V \pm 5% Analog power supply 1: 1.8V \pm 0.1V Analog power supply 2: 3.3V \pm 0.1V Core: 0.8V \pm 0.1V
Package	BGA232, 11mm X 11mm , 0.65pitch
Operating frequency	1.0GHz~1.4GHz

4 Package and Pinout

4.1 Overview

T41ZN processor is offered in BGA232, shown in Figure4-1~Figure4-4. The detailed pin description is listed in Table5-1~Table5-15.

4.2 Solder Process

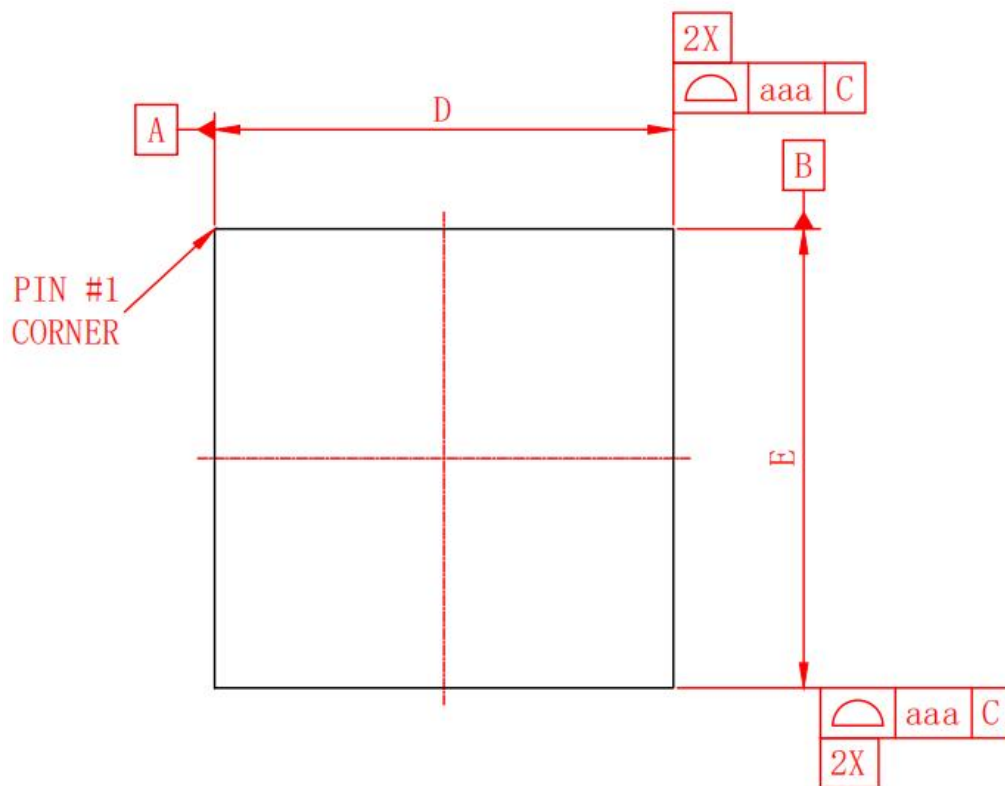
T41ZN package is lead-free. It's reflow profile follows the IPC/JEDEC lead-free reflow profile as contained in J-STD-020C.

4.3 Moisture Sensitivity Level

T41ZN package moisture sensitivity is level 3.

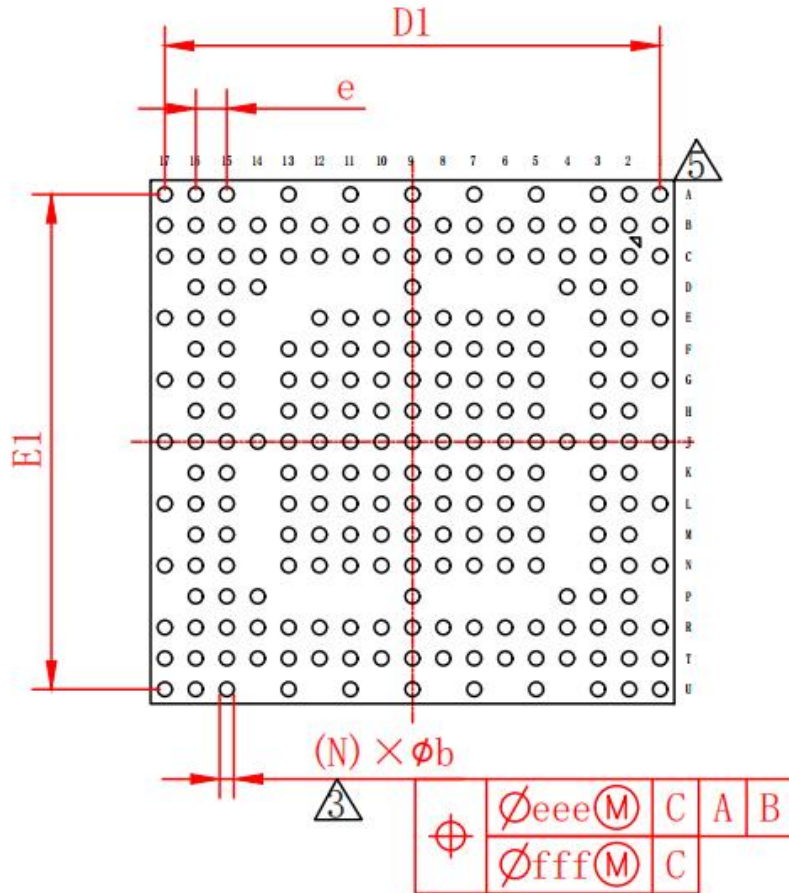
4.4 T41ZN Package

Figure4-1 Top View



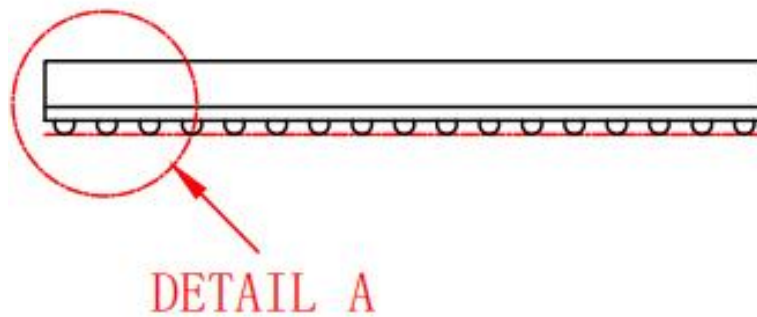
Top View

Figure4-2 Bottom View

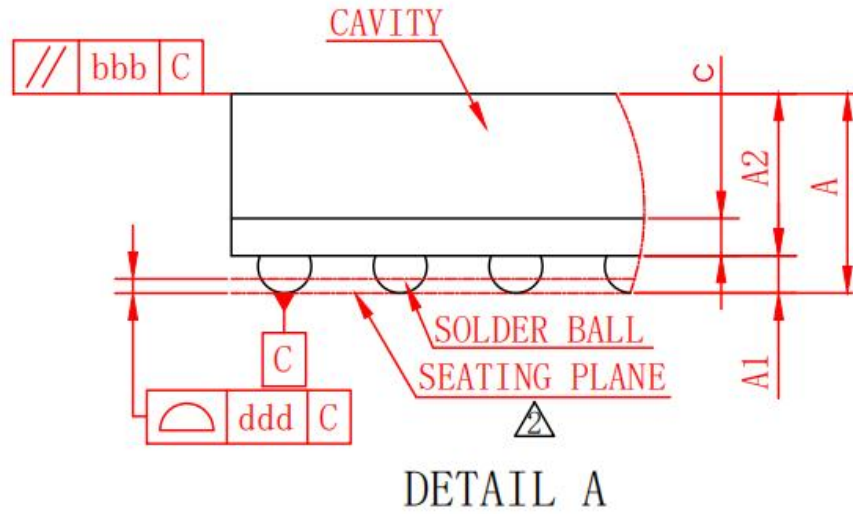


Bottom View

Figure4-3 Side View



Side View

Figure4-4 Enlarged view of detail "A"

Table4-1 Package dimensions

symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.230	---	---	0.048
A1	0.160	0.210	0.260	0.006	0.008	0.010
A2	0.870	0.920	0.970	0.034	0.036	0.038
c	0.190	0.220	0.250	0.007	0.009	0.010
D	10.900	11.000	11.100	0.429	0.433	0.437
E	10.900	11.000	11.100	0.429	0.433	0.437
D1	---	10.400	---	---	0.409	---
E1	---	10.400	---	---	0.409	---
e	---	0.650	---	---	0.026	---
b	0.250	0.300	0.350	0.010	0.012	0.014
aaa	0.100			0.004		
bbb	0.100			0.004		
ddd	0.080			0.003		
eee	0.150			0.006		
fff	0.080			0.003		
Ball Diam	0.300			0.012		
N	232			232		
MD/ME	17/17			17/17		

**NOTE**

TECHNOLOGY SPECIFICATION

1. BALL PAD OPENING: 0.270mm;

△ PRIMARY DATUM C AND SEATING PLANE ARE THE SOLDER BALLS;

△ DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C;

4. SPECIAL CHARACTERISTICS C CLASS: bbb, ddd;

△ THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY;

6. BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES;

5 Pin Description

5.1 Static Memory/DVP/SMB/SSI/DMIC

Table5-1 Static Memory/DVP/SMB/SSI/DMIC Pins(14)

Pin Names	IO	Loc	IO Char.	Pin Description	Power
SD0 DVP_D6 SSI0_CLK PA06	IO I O IO	H2	Hi-Z-rst	SD0: Static memory data bus bit 0 DVP_D6_I: DVP data in bit 6 SSI0_CLK_O: SSI 0 clock PA06: GPIO group A bit 06	VDDIO18
SD1 DVP_D7 SSI0_CE0 PA07	IO I O IO	H3	Hi-Z-rst	SD1: Static memory data bus bit 1 DVP_D7_I: DVP data in bit 7 SSI0_CE0_O:SSI 0 chip 0 select PA07: GPIO group A bit 07	VDDIO18
SD2 DVP_D8 SSI0_DT PA08	IO I O IO	G1	Hi-Z-rst	SD2: Static memory data bus bit 2 DVP_D8_I: DVP data in bit 8 SSI0_DT_O: normal speed ssi 0 transmit data PA08: GPIO group A bit 08	VDDIO18
SD3 DVP_D9 SSI0_DR PA09	IO I IO IO	G2	Hi-Z-rst	SD3: Static memory data bus bit 3 DVP_D9_I: DVP data in bit 9 SSI0_DR_O:normal speed ssi 0 receive data PA09: GPIO group A bit 09	VDDIO18
SD4 DVP_D10 SSI0_GPC PA10	IO I O IO	G3	Hi-Z-rst	SD4: Static memory data bus bit 4 DVP_D10_I: DVP data in bit 10 SSI0_GPC_O: SSI 0 general-purpose control PA10: GPIO group A bit 10	VDDIO18
SD5 DVP_D11 SSI0_CE1 PA11	IO I O IO	F2	Hi-Z-rst	SD5: Static memory data bus bit 5 DVP_D11_I: DVP data in bit 11 SSI0_CE1_O: SSI 0 chip 1 select PA11: GPIO group A bit 11	VDDIO18
SD6 SMB0_SDA PA12	IO IO IO	J1	Hi-Z-rst	SD6: Static memory data bus bit 6 SMB0_SDA: I2C 0 serial data PA12: GPIO group A bit 12	VDDIO18
SD7 SMB0_SCK PA13	IO IO IO	J4	Hi-Z-rst	SD7: Static memory data bus bit 7 SMB0_SCK:I2C 0 serial clock PA13: GPIO group A bit 13	VDDIO18

Pin Names	IO	Loc	IO Char.	Pin Description	Power
SA0 DVP_PCLK DMIC_CLK PA14	O I O IO	F3	Hi-Z-rst	SA0_O: Static memory address bus bit 0 DVP_PCLK_I: camera sensor pixel clock input for DVP model DMIC_CLK_O: Digital microphone Clock output PA14: GPIO group A bit 14	VDDIO18
SA1 DVP_MCLK PA15	O O IO	E1	Hi-Z-rst	SA1_O: Static memory address bus bit 1 DVP_MCLK_O: DVP main clock output PA15: GPIO group A bit 15	VDDIO18
CS2 DVP_HSYNC DMIC_DAT0 PA16	O I I IO	J2	Hi-Z-rst	CS2_O: Static memory chip 2 select DVP_HSYNC: DVP horizontal sync DMIC_DAT0: Digital microphone data bit 0 PA16: GPIO group A bit 16	VDDIO18
RD DVP_VSYNC DMIC_DAT1 PA17	O I I IO	J3	Hi-Z-rst	RD_O: Static memory read signal DVP_VSYNC: DVP vertical sync DMIC_DAT1: Digital microphone data bit 1 PA17: GPIO group A bit 17	VDDIO18
SA2 PA18	O IO	E3	Hi-Z-rst	SA2_O: Static memory address bus bit 2 PA18: GPIO group A bit 18	VDDIO18
WAIT PA19	I IO	E2	Hi-Z-rst	WAIT_I: Static memory/device wait signal PA19: GPIO group A bit 19	VDDIO18

5.2 SFC

Table5-2 SFC Pins(12)

Pin Names	IO	Loc	IO Char.	Pin Description	Power
SSI1_DT SFC1_DT_IO0 PA20	O IO IO	R8	Hi-Z-rst	SSI1_DT: SSI 1 transmit data SFC1_DT_IO0: Serial Flash data PA20: GPIO group A bit 20	VDDIO1
SSI1_DR SFC1_DR_IO1 PA21	I IO IO	T7	Hi-Z-rst	SSI1_DR: SSI 1 receive data SFC1_DR_IO1: Serial Flash data PA21: GPIO group A bit 21	VDDIO1
SSI1_CLK SFC1_CLK PA22	O O IO	T8	Hi-Z-rst	SSI1_CLK: SSI 1 clock SFC1_CLK: Serial Flash clock output PA22: GPIO group A bit 22	VDDIO1
SFC0_DT_IO0 PA23	IO IO	U5	Hi-Z-rst	SFC0_DT_IO0: Serial Flash data PA23: GPIO group A bit 23	VDDIO1
SFC0_DR_IO1 PA24	IO IO	R5	Hi-Z-rst	SFC0_DR_IO1: Serial Flash data PA24: GPIO group A bit 24	VDDIO1

Pin Names	IO	Loc	IO Char.	Pin Description	Power
SFC0_HOLD_IO3 PA25	IO IO	T6	Hi-Z-rst	SFC0_HOLD_IO3: Serial Flash hold signal PA25: GPIO group A bit 25	VDDIO1
SFC0_WP_IO2 PA26	IO IO	T5	Hi-Z-rst	SFC0_WP_IO2: Serial Flash write protect signal PA26: GPIO group A bit 26	VDDIO1
SFC0_CLK PA27	O IO	R6	Hi-Z-rst	SFC0_CLK: Serial Flash clock output PA27: GPIO group A bit 27	VDDIO1
SFC0_CE PA28	O IO	T4	Hi-Z-rst	SFC0_CE: Serial Flash chip enable PA28: GPIO group A bit 28	VDDIO1
SSI1_CE0 SFC1_CE PA29	O O IO	R7	Hi-Z-rst	SSI1_CE0:SSI 1 chip 0 select SFC1_CE:Serial Flash chip enable PA29:GPIO group A bit 29	VDDIO1
SSI1_CE1 SFC1_WP_IO2 PA30	O IO IO	U7	Hi-Z-rst	SSI1_CE1:SSI 1 chip 1 select SFC1_WP_IO2:Serial Flash write protect signal PA30:GPIO group A bit 30	VDDIO1
SSI1_GPC SFC1_HOLD_IO3 PA31	O IO IO	R9	Hi-Z-rst	SSI1_GPC:SSI 1 general-purpose control SFC1_HOLD_IO3:Serial Flash hold signal PA31:GPIO group A bit 31	VDDIO1

5.3 MSCx/PWMx/UARTx/SMBx/SSI1/I2S/GMAC

Table5-3 MSCx/PWMx/UARTx/SMBx/SSI1/I2S/GMAC Pins (31)

Pin Names	IO	Loc	IO Char.	Pin Description	Power
MSC0_D0 PB00	IO IO	H16	Hi-Z-rst	MSC0_D0:MSC (MMC/SD) 0 data bit 0 PB00:GPIO group B bit 00	VDDIO1
MSC0_D1 PB01	IO IO	J15	Hi-Z-rst	MSC0_D1:MSC (MMC/SD) 0 data bit 1 PB01:GPIO group B bit 01	VDDIO1
MSC0_D2 PB02	IO IO	G15	Hi-Z-rst	MSC0_D2:MSC (MMC/SD) 0 data bit 2 PB02:GPIO group B bit 02	VDDIO1
MSC0_D3 PB03	IO IO	G16	Hi-Z-rst	MSC0_D3:MSC (MMC/SD) 0 data bit 3 PB03:GPIO group B bit 03	VDDIO1
MSC0_CLK PB04	O IO	H15	Hi-Z-rst	MSC0_CLK_O:MSC (MMC/SD) 0 clock output PB04:GPIO group B bit 04	VDDIO1
MSC0_CMD PB05	IO IO	G17	Hi-Z-rst	MSC0_CMD:MSC (MMC/SD) 0 command PB05:GPIO group B bit 05	VDDIO1
GMAC_TXCLK UART5_TXD PB06	I O IO	T12	Hi-Z-rst	GMAC_TXCLK_I:gmac transmitting clock UART5_TXD_O:UART 5 transmit data PB06:GPIO group B bit 06	VDDIO1

Pin Names	IO	Loc	IO Char.	Pin Description	Power
GMAC_PHY_CLK UART5_RXD PB07	O I IO	T9	Hi-Z-rst	GMAC_PHY_CLK_O:gmac phy clock UART5_RXD_I:UART 5 receive data PB07:GPIO group B bit 07	VDDIO1
GMAC_TXEN I2S_DAC_BCLK PWM2 PB08	O IO IO IO	U11	Hi-Z-rst	GMAC_TXEN_O:gmac transmitting enable I2S_DAC_BCLK:I2S DAC clock PWM2:PWM channel 2 output PB08:GPIO group B bit 08	VDDIO1
GMAC_RXDV I2S_DAC_LRCK PWM3 PB09	I IO IO IO	U9	Hi-Z-rst	GMAC_RXDV_I:gmac receive data valid I2S_DAC_LRCK:I2S DAC left/right clock PWM3:PWM channel 3 output PB09:GPIO group B bit 09	VDDIO1
GMAC_MDCK I2S_ADC_MCLK SMB2_SDA PB10	O O IO IO	R10	Hi-Z-rst	GMAC_MDCK_O:gmac manage data clock I2S_ADC_MCLK_O:I2S ADC clock SMB2_SDA:I2C 2 serial data PB10:GPIO group B bit 10	VDDIO1
GMAC_MDIO I2S_DAC_MCLK SMB2_SCK PB11	IO O IO IO	T10	Hi-Z-rst	GMAC_MDIO:gmac MDIO which is clocked by MDC I2S_DAC_MCLK_O:I2S DAC clock SMB2_SCK:I2C 2 serial clock PB11:GPIO group B bit 11	VDDIO1
GMAC_TXD0 I2S_ADC_BCLK PWM4 PB13	O IO IO IO	R11	Hi-Z-rst	GMAC_TXD0_O:gmac transmit data bit 0 I2S_ADC_BCLK: I2S ADC bit clock PWM4:PWM channel 4 output PB13:GPIO group B bit 13	VDDIO1
GMAC_TXD1 I2S_ADC_LRCK PWM5 PB14	O IO IO IO	T11	Hi-Z-rst	GMAC_TXD1_O:gmac transmit data bit 1 I2S_ADC_LRCK:I2S ADC left/right clock PWM5:PWM channel 5 output PB14:GPIO group B bit 14	VDDIO1
GMAC_RXD0 I2S_SDTI PWM6 PB15	I I IO IO	U13	Hi-Z-rst	GMAC_RXD0_I:gmac receive data bit 0 I2S_SDTI_I:I2S serial data input signal PWM6:PWM channel 6 output PB15:GPIO group B bit 15	VDDIO1
GMAC_RXD1 I2S_SDTO PWM7 PB16	I O IO IO	R12	Hi-Z-rst	GMAC_RXD1_I:gmac receive data bit 1 I2S_SDTO_O:I2S serial data output signal PWM7:PWM channel 7 output PB16:GPIO group B bit 16	VDDIO1

Pin Names	IO	Loc	IO Char.	Pin Description	Power
PWM0 MSC1_CLK PB17	IO O IO	E16	Hi-Z-rst	PWM0:PWM channel 0 output MSC1_CLK_O:MSC (MMC/SD) 1 clock output PB17:GPIO group B bit 17	VDDIO1
PWM1 MSC1_CMD PB18	IO IO IO	E17	Hi-Z-rst	PWM1:PWM channel 1 output MSC1_CMD:MSC (MMC/SD) 1 command PB18:GPIO group B bit 18	VDDIO1
UART0_RXD MSC1_D0 PB19	I IO IO	D16	Hi-Z-rst	UART0_RXD_I:UART 0 receive data MSC1_D0:MSC (MMC/SD) 1 data bit 0 PB19:GPIO group B bit 19	VDDIO1
UART0_CTS MSC1_D1 TCK_ PB20	I IO I IO	E15	Hi-Z-rst	UART0_CTS_I:UART 0 clear-to-send MSC1_D1:MSC (MMC/SD) 1 data bit 1 TCK_I:JTAG clock input PB20:GPIO group B bit 20	VDDIO1
UART0_RTS MSC1_D2 TMS_ PB21	O IO I IO	C17	Hi-Z-rst	UART0_RTS_O:UART 0 request-to-send MSC1_D2:MSC (MMC/SD) 1 data bit 2 TMS_I:JTAG mode select PB21:GPIO group B bit 21	VDDIO1
UART0_TXD MSC1_D3 PB22	O IO IO	D15	Hi-Z-rst	UART0_TXD_O:UART 0 transmit data MSC1_D3:MSC (MMC/SD) 1 data bit 3 PB22:GPIO group B bit 22	VDDIO1
UART1_TXD TDO_ PB23	O O IO	F15	Hi-Z-rst	UART1_TXD_O:UART 1 transmit data TDO_O:JTAG data output PB23:GPIO group B bit 23	VDDIO1
UART1_RXD TDI_ PB24	I I IO	F16	Hi-Z-rst	UART1_RXD_I:UART 1 receive data TDI_I:JTAG data input PB24:GPIO group B bit 24	VDDIO1
SMB1_SDA UART3_TXD SSI1_CE1 PB25	IO O O IO	C11	Hi-Z-rst	SMB1_SDA:I2C 1 serial data UART3_TXD_O:UART 3 transmit data SSI1_CE1_O:SSI 1 chip 1 select PB25:GPIO group B bit 25	VDDIO1
SMB1_SCK UART3_RXD SSI1_GPC PB26	IO I O IO	C10	Hi-Z-rst	SMB1_SCK:I2C 1 serial clock UART3_RXD_I:UART 3 receive data SSI1_GPC_O:SSI 1 general-purpose control PB26:GPIO group B bit 26	VDDIO1
DRV_VBUS SMB2_SDA SSI1_DT PB27	O IO O IO	B11	Hi-Z-rst	DRV_VBUS_O:USB-5V control SMB2_SDA:I2C 2 serial data SSI1_DT_O:SSI 1 transmit data PB27:GPIO group B bit 27	VDDIO1

Pin Names	IO	Loc	IO Char.	Pin Description	Power
DMIC_CLK	O			DMIC_CLK_O:Digital microphone Clock output	
SMB2_SCK	O	A11	Hi-Z-rst	SMB2_SCK:I2C 2 serial clock	VDDIO1
SSI1_CLK	IO			SSI1_CLK_O:SSI 1 clock	
PB28				PB28:GPIO group B bit 28	
DMIC_DAT0	I			DMIC_DAT0_I:Digital microphone data bit 0	
UART4_TXD	O	B12	Hi-Z-rst	UART4_TXD_O:UART 4 transmit data	VDDIO1
SSI1_DR	I			SSI1_DR_I:SSI 1 receive data	
PB29	IO			PB29:GPIO group B bit 29	
DMIC_DAT1	I			DMIC_DAT1_I:Digital microphone data bit 1	
UART4_RXD	I	C12	Hi-Z-rst	UART4_RXD_I:UART 4 receive data	VDDIO1
SSI1_CE0	O			SSI1_CE0_O:SSI 1 chip 0 select	
PB30	IO			PB30:GPIO group B bit 30	
PB31	IO	B10	Hi-Z-rst	PB31:GPIO group B bit 31	VDDIO1

5.4 UARTx/PWMx/SMBx/SSI0/SSI_SLV/I2S

Table5-4 UARTx/ PWMx/SMBx/SSI0/SSI_SLV/I2S(18)

Pin Names	IO	Loc	IO Char.	Pin Description	Power
MSC1_CLK	O			MSC1_CLK_O:MSC (MMC/SD) 1 clock output	
SSI0_CLK	O	A1	Hi-Z-rst	SSI0_CLK_O:SSI 0 clock	VDDIO2
PC02	IO			PC02:GPIO group C bit 02	
MSC1_CMD	IO			MSC1_CMD:MSC (MMC/SD) 1 command	
SSI0_CE0	O	C3	Hi-Z-rst	SSI0_CE0_O:SSI 0 chip 0 select	VDDIO2
PC03	IO			PC03:GPIO group C bit 03	
MSC1_D0	IO			MSC1_D0:MSC (MMC/SD) 1 data bit 0	
SSI0_DT	O	B2	Hi-Z-rst	SSI0_DT_O:SSI 0 transmit data	VDDIO2
PC04	IO			PC04:GPIO group C bit 04	
MSC1_D1	IO			MSC1_D1:MSC (MMC/SD) 1 data bit 1	
SSI0_DR	I	A2	Hi-Z-rst	SSI0_DR_I:SSI 0 receive data	VDDIO2
PC05	IO			PC05:GPIO group C bit 05	
MSC1_D2	IO			MSC1_D2:MSC (MMC/SD) 1 data bit 2	
SSI0_GPC	O	C2	Hi-Z-rst	SSI0_GPC_O:SSI 0 general-purpose control	VDDIO2
PC06	IO			PC06:GPIO group C bit 06	
MSC1_D3	IO			MSC1_D3:MSC (MMC/SD) 1 data bit 3	
SSI0_CE1	O	B1	Hi-Z-rst	SSI0_CE1_O:SSI 0 chip 1 select	VDDIO2
PC07	IO			PC07:GPIO group C bit 07	

Pin Names	IO	Loc	IO Char.	Pin Description	Power
UART0_TXD SMB2_SDA PC08	O IO IO	B6	Hi-Z-rst	UART0_TXD_O:UART 0 transmit data SMB2_SDA:I2C 2 serial data PC08:GPIO group C bit 08	VDDIO2
UART0_RXD SMB2_SCK PC09	I IO IO	C6	Hi-Z-rst	UART0_RXD_I:UART 0 receive data SMB2_SCK:I2C 2 serial clock PC09:GPIO group C bit 09	VDDIO2
UART0_CTS I2S_DAC_MCLK PC11	I O IO	C5	Hi-Z-rst	UART0_CTS_I:UART 0 Clear-to-Send I2S_DAC_MCLK_O:I2S DAC clock output PC11:GPIO group C bit 11	VDDIO2
UART0_RTS I2S_ADC_MCLK PC12	O O IO	A5	Hi-Z-rst	UART0_RTS_O:UART 0 Request-to-Send I2S_ADC_MCLK_O:I2S ADC clock output PC12:GPIO group C bit 12	VDDIO2
UART2_TXD I2S_ADC_BCLK PC13	O IO IO	B7	Hi-Z-rst	UART2_TXD_O:UART 2 transmit data I2S_ADC_BCLK:I2S ADC bit clock PC13:GPIO group C bit 13	VDDIO2
UART2_RXD I2S_ADC_LRCK PC14	I IO IO	C7	Hi-Z-rst	UART2_RXD_I:UART 2 receive data I2S_ADC_LRCK:I2S ADC left/right clock PC14:GPIO group C bit 14	VDDIO2
SSI_SLV_CLK I2S_DAC_BCLK PWM0 EXCLK PC15	I IO IO O IO	B4	Hi-Z-rst	SSI_SLV_CLK_I:SSI slave clock I2S_DAC_BCLK:I2S DAC bit clock PWM0:PWM channel 0 output EXCLK_O:external clock input PC15:GPIO group C bit 15	VDDIO2
SSI_SLV_CE0 I2S_DAC_LRCK PWM1 RTC32K PC16	I IO IO O IO	A3	Hi-Z-rst	SSI_SLV_CE0_I:SSI slave chip 0 select I2S_DAC_LRCK:I2S DAC left/right clock PWM1:PWM channel 1 output RTC32K_O: PC16:GPIO group C bit 16	VDDIO2
SSI_SLV_DT I2S_SDTO PWM2 PC17	IO O IO IO	B3	Hi-Z-rst	SSI_SLV_DT:SSI slave transmit data I2S_SDTO_O:I2S serial data output signal PWM2:PWM channel 2 output PC17:GPIO group C bit 17	VDDIO2
SSI_SLV_DR I2S_SDTI PWM3 PC18	IO I IO IO	B5	Hi-Z-rst	SSI_SLV_DR:SSI slave receive data I2S_SDTI_I:I2S serial data input signal PWM3:PWM channel 3 output PC18:GPIO group C bit 18	VDDIO2
UART2_CTS SMB1_SDA PC19	I IO IO	A7	Hi-Z-rst	UART2_CTS_I:UART 2 clear-to-send SMB1_SDA:I2C 1 serial data PC19:GPIO group C bit 19	VDDIO2

Pin Names	IO	Loc	IO Char.	Pin Description	Power
UART2_RTS	O			UART2_RTS_O:UART 2 Request-to-Send	VDDIO2
SMB1_SCK	IO	C8	Hi-Z-rst	SMB1_SCK:I2C 1 serial clock	
PC20	IO			PC20:GPIO group C bit 20	

5.5 SLCD/PWMx/BT656/UARTx

Table5-5 SLCD/PWMx/BT656/UARTx Pins(13)

Pin Names	IO	Loc	IO Char.	Pin Description	Power
SLCD_D0	O	A15	Hi-Z-rst	SLCD_D0_O:smart lcd data output bit 0	VDDIO1
BT656_D0	O			BT656_D0_O:BT656 data bit 0	
UART3_TXD	O			UART3_TXD_O:UART 3 transmit data	
PD00	IO			PD00:GPIO group D bit 00	
SLCD_D1	O	B15	Hi-Z-rst	SLCD_D1_O:smart lcd data output bit 1	VDDIO1
BT656_D1	O			BT656_D1_O:BT656 data bit 1	
UART3_RXD	I			UART3_RXD_I:UART 3 receive data	
PD01	IO			PD01:GPIO group D bit 01	
SLCD_D2	O	A16	Hi-Z-rst	SLCD_D2_O:smart lcd data output bit 2	VDDIO1
BT656_D2	O			BT656_D2_O:BT656 data bit 2	
UART4_TXD	O			UART4_TXD_O:UART 4 transmit data	
PD02	IO			PD02:GPIO group D bit 02	
SLCD_D3	O	C15	Hi-Z-rst	SLCD_D3_O:smart lcd data output bit 3	VDDIO1
BT656_D3	O			BT656_D3_O:BT656 data bit 3	
UART4_RXD	I			UART4_RXD_I:UART 4 receive data	
PD03	IO			PD03:GPIO group D bit 03	
SLCD_D4	O	A17	Hi-Z-rst	SLCD_D4_O:smart lcd data output bit 4	VDDIO1
BT656_D4	O			BT656_D4_O:BT656 data bit 4	
UART5_TXD	O			UART5_TXD_O:UART 5 transmit data	
PD04	IO			PD04:GPIO group D bit 04	
SLCD_D5	O	B16	Hi-Z-rst	SLCD_D5_O:smart lcd data output bit 5	VDDIO1
BT656_D5	O			BT656_D5_O:BT656 data bit 5	
UART5_RXD	I			UART5_RXD_I:UART 5 receive data	
PD05	IO			PD05:GPIO group D bit 05	
SLCD_D6	O	B17	Hi-Z-rst	SLCD_D6_O:smart lcd data output bit 6	VDDIO1
BT656_D6	O			BT656_D6_O:BT656 data bit 6	
SMB1_SDA	IO			SMB1_SDA:I2C 1 serial data	
PD06	IO			PD06:GPIO group D bit 06	

Pin Names	IO	Loc	IO Char.	Pin Description	Power
SLCD_D7 BT656_D7 SMB1_SCK PD07	O O IO IO	C16	Hi-Z-rst	SLCD_D7_O:smart lcd data output bit 7 BT656_D7_O:BT656 data bit 7 SMB1_SCK:I2C 1 serial clock PD07:GPIO group D bit 07	VDDIO1
SLCD_WR BT656_PCLK PD08	O O IO	B14	Hi-Z-rst	SLCD_WR_O:smart lcd write data control BT656_PCLK_O:BT65 pixel clock PD08:GPIO group D bit 08	VDDIO1
SLCD_TE UART2_CTS PWM4 PD09	I I IO IO	A13	Hi-Z-rst	SLCD_TE_I:smart lcd tearing effect UART2_CTS_I:UART2 clear-to-send handshaking PWM4:PWM channel 4 output PD09:GPIO group D bit 09	VDDIO1
SLCD_CS UART2_RTS PWM5 PD10	O O IO IO	B13	Hi-Z-rst	SLCD_CS_O:smart lcd chip select UART2_RTS_O:UART2 request-to-send handshaking PWM5:PWM channel 5 output PD10:GPIO group D bit 10	VDDIO1
SLCD_DC UART2_TXD PWM6 PD11	O O IO IO	C13	Hi-Z-rst	SLCD_DC_O:smart lcd cmd/data identify UART2_TXD_O:UART 2 data transmit PWM6:PWM channel 6 output PD11:GPIO group D bit 11	VDDIO1
SLCD_RDY UART2_RXD PWM7 PD12	I I IO IO	C14	Hi-Z-rst	SLCD_RDY_I:smart lcd work status UART2_RXD_I:UART 2 receive data PWM7:PWM channel 7 output PD12:GPIO group D bit 12	VDDIO1

5.6 System Boot Select

Table5-6 Boot Select Pins(2)

Pin Names	IO	Loc	IO Char.	Pin Description	Power
(BOOT_SEL0) PC00	I IO	A9	PU_rst	PC00:GPIO group C bit 00	VDDIO1
(BOOT_SEL1) PC01	I IO	B9	PD_rst	PC01:GPIO group C bit 01	VDDIO1

5.7 System Control

Table5-7 System Control Pins(7)

Pin Names	IO	Loc	IO Char.	Pin Description	Power
TRST	I	D14	PD_rst	TRST_: JTAG reset	VDDIO1
PPRST	I	L16	PU_rst	PPRST_: Power on reset and RESET-KEY reset input	VDDIO_RTC
TEST_TE	I	L13	PD_rst	TEST_TE: Manufacture test enable, program enable	VDDIO_RTC
POR_CTL	I	K16	PU_rst	POR_CTL: Power-on-Reset model bypass control	VDDIO_RTC
RST_OUT	O	J16	PD_rst	RST_OUT_: System Reset output	-
WKUP_PD31	I	J17	PU_rst	WKUP_: Wakeup signal after main power down	VDDIO_RTC
PWRON	O	K15	PU_rst	PWRON: Power on/off control of main power	VDDIO_RTC

5.8 Digital IO/CORE Power/Ground

Table5-8 Digital IO/CORE Power Supplies Pins (7)

Pin Names	IO	Loc	Pin Description	Power
VDD	P	H5,H6,H7,H8,H9,H10,H11,H12,H13,J5,J13,K5,K13,L5,M5,M6,N6,N7,N8,N9,N10	VDD: CORE digital power, 0.8V	-
VSS	P	G6,G7,G8,G9,G10,G11,G12,G13,J6,J7,J8,J9,J10,J11,J12,K6,K7,K8,K9,K10,K11,K12,L6,L7,L8,L9,L10,L11,L12,M7,M8,M9,M10,M11,M12,M13,N12	VSS: IO analog ground and CORE digital ground	-
VDDIO1	P	J14,P9	VDDIO1: 3.3V or 1.8V, for Fail-Safe type IO power supply	-
VDDIO2	P	C4	VDDIO2: 3.3V or 1.8V, for Fail-Safe type IO power supply	-
VDDIO18	P	K2,N11	VDDIO18*: For 1.8V type IO power supply	-
VDDIO_RTC	P	L17	VDDIO_RTC: 3.3V or 1.8V power for RTC and hibernating mode controlling that never power down	-
VDD_RTC	P	L15	VDD_RTC: 0.8V, Logic power supply for RTC	-

5.9 DDR PHY IO and Power Supply

Table5-9 DDR PHY IO and Power Supply Pins (6)

Pin Names	IO	Loc	Pin Description	Power
DDRPLL VCCA	P	B8	DDRPLL_VCCA: 1.5V/1.35V, DDR PHY PLL power supply for analog	-

Pin Names	IO	Loc	Pin Description	Power
DDR_ZQ	P	F13	Need to connect 240ohm resistor between this pad and VSSQ for ZQ Calibration	-
DDRVDD	P	F5,F6,F7,F8,F9,F10,F11,F12	power pin for DDR SIP in T41ZN(1.5V for DDR3, 1.35V for DDR3L)	-
DDRPLL VSSA	P	C9	Ground (PLL)	-
DDR_VREF	P	E5	Reference voltage	-
VDDMEM		E6,E7,E8,E9, E10,E11,E12	Power pin for DDR PHY in T41ZN(1.5V for DDR3, 1.35V for DDR3L)	

5.10 USB 2.0 PHY IO and Power Supply

Table5- 10 USB 2.0 PHY IO and Power Supply Pins(7)

Pin Names	IO	Loc	Pin Description	Power
USB0PP	IO	T2	USB0PP/ USB0PN: The differential input/output signals of the PHY that support multiple modes. Depending on mode of operation, they are either signaling 3.3 or 800mV differential.	USB_AVD33
USB0PN	IO	U1		
USB0ID	IO	U2	USB0ID: Used to identify the device attached to the PHY. The state of the pin is one of: high impedance(>1MΩ) or low impedance(<10Ω to ground)	USB_AVD18
USB_AVD08	P	R4	USB_AVD08: This is the analog supply that is used to support 0.8V circuits within the PHY.	-
USB_AVD18	P	T3	USB_AVD18: This is the analog supply that is used to support 1.8V signaling.	-
USB_AVD33	P	R3	USB_AVD33: This is the analog supply that is used to support 3.3V signaling.	-
VBUS	IO	U3	VBUS: power supply for the device and other USB functions.	USB_AVD33

5.11 MIPI-CSI IO and Power Supply

Table5-11 MIPI-CSI IO/Power Supply Pins(9)

Pin Names	IO	Loc	Pin Description	Power
CSI_VSSA	P	N5	CSI_VSSA: Analog power ground	-
CSI_VCCA08	P	N2	CSI_VCCA08: 0.8V analog supply voltage	-
CSI_VCCA18	P	K3	CSI_VCCA18: 1.8V analog supply voltage	-
CSI_CLKP	IO	L3	CSI_CLKP: Clock lane serial pins	CSI_VCCA18
CSI_CLKN	IO	M2	CSI_CLKN: Clock lane serial pins	CSI_VCCA18

Pin Names	IO	Loc	Pin Description	Power
CSI_DATAP0	IO	L1	CSI_DATAP0: Data lane 0 serial pins	CSI_VCCA18
CSI_DATAN0	IO	L2	CSI_DATAN0: Data lane 0 serial pins	CSI_VCCA18
CSI_DATAP1	IO	M3	CSI_DATAP1: Data lane 1 serial pins	CSI_VCCA18
CSI_DATAN1	IO	N1	CSI_DATAN1: Data lane 1 serial pins	CSI_VCCA18

5.12 Successive Approximation ADC(SAR-ADC) IO and Power Supply

Table5-12 Successive Approximation ADC(SAR-ADC) IO and Power Supply Pins (7)

Pin Names	IO	Loc	Pin Description	Power
SADC_VREFP	P	N16	SADC_VREFP: Positive reference Voltage input	-
SADC_AVDD	P	N17	SADC_AVDD: analog power, 1.8 V	-
SADC_AGND	P	N13	SADC_AGND: analog power, ground	-
SADC_VIN0	AIO	P15	SADC_VIN0:channel 0 input	SADC_AVDD
SADC_VIN1	AIO	R17	SADC_VIN1:channel 1 input	SADC_AVDD
SADC_VIN2	AIO	P16	SADC_VIN2:channel 2 input	SADC_AVDD
SADC_VIN3	AIO	N15	SADC_VIN3:channel 3 input	SADC_AVDD

5.13 Audio CODEC IO and Power Supply

Table5-13 Audio CODEC IO and Power Supply Pins (9)

Pin Names	IO	Loc	Pin Description	Power
MICNL	AIO	P2	MICNL: Left ADC channel input	CODEC_AVDD
MICPL	AIO	N3	MICPL: Left ADC channel input	CODEC_AVDD
HPOUTL	AIO	T1	HPOUTL: Left DAC channel output P end	CODEC_AVDD
VCM	AIO	R2	VCM: Reference voltage output	CODEC_AVDD
MICBIAS	AIO	P3	MICBIAS: Microphone bias output	CODEC_AVDD
CODEC_AVDD	P	R1	CODEC_AVDD:1.8V analog supply	-
CODEC_AVSS	P	P4	CODEC_AVSS: Digital ground	-

5.14 OTP IO and Power Supply

Table5-14 OTP IO and Power Supply Pins (1)

Pin Names	IO	Loc	Pin Description	Power
EFUSE_AVDD	P	D4	EFUSE_AVDD: EFUSE programming power, 1.8V	-

5.15 OSC and PLL IO and Power Supply

Table5-15 OSC and PLL IO and Power Supply Pins (4)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
EXCLK_XI	AI	C1	2~30 MHz Oscillator, OSC on/off	EXCLK_XI: external oscillator clock input or external 24MHz clock input	PLL_AVDD
EXCLK_XO	AO	D2		EXCLK_XO: external oscillator clock output	PLL_AVDD
PLL_AVDD	P	D3	-	PLL_AVDD: PLL analog power, 1.8V	-
PLL_AVSS	P	G5	-	PLL_AVSS: PLL analog power, ground	-


NOTE

1 The meaning of phases in IO cell characteristics are:

- Pull up: The IO cell contains a pull-up resistor and fixed pull up.
- Pull down: The IO cell contains a pull-down resistor and fixed pull down.
- PU_rst: The IO cell during reset and after the pull up function is enabled.
- PD_rst: The IO cell during reset and after the pull down function is enabled.
- Hi-Z-rst: The IO cell during reset and after the pull up and down function is disabled.
- SMT: The IO cell is Schmitt trigger input and fixed.
- SMT-rst: The IO cell during reset and after the Schmitt trigger input function is enabled.
- SR-rst: The IO cell during reset and after the slew-rate function select fast mode.
- SPU-rst: Some of the IO cells support Strong Pull up.

5.15.1 Electrical Characteristics

Test conditions: AVDD=1.8V, DVDD=0.9V, TA=25°C, 1KHz Sine Input, Fs=48KHz

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Operating Condition						
Analog Supply	AVDD		1.62	1.8	1.98	V
Digital Supply	DVDD		0.81	0.9	0.99	V
Microphone Bias						
Bias Voltage	V _{MICB}	-	0.5*AVDD	-	0.85*AVDD	V
Bias Current	I _{MICB}	-	-	-	3	mA
Microphone Gain Boost PGA						
Programmable Gain	G _{BST}	-	0	-	20	dB
Input Resistance	R _{IN}	-	8	-	88	KΩ
Input Capacitance	C _{IN}	-	-	10	-	pF
ALC PGA						
Programmable Gain	G _{ALC}	-	-18	-	28.5	dB
Gain Step Size	-	-	-	1.5	-	dB
ADC						

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Signal to Noise Ratio	SNR	A-weighted	-	92	-	dB
Total Harmonic Distortion	THD	-3dBFS input	-	-81	-	dB
Channel Separation	-	-	-	80	-	dB
Headphone Output Driver						
Programmable Gain	G _{DRV}	-	-39	-	6	dB
Gain Step Size	-	-	-	1.5	-	dB
Output Resistance	R _{OUT}	-	-	-	1	Ω
Output Capacitance	C _{OUT}	-	-	20	-	pF
Power Supply Rejection	P _{SRR}	1KHz	-	55	-	dB
Headphone Output						
Signal to Noise Ratio	SNR	A-weighted	-	93	-	dB
Total Harmonic Distortion	THD	60mW16Ω load	-	-70	-	dB
		30mW32Ω load	-	-75	-	dB
		-3dBFS output 600Ω load	-	-80	-	dB
Power Consumption						
Standby				0.05		mA
Recording				2.5		mA
Playback		Quiescent Output		2.5		mA

5.16 The Ball Assignment of T41ZN

Figure 5-1~Figure 5-4 show the ball assignment of T41ZN.

Figure5-1 T41ZN Ball Assignment (Part 1/4)

	0	1	2	3	4	5	6	7	8	9
A		MSC1_CLK_S SI0_CLK_PC 02	MSC1_D1_SS I0_DR_PC05	SSI_SLV_CE0 _I2S_DAC_L RCK_PWM1_ RTC32K_PC1 6		UART0_RTS_ I2S_ADC_MC LK_PC12		UART2_CTS_ SMB1_SDA_P C19		BOOT_SEL0_ PC00
B		MSC1_D3_SS I0_CE1_PC07	MSC1_D0_SS I0_DT_PC04	SSI_SLV_DT_ I2S_SDTO_P WM2_PC17	SSI_SLV_CLK _I2S_DAC_B CLK_PWM0_ EXCLK_PC15	SSI_SLV_DR _I2S_SDTLP WM3_PC18	UART0_TXD_ SMB2_SDA_P C08	UART2_TXD_I 2S_ADC_BCL K_PC13	DDRPLL_VC CA	BOOT_SEL1_ PC01
C		EXCLK_XIN	MSC1_D2_SS I0_GPC_PC0 6	MSC1_CMD_ SSI0_CE0_P C03	VDDIO2	UART0_CTS_ I2S_DAC_MC LK_PC11	UART0_RXD_ SMB2_SCK_P C09	UART2_RXD_ I2S_ADC_LR CK_PC14	UART2_RTS_ SMB1_SCK_P C20	DDRPLL_VSS A
D			EXCLK_XOUT	PLL_AVDD	EFUSE_AVDD					RZQ
E	SA1_DVP_MC LK_PA15	WAIT_PA19	SA2_PA18			DDR_VREF	VDDMEM	VDDMEM	VDDMEM	VDDMEM
F		SD5_DVP_D1 1_SSI0_CE1_ PA11	SA0_DVP_PC LK_DMIC_CL K_PA14			DDR_VDD	DDR_VDD	DDR_VDD	DDR_VDD	DDR_VDD
G	SD2_DVP_D8 _SSI0_DT_PA 08	SD3_DVP_D9 _SSI0_DR_P A09	SD4_DVP_D1 0_SSI0_GPC _PA10			PLL_AVSS	VSS	VSS	VSS	VSS
H		SD0_DVP_D6 _SSI0_CLK_P A06	SD1_DVP_D7 _SSI0_CE0_P A07			VDD	VDD	VDD	VDD	VDD
J	SD6_SMB0_S DA_PA12	CS2_DVP_HS YNC_DMIC_D AT0_PA16	RD_DVP_VSY NC_DMIC_DA T1_PA17	SD7_SMB0_S CK_PA13		VDD	VSS	VSS	VSS	VSS

Figure5-2 T41ZN Ball Assignment (Part 2/4)

10	11	12	13	14	15	16	17	
	DMIC_CLK_S MB2_SCK_SS I1_CLK_PB28		SLCD_TE_UA RT2_CTS_P WM4_PD09		SLCD_D0_BT 656_D0_UAR T3_TXD_PD0 0	SLCD_D2_BT 656_D2_UAR T4_TXD_PD0 2	SLCD_D4_BT 656_D4_UAR T5_TXD_PD0 4	A
GPIO_PB31	DRV_VBUS_S MB2_SDA_SS I1_DT_PB27	DMIC_DAT0_ UART4_TXD_ SSI1_DR_PB 29	SLCD_CS_U ART2_RTS_P WM5_PD10	SLCD_WR_B T656_PCLK_ PD08	SLCD_D1_BT 656_D1_UAR T3_RXD_PD0 1	SLCD_D5_BT 656_D5_UAR T5_RXD_PD0 5	SLCD_D6_BT 656_D6_SMB 1_SDA_PD06	B
SMB1_SCK_ UART3_RXD_ SSI1_GPC_P B26	SMB1_SDA_U ART3_TXD_S SI1_CE1_PB2 5	DMIC_DAT1_ UART4_RXD_ SSI1_CE0_P B30	SLCD_DC_U ART2_TXD_P WM6_PD11	SLCD_RDY_ UART2_RXD_ PWM7_PD12	SLCD_D3_BT 656_D3_UAR T4_RXD_PD0 3	SLCD_D7_BT 656_D7_SMB 1_SCK_PD07	UART0_RTS_ MSC1_D2_TM S_PB21	C
				TRST_	UART0_TXD_ MSC1_D3_PB 22	UART0_RXD_ MSC1_CMD_ PB19		D
VDDMEM	VDDMEM	VDDMEM			UART0_CTS_ MSC1_CLK_T CK_PB20	PWM0_MSC1 _D0_PB17	PWM1_MSC1 _D1_PB18	E
DDRVD	DDRVD	DDRVD	DDR_ZQ		UART1_TXD_ TDO_PB23	UART1_RXD_ TDI_PB24		F
VSS	VSS	VSS	VSS		MSC0_D2_PB 02	MSC0_D3_PB 03	MSC0_CMD_ PB05	G
VDD	VDD	VDD	VDD		MSC0_CLK_P B04	MSC0_D0_PB 00		H
VSS	VSS	VSS	VDD	VDDIO1	MSC0_D1_PB 01	RST_OUT	WKUP_PD31	J

Figure5-3 T41ZN Ball Assignment(Part 3/4)

J	SD6_SMB0_S DA_PA12	CS2_DVP_HS YNC_DMIC_D AT0_PA16	RD_DVP_VSY NC_DMIC_DA T1_PA17	SD7_SMB0_S CK_PA13	VDD	VSS	VSS	VSS	VSS
K		VDDIO18	CSI_VCCA18		VDD	VSS	VSS	VSS	VSS
L	CSI_DATAP0	CSI_DATAN0	CSI_CLKP		VDD	VSS	VSS	VSS	VSS
M		CSI_CLKN	CSI_DATAP1		VDD	VDD	VSS	VSS	VSS
N	CSI_DATAN1	CSI_VCCA08	MICPL		CSI_VSSA	VDD	VDD	VDD	VDD
P		MICNL	MICBIAS	CODEC_AVS S					VDDIO1
R	CODEC_AVD D	VCM	USB_AVD33	USB_AVD08	SFC0_DR_IO 1_PA24	SFC0_CLK_P A27	SSI1_CE0_SF C1_CE_PA29	SSI1_DT_SF C1_DT_IO0_ PA20	SSI1_GPC_S FC1_HOLD_I O3_PA31
T	HPOUTL	USB0PP	USB_AVD18	SFC0_CE_PA 28	SFC0_WP_IO 2_PA26	SFC0_HOLD_ IO3_PA25	SSI1_DR_SF C1_DR_IO1_ PA21	SSI1_CLK_SF C1_CLK_PA2 2	GMAC_PHY_ CLK_UART5_ RXD_PB07
U	USB0PN	USB0ID	VBUS		SFC0_DT_IO 0_PA23		SSI1_CE1_SF C1_WP_IO2_ PA30		GMAC_RXDV _I2S_DAC_L RCK_PWM3_ PB09
	1	2	3	4	5	6	7	8	9

Figure5-4 T41ZN Ball Assignment(Part 4/4)

VSS	VSS	VSS	VDD	VDDIO1	MSC0_D1_PB01	RST_OUT	WKUP_PD31	J
VSS	VSS	VSS	VDD		PWRON	POR_CTL		K
VSS	VSS	VSS	TEST_TE		VDD_RTC	PPRST_	VDDIO_RTC	L
VSS	VSS	VSS	VSS		OSC32_XO	OSC32_XI		M
VDD	VDDIO18	VSS	SADC_AGND		SADC_VN3	SADC_VREFF	SADC_AVDD	N
				NC	SADC_VN0	SADC_VN2		P
GMAC_MDCK_I2S_ADC_MCLK_SMB2_SDA_PB10	GMAC_TXD0_I2S_ADC_BCLK_PWM4_PB13	GMAC_RXD1_I2S_SDTOPWM7_PB16	NC	NC	NC	NC	SADC_VN1	R
GMAC_MDIO_I2S_DAC_MCLK_SMB2_SCK_PB11	GMAC_TXD1_I2S_ADC_LRCLK_PWM5_PB14	GMAC_TXCLK_UART5_TXD_PB06	NC	NC	NC	NC	NC	T
	GMAC_TXEN_I2S_DAC_BCLK_PWM2_PB08		GMAC_RXD0_I2S_SDTIPWM6_PB15		NC	NC	NC	U
10	11	12	13	14	15	16	17	

6 Electrical Specifications

6.1 Power Consumption Parameters

Table 6-1 describes power consumption parameters.



- The values of power consumption parameters are provided based on typical application scenarios.
- Design board power supplies by following the T41ZN Hardware Design User Guide.

Table 6-1 Power consumption parameters

Symbol	Parameter	Typ	Max	Unit
VDD_DDR	VDD DDR core power	TBD	TBD	mW
VDD_CPU	CPU core power	TBD	TBD	mW



The VDD and DDR core power supplies need to be combined into one power supply. For details, see the T41ZN Hardware Design User Guide.

6.2 Recommended Operating Conditions

Table 6-2 Recommended operating conditions for power supplies

Symbol	Description	Min	Typ	Max	Unit
VDDMEM	VDDMEM voltage for SSTL18 (DDR3/DDR3L)	1.425/ 1.283	1.5/ 1.35	1.575 /1.45	V
DDRVDD	DDR3/DDR3L KGD power supplies voltage	1.425/ 1.283	1.5/ 1.35	1.575 /1.45	V
DDRPLL_VCCA	DDR PLL power supplies voltage	1.62	1.8	1.98	V
VDDIO2	GPIO power domain 2 supplies voltage	2.97/ 1.62	3.3/ 1.8	3.63/ 1.98	V
VDDIO1	GPIO power domain 1 supplies voltage	2.97/ 1.62	3.3/ 1.8	3.63/ 1.98	V
VDDIO18	GPIO power domain 0 supplies voltage	1.62	1.8	1.98	V
VDDIO33_RTC	3.3V power for RTC and hibernating mode controlling that never power down	2.97/ 1.62	3.3/ 1.8	3.63/ 1.98	V
VDD	VDD core supplies voltage	0.72	0.8	0.88	V

Symbol	Description	Min	Typ	Max	Unit
VDD_RTC	Logic power supply for RTC	0.72	0.8	0.88	V
PLL_AVDD	PLL analog voltage	1.62	1.8	1.98	V
EFUSE_AVDD	EFUSE program supplies voltage	1.62	1.8	1.98	V
SADC_AVDD	SAR-ADC analog voltage	1.62	1.8	1.98	V
CSI_VCCA08	MIPI RX 0.8V analog supply voltage	0.72	0.8	0.88	V
CSI_VCCA18	MIPI RX 1.8V analog supply voltage	1.62	1.8	1.98	V
USB_AVDD08	USB PHY AVDD08 analog voltage	0.72	0.8	0.88	V
USB_AVDD18	USB PHY AVDD18 analog voltage	1.62	1.8	1.98	V
USB_AVDD33	USB PHY AVDD33 analog voltage	3.0	3.3	3.6	V
CODEC_AVDD	CODEC analog voltage	1.62	1.8	1.98	V

Table 6-3 Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
V _{DD}	Pre-Driver voltage	0.72	0.8	0.88	V
V _{DDPST}	Post-Driver voltage	1.62	1.8	1.98	V
V _{IMAX}	Maximum input voltage			V _{DDIO} +0.3	V
V _{DDramp-upslew}	Ramp up slew for VDD			0.018	V/us
V _{DDIOramp-upslew}	Ramp up slew for VDDIO			0.018	V/us


NOTE

The V_{imax} is not for DC signal level, but just for a reference of over-shoot/under-shoot, no guarantee of electrical spec and reliability.

Table6-4~Table6-5 describe the recommended operating conditions for VDDIO1/VDDIO2 supplied pins.

Table 6-4 Recommended operating conditions [3.3V Logic]

Parameter	Description	Min	Typ	Max	Unit
V _{VDD}	Core supply voltage	0.72	0.8	0.88	V
V _{DVDD}	I/O supply voltage	2.97	3.3	3.63	V
V _{PAD}	Voltage at IO	-0.3	-	V _{DVDD} +0.3	V
V _{IH}	High-level input voltage at IO	2	-	V _{DVDD} +0.3	V
V _{IL}	Low-level input voltage at IO	V _{DVSS} -0.3	-	0.8	V

Table 6-5 Recommended operating conditions [1.8V Logic]

Parameter	Description	Min	Typ	Max	Unit
V _{VDD}	Core supply voltage	0.72	0.8	0.88	V
V _{DVDD}	I/O supply voltage	1.62	1.8	1.98	V
V _{PAD}	Voltage at IO	-0.3	-	V _{DVDD} +0.3	V
V _{IH}	High-level input voltage at IO	0.65*V _{DVDD}	-	V _{DVDD} +0.3	V

Parameter	Description	Min	Typ	Max	Unit
V _{IL}	Low-level input voltage at IO	V _{DVSS} -0.3	-	0.35*V _{DVDD}	V

Table 6-6 Recommended operating conditions for others

Symbol	Description	Min	Typ	Max	Unit
T _A	Operating Ambient Temperature	TBD	25	TBD	°C
T _J	Operating Junction Temperature	TBD	25	TBD	°C
T _J	Maximum Junction Temperature	TBD	25	TBD	°C
T _{STG}	Storage Temperature	TBD	25	TBD	°C

6.3 General Purpose Input/Output(GPIO)

Power Domain	Voltage Supply
VDDIO1	VDDIO18/VDDIO33
VDDIO2	VDDIO18/VDDIO33
VDDIO18	VDDIO18
VDDIO_RTC	VDDIO33

6.3.1 Power Domain VDDIO18 DC Characteristics

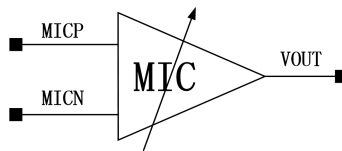
Parameter	Min	Nom	Max	Unit
V _{IL} Input Low Voltage	-0.3	-	0.35*VDDIO	V
V _{IH} Input High Voltage	0.65*VDDIO	-	VDDIO+0.3	V
V _T Threshold Point	0.91	1.12	1.12	V
V _{T+} Schmitt Trigger Low to High Threshold Point	0.98	1.18	1.2	V
V _{T-} Schmitt Trigger High to Low Threshold Point	0.75	0.96	0.96	V
V _{T_{PU}} Threshold Point with Pull-up Resistor Enabled	0.82	1.06	1.06	V
V _{T_{PD}} Threshold Point with Pull-down Resistor Enabled	0.92	1.12	1.13	V
V _{T_{PU}} ⁺ Schmitt Trigger Low to High Threshold Point with Pull-up Resistor Enabled	0.86	1.12	1.13	V
V _{T_{PU}} ⁻ Schmitt Trigger High to Low Threshold Point with Pull-up Resistor Enabled	0.7	0.92	0.92	V
V _{T_{PD}} ⁺ Schmitt Trigger Low to High Threshold Point with Pull-down Resistor Enabled	0.98	1.19	1.22	V
V _{T_{PD}} ⁻ Schmitt Trigger High to Low Threshold Point with Pull-down Resistor Enabled	0.76	0.97	0.97	V
V _{T_{SPU}} Threshold Point with Strong Pull-up Resistor Enabled	0.83	1.05	1.05	V
V _{T_{SPU}} ⁺ Schmitt Trigger Low to High Threshold Point with strong Pull-up Resistor Enabled	0.92	1.11	1.11	V
V _{T_{SPU}} ⁻ Schmitt Trigger High to Low Threshold Point with strong Pull-up Resistor Enabled	0.63	0.88	0.88	V

Parameter		Min	Nom	Max	Unit
I _I	Input Leakage Current @ V _I = 1.8V or 0V	-	-	±10μ	A
I _{OZ}	Tri-state Output Leakage Current @ V _O = 1.8V or 0V	-	-	±10μ	A
R _{SPU}	Strong Pull-up Resistor	1.6k	2.1k	3k	Ω
R _{PU}	Pull-up Resistor	32k	49k	79k	Ω
R _{PD}	Pull-down Resistor	30k	36k	65k	Ω
V _{OL}	Output Low Voltage	-	-	0.45	V
V _{OH}	Output High Voltage	VDDIO-0.45	-	-	V

6.4 Audio Codec

6.4.2 Analog Interface Description

Microphone input



There are two inputs channels named left ADC channel and right ADC channel. In the each channel, there are two inputs which are configured as differential input by the microphone PGA(MICL and MICR).

In the left channel, microphone inputs are MICPL and MICNL. In the right channel, microphone inputs are MICPR and MICRL.

Microphone PGA has a gain range from 0dB to 20dB.

ALC

Automatic Level Control (ALC) function is included to adjust the signal level, which is input into ADC. ALC will measure the signal magnitude and compare it to defined threshold. Then it will adjust the ALC controlled PAG (ALC_L and ALC_R) gain according to the comparison result.

The programmable gain range of ALC controlled PAG is from -18dB to +28.5dB. The tuning step is 1.5dB.

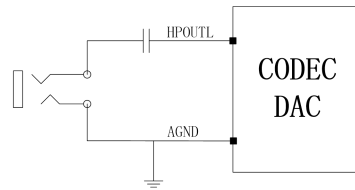
DAC OUTPUT

Support headphone output or line output configurations. The output can drive load through DC-blocking capacitor.

In the configuration using DC-blocking capacitor, shown in the following figure, the headphone ground is connected to the real ground. The capacitance and the resistance determine the lower cut-off frequency. For instance, if 600Ω load and 4.7uF DC-blocking capacitor is used, the lower cut-off frequency is:

$$f = \frac{1}{2 \times RC} = \frac{1}{2 \times 600 \times 4.7 \times 10^{-6}} = 56.5Hz$$

The DC-blocking capacitor can be increased to lower the cut-off frequency for better bass response.



The out driver has a gain range from -39dB to +6dB with a tuning step of 1.5dB.

Microphone Bias

The output of the Microphone bias is used for bias external microphones. The bias voltage can vary from $0.5 \times \text{CODEC_AVDD}$ to $0.85 \times \text{CODEC_AVDD}$ with a step of $0.025 \times \text{CODEC_AVDD}$.

6.5 USB 2.0 OTG PHY

6.5.1 DC/AC Specifications

Table 6-7 Transmitter Specification

Description	Min	Typ	Max	Unit
USB_AVDD08	0.72	0.8	0.88	V
USB_AVDD18	1.62	1.8	1.98	V
USB_AVDD33	3.0	3.3	3.6	V
High input level(V_{IH})	-	1.2	-	V
Low input level(V_{IL})	-	0	-	V
Output resistance(R_{OUT}) Classic mode($V_{OUT} = 0$ or $3.3V$)	40.5	45	49.5	ohms
HS mode($V_{OUT} = 0$ to $800mV$)	40.5	45	49.5	ohms
Output capacitance(seen from D+ or D-)(C_{OUT})	-	-	3	pF
Differential output signal high Classic(LS/FS); $I_O = 0mA(V_{OH})$	2.97	3.3	3.63	V
Classic(LS/FS); $I_O = 6mA$	2.2	2.7	-	
HS mode; $I_O = 0mA$	360	400	440	mV
Differential output signal low Classic(LS/FS); $I_O = 0mA(V_{OL})$	-0.33	0	0.33	V
Classic(LS/FS); $I_O = 6mA$	-	0.3	0.8	
HS mode; $I_O = 0mA$	-40	0	40	mV
Output Common Mode Voltage Classic(LS/FS) mode(V_M)	1.45	1.65	1.85	V
HS mode	0.175	0.2	0.225	V
Rise and fall time LS mode	75	87.5	300	ns
(T_R/T_F) FS mode	4	12	20	ns
HS mode	0.8	1.0	1.2	ns
Vring into load	-	-	10	%
Propagation delay(data to D+/D-) LS mode	30	TBD	300	ns
FS mode	0		12	ns
HS mode	-		-	ns
Propagation delay(tx_en to D+/D-) Classic mode (TPZH/TPZL)	-	-	2	ns
HS mode	-	-	2	ns

Description	Min	Typ	Max	Unit
Adaptive termination acquisition	-	-	7.5	7.5MHz Cycles

Table 6-8 Receiver Specifications

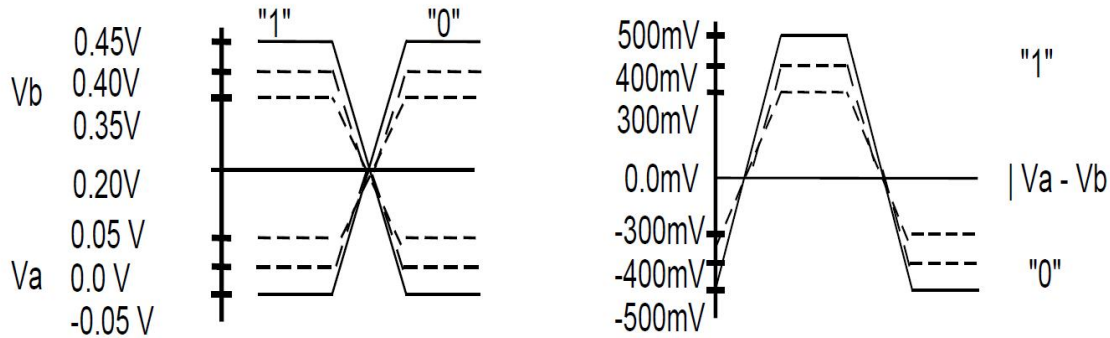
Description	Min	Typ	Max	Unit
USB_AVD33	3.0	3.3	3.6	V
Receiver sensitivity(RSENS)				
Classic mode		+250		mV
HS mode		+25		mV
Receiver common mode(RCM)				
Classic mode	0.8	1.65	2.5	V
HS mode(differential and squelch comparator)	0.1	0.2	0.3	V
HS mode(disconnect comparator)	0.5	0.6	0.7	V
Input capacitance(seen at D+ or D-)	-	-	3	pF
Squelch threshold	100	-	150	mV
Disconnect threshold	570	600	664	mV
High output level(V _{OH})	-	1.8	-	V
Low output level(V _{OL})	-	0	-	V
Propagation delay(TP)				
Classic mode(D+/D- to cl_diff_rx)			16	ns
Classic mode(D+/D- to se_datap_rx or se_datam_rx)			8	ns
HS mode(D+/D- to input of DLL)			1	ns

Table 6-9 Reference Specification

Description	Min	Typ	Max	Unit
USB_AVD18	1.62	1.8	1.98	V
Bandgap voltage(5% tolerance)	1.18	1.25	1.312	V
Current reference(2% tolerance)	290	300	306	uA
Power	-	-	6	mW
Reference_en to stable voltage reference	-	-	4	us

Table 6-10 Clock and Data Recovery Specification

Description	Min	Typ	Max	Unit
USB_AVD08	0.72	0.8	0.88	V
Bit loss				
*The total bit loss through a receive path is 4 bit times. This is divided between the Rx un-squelching circuitry and the DLL.	-	-	4	bits
Latency(intrinsic)	-	-	4	clock cycles
Latency(elasticity buffer)	-	-	17	clock cycles

Figure 6-1 Single Ended Signal Swing Differential Signal Swing

Table 6-11 VBUS DC Parameters

Parameter	Symbol	Min	Typ	Max	Unit
VBUS Voltage					
VBUS Output Voltage	VBUS	4.6	-	5.25	V
VBUS_VALID Comparator Threshold	-	4.4	4.5	4.6	V
SESSION_VALID Comparator Threshold	-	1.0	1.4	1.8	V
B_SESSION_END Comparator Threshold	-	0.4	0.5	0.6	V
Pull up/Pull down Resistor Specifications(DP,DM,UID)					
Pull down Resistor on DP	-	14.5	15	16	K Ω
Pull down Resistor on DM	-	14.5	15	16	K Ω
Pull up Resistor on DP	-	2.35	2.4	2.5	K Ω
Pull up Resistor in DM	-	2.35	2.4	2.5	K Ω
UID Pull up Resistor	-	160	200	240	K Ω

6.6 Power On, Reset and BOOT

6.6.1 Power-On Sequence

The external voltage regulator and other power-on devices must provide the T41ZN processor with a specific sequence of power and resets to ensure proper operation. Figure 6-2 shows this sequence and Table 6-11 gives the timing parameters. Following are the name of the power.

- VDD08: all 0.8V power supplies: VDD, CSI_VCCA08, USB_AVD08
- VMEM: DDRVDD, VDDMEM
- VDDIO18: all other digital IO: VDDIO2, DDRPLL_VCCA, VDDIO18, PLL_AVDD, SADC_AVDD, CSI_VCCA18, USB_AVD18, CODEC_AVDD
- VDDIO33: VDDIO1, VDDIO2, VDDIO18_RTC, USB_AVD33

Table 6-12 Power-On Sequence Parameters

	Parameter	Min	Max	Unit
T1	VDDIO18 rise time ^[1]	TBD	TBD	ms
T2	VDD08 rise time	TBD	TBD	ms
T3	VMEM rise time	TBD	TBD	ms

	Parameter	Min	Max	Unit
T4	VDDIO33 rise time	TBD	TBD	ms
T5	Delay between VDDIO18 arriving 50% to VDD095 arriving 50%	TBD	TBD	ms
T6	Delay between VDD08 arriving 50% to VMEM arriving 50%	TBD	TBD	ms
T7	Delay between VMEM arriving 50% to VDDIO33 arriving 50%	TBD	TBD	ms
T8	Delay between VDD08 arriving 50% to POR_OUT arriving 50%	120	TBD	us
T9	Delay between POR_OUT arriving 50% to CHIP inner reset arriving 50%	10	TBD	ms
T10	PPRST_ kept time ^[2]	100	TBD	us
T11	VDDIO_RTC rise time	TBD	TBD	ms
T12	VDD_RTC rise time	TBD	TBD	ms
T13	Delay between VDDIOIO_RTC arriving 50% to VDD_RTC arriving 50%	TBD	TBD	ms
T14	Delay between VDDIO_RTC arriving 50% to VDDIO18 arriving 50%	TBD	TBD	ms


NOTE

- [1]: The power rise time is defined as 10% to 90%.
- [2]: The PPRST_ must be kept at least 100us.

Figure 6-2 Power-On Sequence Diagram

TBD

6.6.2 Reset procedure

There are 4 reset sources: 1. PPRST_ pin reset; 2. POR hardware reset and 3. WDT timeout reset; 4. Hibernating reset. After reset, program start from boot.

- PPRST_ pin reset.

This reset is triggered when PPRST_ pin is put to logic 0. It happens in power on RTC power and RESET-KEY pressed to reset the chip from unknown dead state. The reset end time is about 1M EXCLK cycles after rising edge of PPRST_.

- POR(Power-On-Reset) hardware reset.

The chip POR circuit provides reliable reset function for general applications. Powered by 1.8V analog supply and monitors 0.8V digital and 1.8V analog supply. It generates reset signal to digital logic. Set low if analog supply or digital supply is below the threshold voltage (typical 1.35V threshold for 1.8V supply and 0.6V threshold for 0.8V supply), and will be set high if both of analog supply and digital supply exceed the threshold voltage.

- WDT reset.

This reset happens in case of WDT timeout. The reset keeps for about a few RTCLK cycles.

After reset, all GPIO shared pins are put to GPIO input function (excluded JTAG pins) and most of their

internal pull-up/down resistor are set to on, see “2.2Pin Description” for details. The oscillators are on.

- Hibernating reset.

This reset happens in case of wake up the main power from power down. The reset keeps for about 15ms ~ 250ms programmable, plus 1M EXCLK cycles, start after WKUP_ signal is recognized.

6.6.3 BOOT

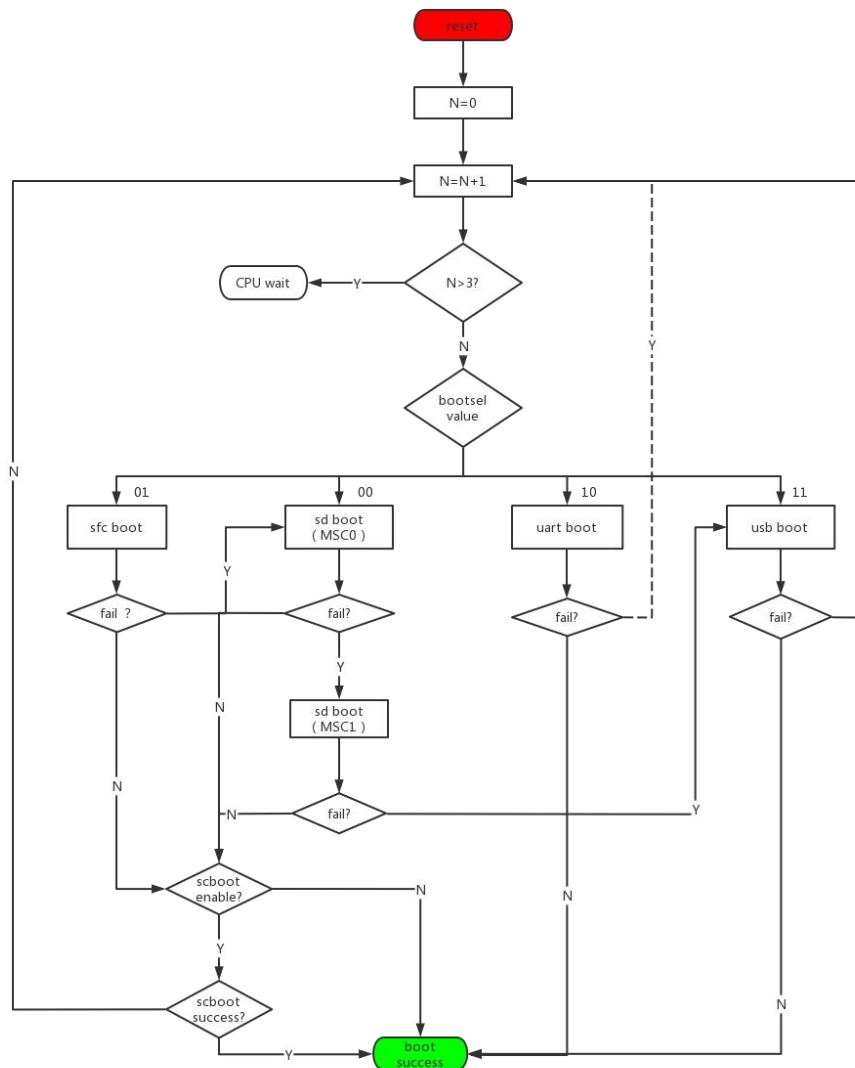
The boot sequence of the T41ZN is controlled by boot_sel[1:0]. The configuration is shown as follow:

Table 6-13 Boot Configuration of T41ZN

boot_sel[1:0]	Boot method
00	MMC/SD boot @ MSC0 (MMC/SD use GPIO Port B. MSC1 use GPIO Port C)
01	SFC boot @ CS4 (SPI boot)
10	UART boot @ CS2(Ymodem@115200/9600)
11	USB boot @USB2.0 device, EXTCLK=24MHz

1. When SFC boot start failure, the program in bootrom will go into MSC0 boot. If it is boot from MMC/SD card at MSC0, its function pins MSC0_D0~MSC0_D3, MSC0_CLK, MSC0_CMD are initialized, the boot program loads the maximum 100KB code from MMC/SD card to cache and jump to uboot spl. By default, four data buses MSC0_D0 to MSC0_D3 are used. If they fail, use one data bus MSC0_D0.
2. When MSC0 boot start failure, the program in bootrom will go into MSC1 boot. If it is boot from MMC/SD card at MSC1, its function pins MSC1_D0~MSC1_D3, MSC1_CLK, MSC1_CMD are initialized, the boot program loads the maximum 100KB code from MMC/SD card to cache and jump to it. By default, four data buses MSC1_D0 to MSC1_D3 are used. If they fail, use one data bus MSC1_D0. If MSC1 boot start failure, jump to USB boot.
3. To use UART boot, bootsel[1:0] must be set to 10. When UART boot fails, no other boot methods will be tried. The UART boot only supports the Ymodem protocol. The default baud rate is 115200. If the UART boot fails, 9600 baud rate will be attempted.

Figure 6-3 Boot sequence diagram of T41ZN



As shown in boot sequence Block Diagram, after reset, the boot program on the internal boot ROM executes as follows:

1. Disable all interrupts and read boot_sel[0] and boot_sel[1] to determine the boot method.
2. There 26KB backup reading failed, the 26KB backup at 128th, 256th , ..., and finally 1024th page will be tried in consecutive order.
3. If it is boot from MMC/SD card at MSC0, its function pins MSC0_D0~ MSC0_D3, MSC0_CLK, MSC0_CMD are initialized, the boot program loads the maximum 100KB code from MMC/SD card to cache and jump to it.
4. If it is boot from USB, a block of code will be received through USB cable connected with host PC and be stored in cache. Then branch to this area in cache.

5. If it is boot from SPI nor/nand at SFC, its function pins SFC_CLK, SFC_CE, SFC_DR, SFC_DT, SFC_WP, SFC_HOLD are initialized, the boot program loads the maximum 100KB code from SPI NAND/NOR flash to cache and jump to it.
6. If uart boot is used, rx and tx of uart1 are initialized for protocol sending and receiving. The maximum value is 100KB.

7 Thermal Characteristics

7.1 Temperature and Thermal Resistance Parameters

Table 7-1, Table 7-2, and Table 7-3 describe temperature and thermal resistance parameters.

Table 7-1 Operating environment parameters

Symbol	Parameter	Min	Max	Unit
Ambient temperature	T_A	TBD	TBD	°C



- Under no condition can the chip junction temperature exceed the destructive junction temperature in Table 7-1. If the chip junction temperature exceeds the destructive junction temperature, the chip may be physically damaged.
- Under normal working conditions, the chip junction temperature should be less than or equal to the maximum junction temperature for normal working in Table 7-1.

Table 7-2 lists the requirements on the junction temperatures of T41ZN.

Table 7-2 Requirements on the junction temperatures of T41ZN

Package	Maximum Junction Temperature for Normal Working (°C)	Destructive Junction Temperature (°C)
TFBGA	TBD	TBD

Table 7-3 lists the thermal resistance parameters of T41ZN.

Table 7-3 Thermal resistance parameters

Parameter	Symbol	Min	Typ	Max	Unit
Junction-to-ambient thermal resistance	θ_{JA}	TBD	TBD	TBD	°C/W
Junction-to-board thermal resistance	θ_{JB}	TBD	TBD	TBD	°C/W
Junction-to-case thermal resistance	θ_{JC}	TBD	TBD	TBD	°C/W

8 Interface Timings

8.1 SFC Interface Timings

8.1.1 Propagation Delay

The propagation delay do not effect the data transmission and it would not effect the data reception when the serial clock has a low frequency as shown in the Figure 8-1.

But when the serial clock run at a fast frequency the propagation delay will cause the incoming data could not arrival at the right clock edge then the sampling point should be adjustable as shown in the Figure 8-2.

Figure 8-1 Sample Point (No Delay)

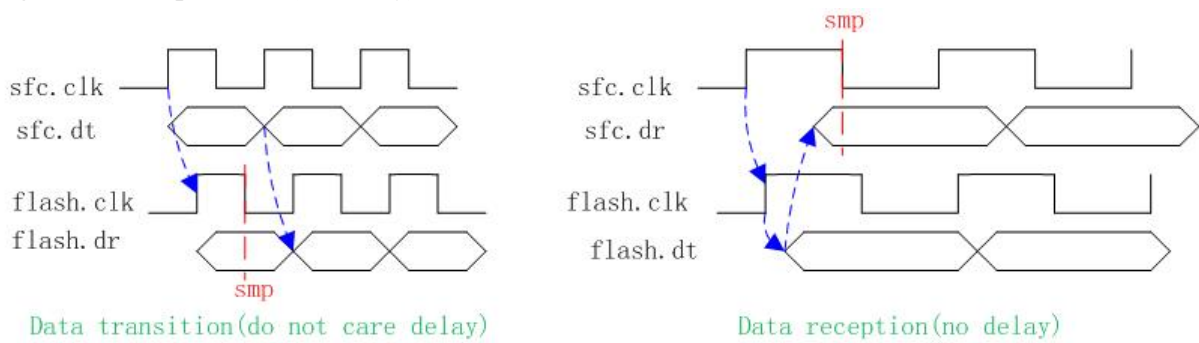
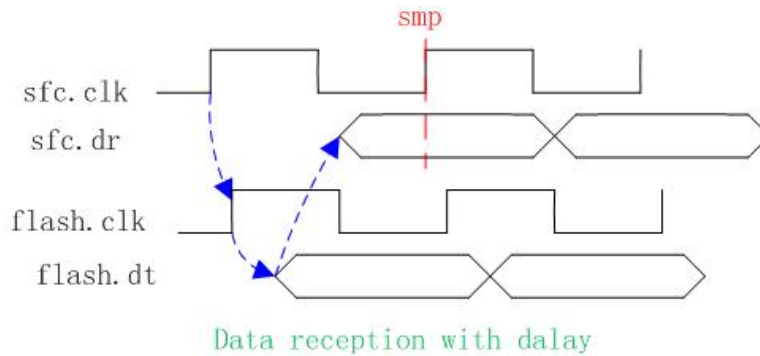


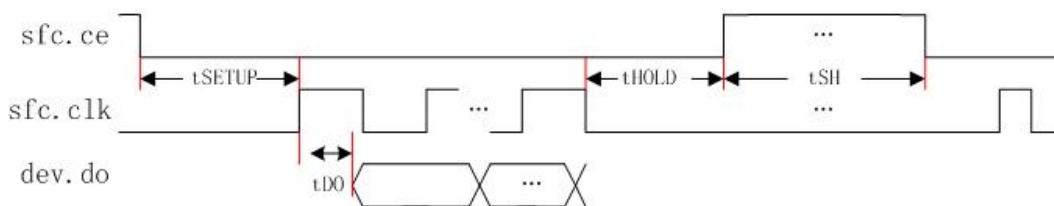
Figure 8-2 Sample Point (Delay)



8.1.2 AC Timing

Tsetup (tSLCH), tHOLD (tCHSH), tSH (tSHSL), are configurable.

Figure 8-3 AC Timing



8.2 Ethernet MAC Port Timings

8.2.1 RMII Timings

Figure 8-4 shows the 10/100 Mbit/s RX timing of the RMII.

Figure 8-4 10/100 Mbit/s RX timing of the RMII

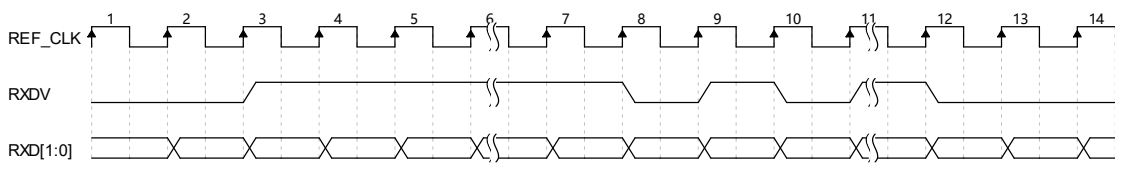


Figure 8-5 shows the 10/100 Mbit/s TX timing of the RMII.

Figure 8-5 10/100 Mbit/s TX timing of the RMII

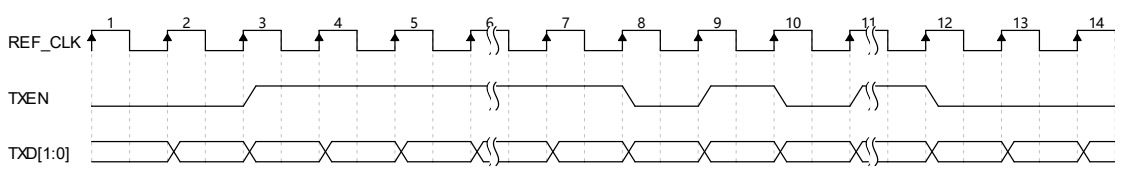


Figure 8-6 shows the timing parameters of the RMII.

Figure 8-6 Timing parameters of the RMII

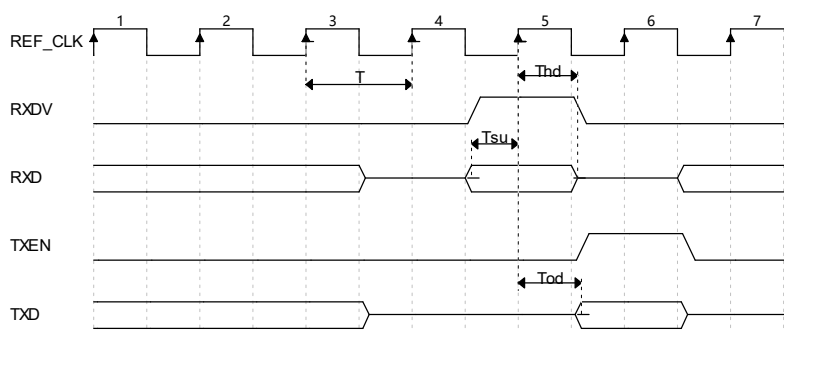


Table 8-1 describes the RMII timing parameters of the RMII.

Table 8-1 Timing parameters of the RMII

Parameter	Symbol	Signal	Min	Max	Unit
RMII clock cycle	T	REF_CLK	20	20	ns
Setup time of RMII signal	Tsu (RX)	RXDV/RXD[1:0]	4	N/A	ns
Hold time of RMII signal	Thd (RX)	RXDV/RXD[1:0]	2	N/A	ns
RMII output signal delay	Tod (TX)	TXEN/TXD[1:0]	3	16	ns

8.2.2 MDIO Interface Timings

Figure 8-7 shows the read timing of the MDIO interface.

Figure 8-7 Read timing of the MDIO interface

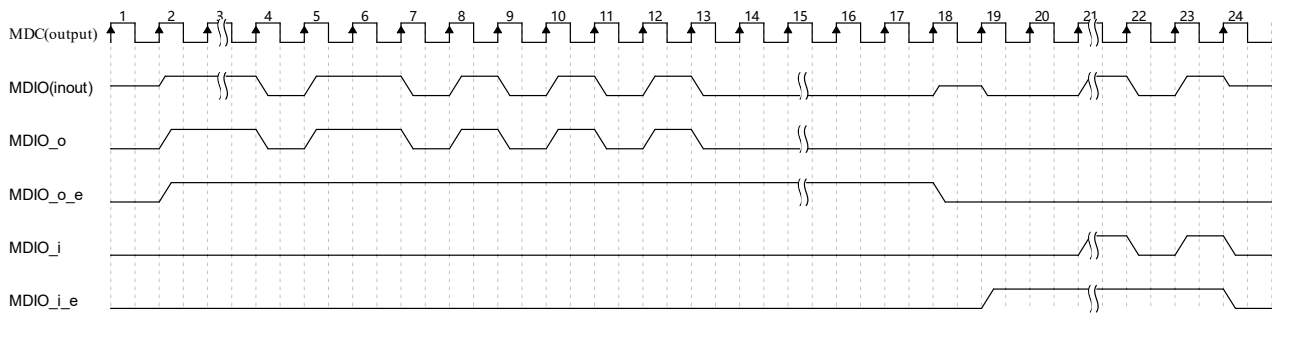


Figure 8-8 shows the write timing of the MDIO interface.

Figure 8-8 Write timing of the MDIO interface

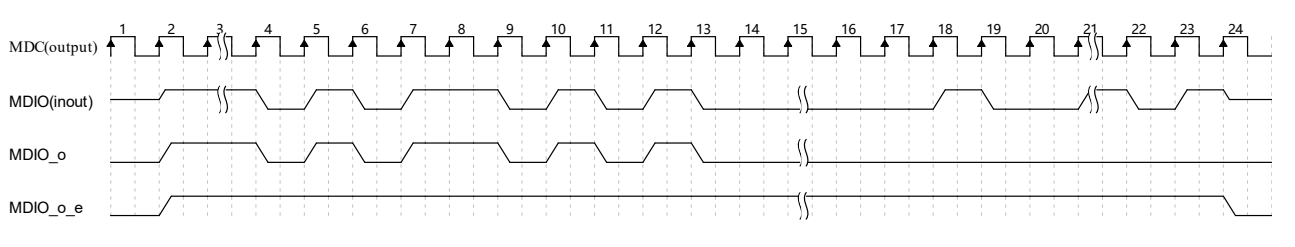


Figure 8-9 shows the RX timing parameters of the MDIO interface.

Figure 8-9 RX timing parameters of the MDIO interface

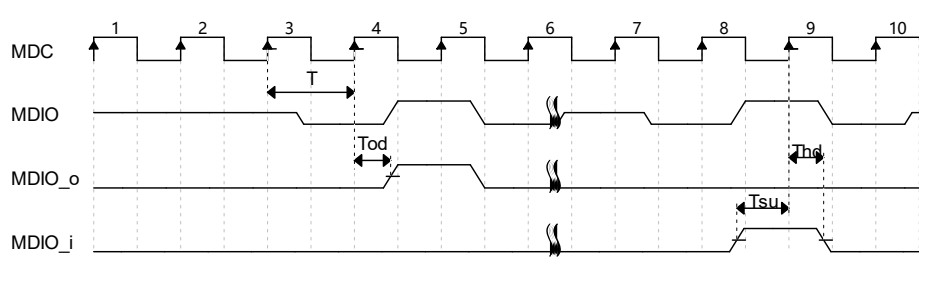


Table 8-2 describes the timing parameters of the MDIO interface.

Table 8-2 Timing parameters of the MDIO interface

Parameter	Symbol	Signal	Min	Max	Unit
MDIO clock cycle	T	MDC	400	400	ns
MDIO output signal delay	Tod(TX)	MDIO	0	300	ns
Setup time of MDIO signal	Tsu(RX)	MDIO	10	N/A	ns
Hold time of MDIO signal	Thd(RX)	MDIO	10	N/A	ns

8.3 VI Interface Timing

8.3.1 BT/DVP Timings

Figure 8-10 shows the VI interface timing in CMOS mode.

Figure 8-10 VI interface timing in CMOS mode

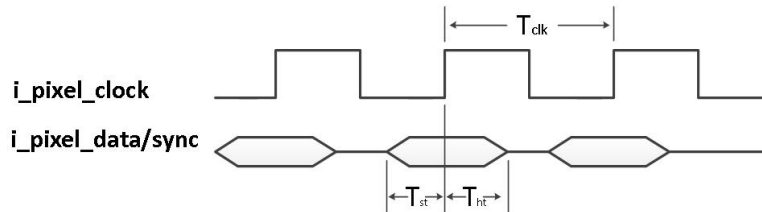


Table 8-3 describes the VI interface timing parameters.

Table 8-3 VI interface timing parameters

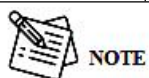
Parameter	Symbol	Min	Typ	Max	Unit
Video Input clock cycle	T_{clk}	6.0	N/A	N/A	ns
Input signal setup time	T_{st}	TBD	N/A	N/A	ns
Input signal hold time	T_{ht}	TBD	N/A	N/A	ns

8.3.2 MIPI-CSI Timings

Table 8-4 describes the MIPI-CSI timing parameters.

Table 8-4 MIPI-CSI timing parameters

Symbol	Description	Min	Tye	Max	Unit
F_{MAX}	Data rate	N/A	N/A	2	Gbit/s
T_{PERIOD}	Differential clock cycle	1	T	N/A	ns
$TDUTY$	Differential clock duty cycle	0.45T	N/A	0.55T	ns
$TSET$	Differential clock setup time	0.15 x UI	N/A	N/A	ns
THD	Differential clock hold time	0.15 x UI	N/A	N/A	ns
$TRISE$	Differential clock rising time (20%–80%)	0.15	N/A	N/A	ns
$TFALL$	Differential clock falling time (20%–80%)	N/A	N/A	0.3 x UI	ns



UI = T/2

8.4 Video Output Interface Timings

Figure 8-11 shows the BT.656/BT.1120 interface timing.

Figure 8-11 BT.656/BT.1120 interface timing

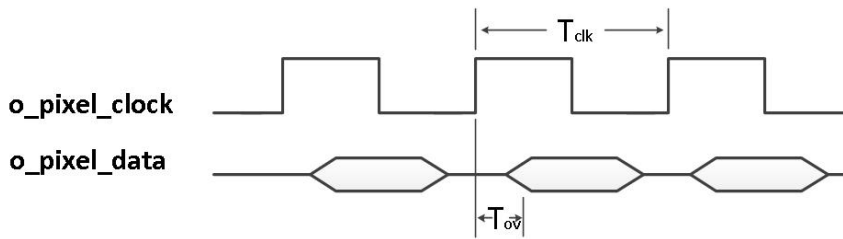


Table 8-5 describes the timing parameters of the BT.656/BT.1120 interface.

Table 8-5 Timing parameters of the BT.656/BT.1120 interface

Parameter	Symbol	Min	Typ	Max	Unit
Video Out clock cycle	Tclk	6	N/A	N/A	ns
Output signal delay	Tov	TBD	N/A	TBD	ns

Figure 8-12 shows the Chip select timing and Address timing.

Figure 8-12 Chip select timing and Address timing

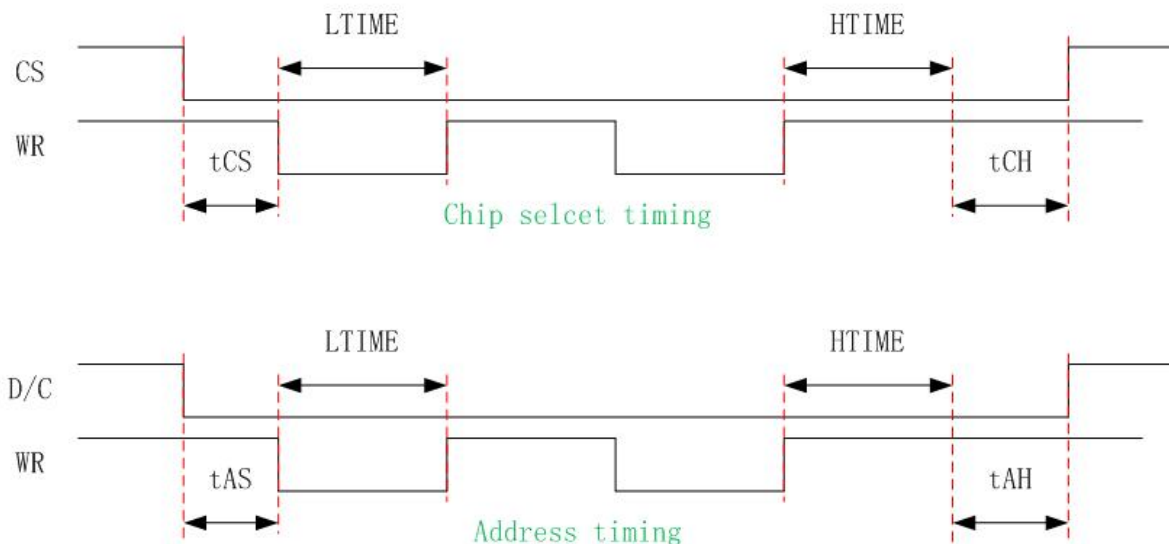


Table 8-6 describes the timing parameters of the LCDC interface.

Table 8-6 Timing parameters of the LCDC interface

Parameter	Symbol	MIN	TYPE	MAX	Unit
Chip select set up time(write)	TCS	15	N/A	N/A	ns

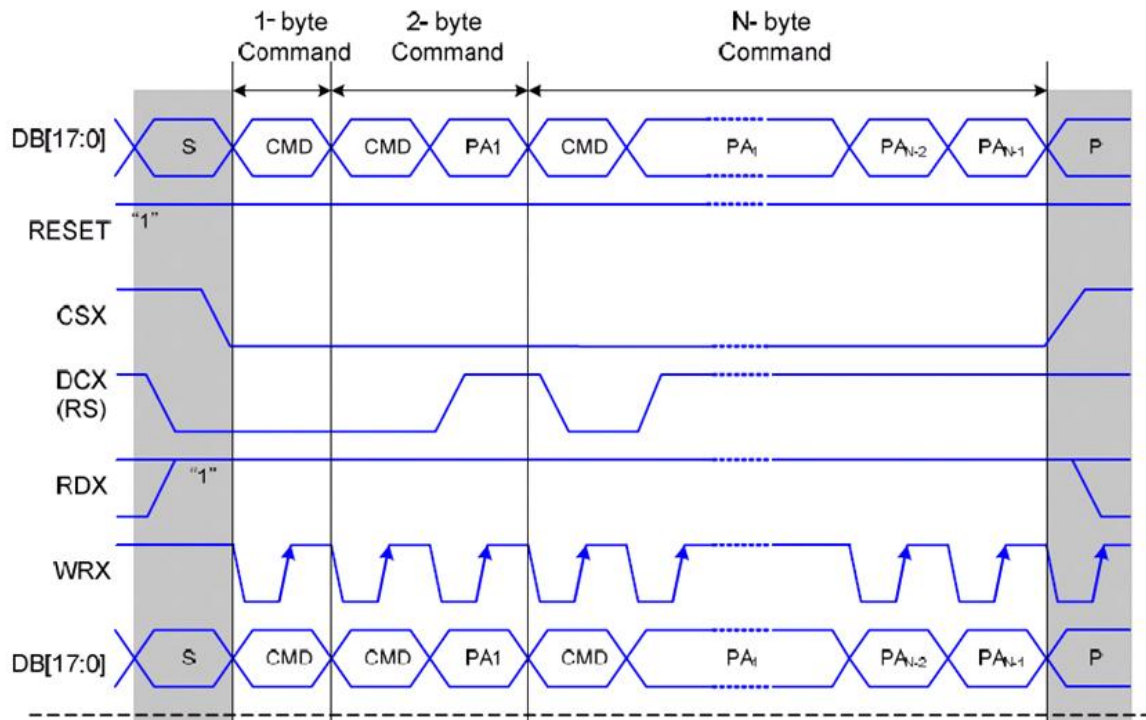
Parameter	Symbol	MIN	TYPE	MAX	Unit
Chip select hold time(write)	TCH	10	N/A	N/A	ns
Address set up time(write)	TAS	0	N/A	N/A	ns
Address hold time(write)	TAH	10	N/A	N/A	ns


NOTE

For details about how to set parameters, see the SLCD_TIMING register section.

Figure 8-13 shows the timing of the SLCD write.

Figure 8-13 The timing of the SLCD write



8.6 I2S Interface Timing

Figure 8-14 shows the RX timing of the I2S interface.

Figure 8-14 RX timing of the I2S interface

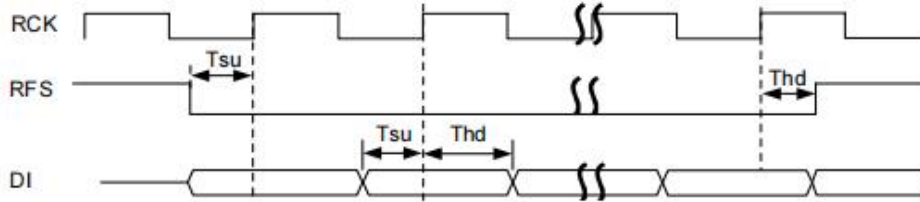


Figure 8-15 shows the TX timing of the I2S interface.

Figure 8-15 TX timing of the I2S interface

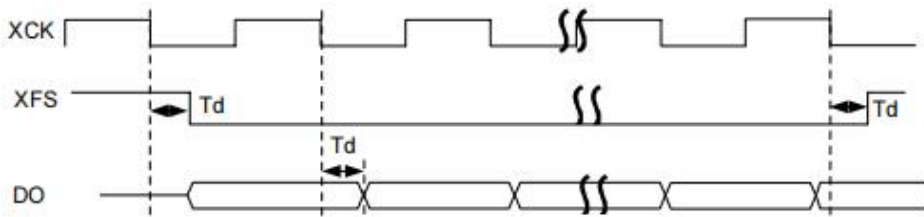


Table 8-7 describes the timing parameters of the I2S interface.

Table 8-7 Timing parameters of the I2S interface

Parameter	Symbol	Min	Typ	Max	Unit
Input signal setup time	T_{su}	10	N/A	N/A	ns
Input signal hold time	T_{hd}	10	N/A	N/A	ns
Output signal delay	T_d	0	N/A	8	ns

8.7 SMB Interface Timing

Figure 8-16 shows the SMB transfer timing.

Figure 8-16 SMB transfer timing

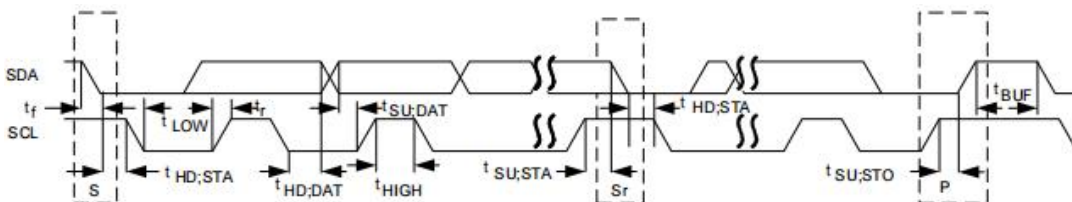


Table 8-8 describes the timing parameters of the SMB interface.

Table 8-8 Timing parameters of the SMB interface

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
Serial clock (SCL) frequency	f_{SCL}	0	100	0	400	kHz

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
Start hold time	$t_{HD;STA}$	4.0	N/A	0.6	N/A	μs
SCL low-level cycle	t_{LOW}	4.7	N/A	1.3	N/A	μs
SCL high-level cycle	t_{HIGH}	4.0	N/A	0.6	N/A	μs
Start setup time	$t_{SU;STA}$	4.7	N/A	0.6	N/A	μs
Data hold time	$t_{HD;DAT}$	0	3.45	0	0.9	μs
Data setup time	$t_{SU;DAT}$	250	N/A	100	N/A	ns
Serial data (SDA) and SCL rising time	t_r	N/A	1000	$20 + 0.1 \times C_b$	300	ns
SDA and SCL falling time	t_f	N/A	300	$20 + 0.1 \times C_b$	300	ns
End setup time	$t_{SU;STO}$	4.0	N/A	0.6	N/A	μs
Bus release time from start to end	t_{BUF}	4.7	N/A	1.3	N/A	μs
Bus load	C_b	N/A	400	N/A	400	pF
Low-level noise tolerance	V_{nL}	$0.1 \times V_{DD}$	N/A	$0.1 \times V_{DD}$	N/A	V
High-level noise tolerance	V_{nH}	$0.2 \times V_{DD}$	N/A	$0.2 \times V_{DD}$	N/A	V

8.8 SSI Timings

Figure 8-17 shows the SSI timing.

Figure 8-17 SSI timing

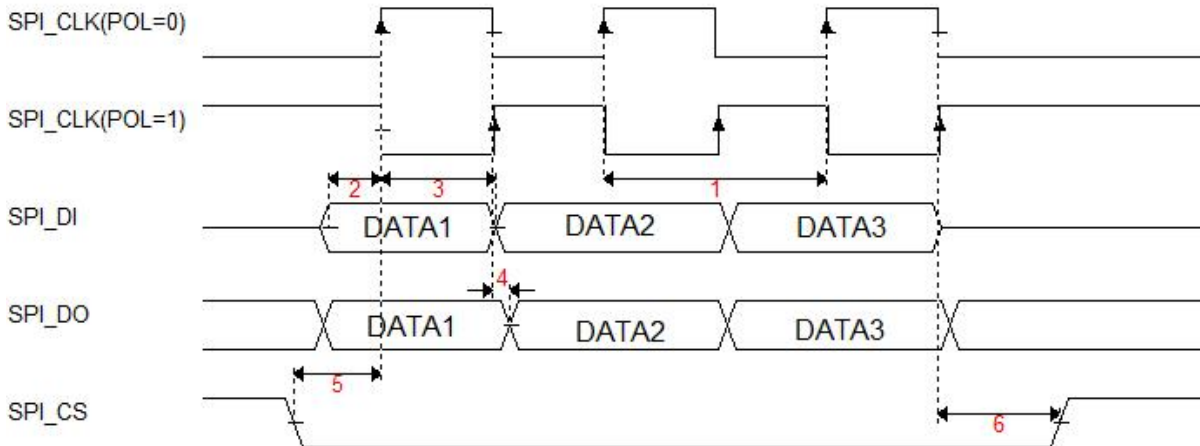


Table 8-9 describes the SSI timing parameters.

Table 8-9 SSI timing parameters

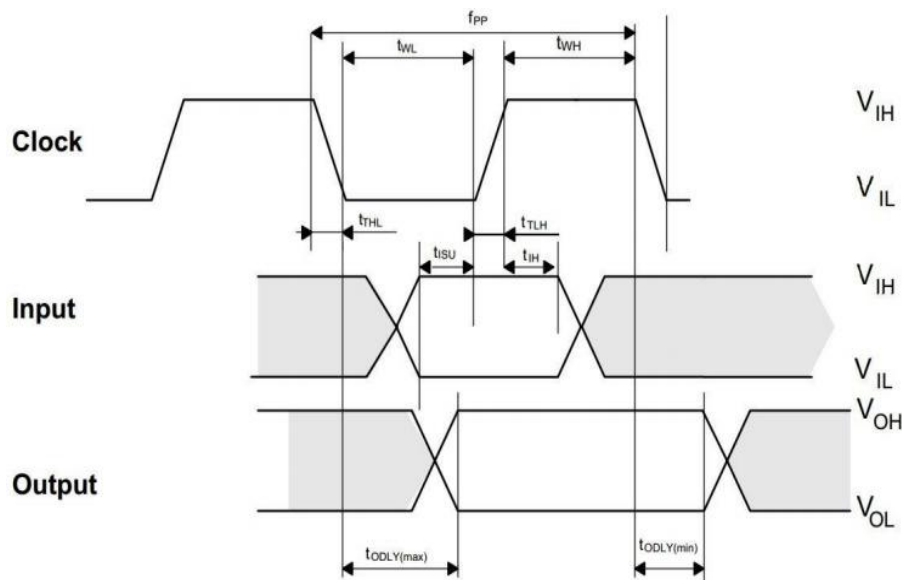
Parameter	Symbol	MIN	TYPE	MAX	Unit	Remark
Cycle time SPI_CLK	T_c	$DEV_CLK/256$	N/A	$DEV_CLK/2$	ns	Depends on Ctrl-register

Parameter	Symbol	MIN	TYPE	MAX	Unit	Remark
Setup time SPI_DI	Tsu	N/A	1/2 Tc	N/A	ns	
Hold time SPI_DI	Th	N/A	1/2 Tc	N/A	ns	
Delay time SPI_DO	Td	0.1	N/A	0.7	ns	
Delay time SPI_CLK valid	Tb	1/2 Tc	N/A	4 Tc	ns	Depends on Ctrl-register
Delay time SPI_CS invalid	Te	1/2 Tc	N/A	4 Tc	ns	Depends on Ctrl-register

8.9 SDIO/MMC(MSC) Interface Timings

Figure 8-18 shows the default-speed timings of the SD/MMC interface.

Figure 8-18 The default-speed timings of the SD/MMC interface



Speed Mode	Maximum Frequency (MHz)/Cycle (ns)		Minimum Input Hold Time	Minimum Input Setup Time	Maximum Output Delay of the Card
Backward legacy MMC card	26 MHz	38.5 ns	3ns	3ns	11.7ns
SD_SDR12	25 MHz	40 ns	5.0ns	5.0 ns	14 ns
Identificatio mode	400 kHz	2.5 μ s	5.0ns	5.0 ns	50ns

Figure 8-19 shows the high-speed timings of the SD/MMC interface.

Figure 8-19 High-speed timings of the SD/MMC interface

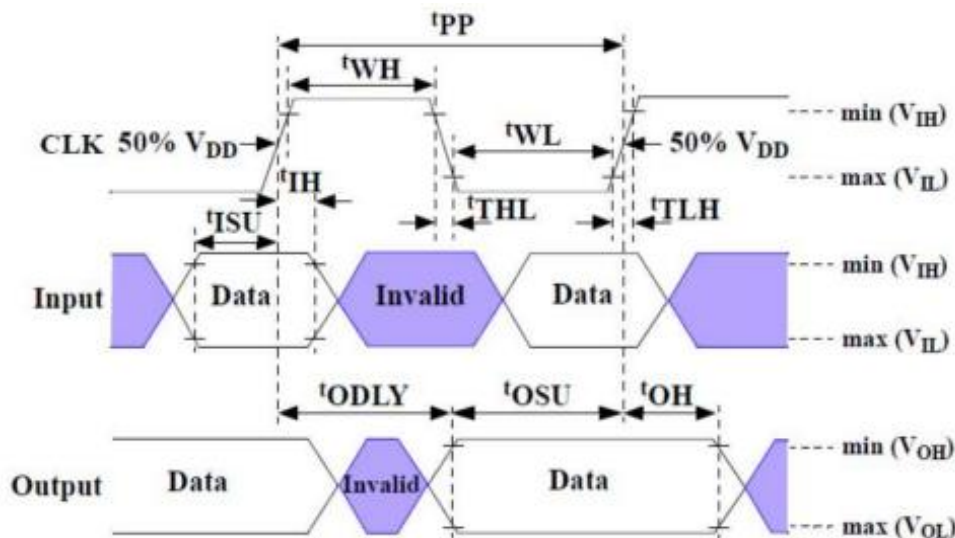


Table 8-10 describes the high-speed mode timing parameters of the SD/MMC interface.

Table 8-10 Timing parameters of the SD/MMC interface

Speed Mode	Maximum Frequency		Minimum Hold Time	Minimum Setup Time	Maximum Output Delay of the Card
	(MHz)	(ns)			
MMC_HS	50MHz	20 ns	3.0 ns	3.0 ns	13.7 ns
SD_SDR25	50MHz	20 ns	2.0 ns	6.0ns	14 ns
SD_HS	50 MHz	20 ns	2.0 ns	6.0 ns	14 ns
Identification mode	400 kHz	2.5 μ s	5.0ns	5.0 ns	50ns

8.10 DMIC Timings

Figure 8-20 show the timing relationship for the DMIC transfers. The DMIC_CLK is generated from DMIC Controller to Sensor(Digital Microphone sensor). DMIC Controller samples the data Pins use the different edge to two channels. DMIC Controller can sample two pins and 4 channels data from data pin. In other word, one pin can connect two Sensor, one Sensor data sample at rising edge and another Sensor data sample at falling edge.

Figure 8-20 The DMIC signal Timing

