Model Name: T430QVN01.0

Issue Date: 2014/09/01

(*) Preliminary Specifications
( ) Final Specifications

Customer Signature	Date	AUO	Date
Approved By		Approval By PM Director	
Note		Reviewed By RD Director	
		Reviewed Bv Proiect Leader	
		Prepared By PM	

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0.0	2014/08/22	---	First release
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1. General Description

This specification applies to the 43 inch Color TFT-LCD SKD model T430QVN01.0. This Open Cell Unit has a TFT active matrix type liquid crystal panel 3,840x2,160 pixels, and diagonal size of 43 inch. This Open Cell Unit supports 3,840x2,160 mode. Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 10-bit (8bit+FRC) gray scale signal for each dot.

*** General Information**

Items	Specification	Unit	Note
Active Screen Size	43	Inch	
Display Area	941.184 (H) x 529.416 (V)	mm	
Outline Dimension	953 (H) x 543 (V)	mm	
Cell Dimension	953 (H) x 543 (V) x 1.34(D)	mm	D: cell thickness
Driver Element	a-Si TFT active matrix		
Bezel Opening	---	mm	Customer Design
Display Colors	10 bit (8bit+FRC)	Colors	
Number of Pixels	3,840 x 2,160	Pixel	
Pixel Pitch	0.49005 (H) x 0.49005(W)	mm	
Pixel Arrangement	RGB vertical stripe		
Display Operation Mode	Normally Black		
Surface Treatment	Anti-Glare, 3H		Haze=2%
Weight	1500	g	
Rotate Function	Unachievable		Note 1
Display Orientation	Signal input with “ABC”		Note 2

Note 1: Rotate Function refers to LCD display could be able to rotate.

Note 2: LCD display as below illustrated when signal input with “ABC”.

2. Absolute Maximum Ratings

The followings are maximum values which, if exceeded, may cause faulty operation or damage to the unit

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	V_{DD}	-0.3	14	$[Volt]_{DC}$	Note 1
Input Voltage of Signal	Vin	-0.3	4	$[Volt]_{DC}$	Note 1
Operating Temperature	TOP	0	+50	[°C]	Note 2
Operating Humidity	HOP	10	90	[%RH]	Note 2
Storage Temperature	TST	-20	+60	[°C]	Note 2
Storage Humidity	HST	10	90	[%RH]	Note 2
Panel Surface Temperature	PST		65	[°C]	Note 3
Electro Statistic Voltage	ESD		±2	[KV]	Note 4

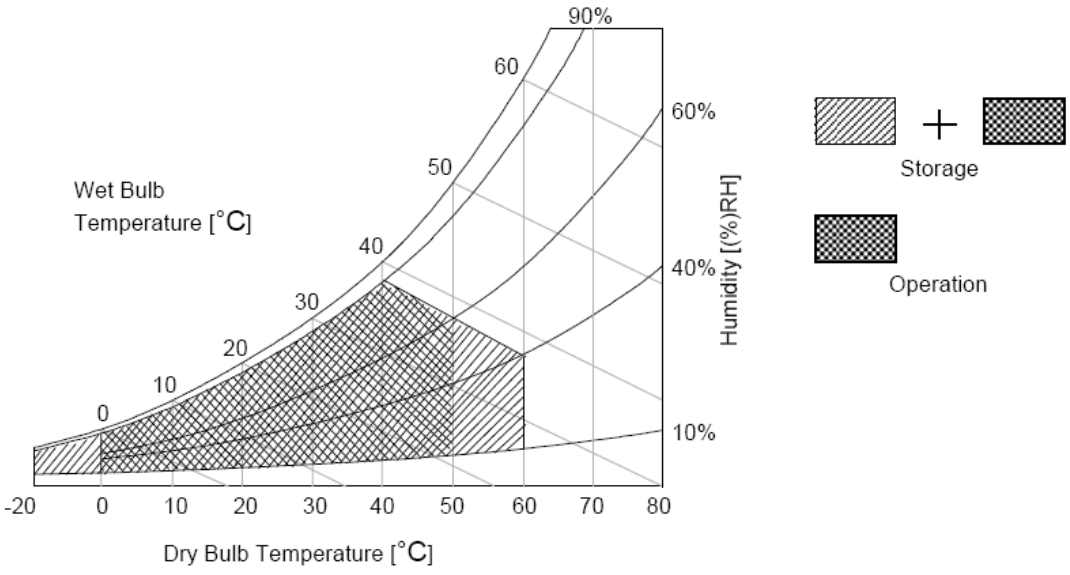
Note 1: Duration-50 msec.

Note 2: Maximum Wet-Bulb should be 39℃ and No condensation.

The relative humidity must not exceed 90% non-condensing at temperatures of 40℃ or less. At temperatures greater than 40℃, the wet bulb temperature must not exceed 39℃.

Note 3: Surface temperature is measured at 50℃ Dry condition

Note 4: ESD protection procedure must be applied during production process; especially polarizer protection films remove process. Please directly contact AUO if module process advice is required.



3. Electrical Specification

The T430QVN01.0 Open Cell Unit requires power input which is employed to power the LCD electronics and to drive the TFT array and liquid crystal.

3.1 Electrical Characteristics

3.1.1 DC Characteristics

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max		
LCD							
Power Supply Input Voltage		V_{DD}	10.8	12	13.2	V_{DC}	
Power Supply Input Current		I_{DD}	--	0.85	1.9	A	1
Power Consumption		P_C	--	10.2	22.8	Watt	1
Inrush Current		I_{RUSH}	--	--	5	A	2
Permissible Ripple of Power Supply Input Voltage		V_{RP}	--	--	V_{DD} * 5%	mV_{pk-pk}	3
CMOS Interface	Input High Threshold Voltage	V_{IH} (High)	2.7	--	3.3	V_{DC}	4
	Input Low Threshold Voltage	V_{IL} (Low)	0	--	0.6	V_{DC}	4
V-by-one Interface	CML Differential Input High Threshold	V_{RTH}	+50	--	--	mV_{DC}	
	CML Differential Input Low Threshold	V_{RTL}	--	--	-50	mV_{DC}	
	CML Common mode Bias Voltage	V_{RCT}	0.8	0.9	1.0	mV_{DC}	

3.1.2 AC Characteristics

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max		
V-by-one Interface	VRXINP/N input each bit Period	T_{RRIP} (UI)	310	--	379	ps	5
	Receiver Clock : Spread Spectrum Modulation range	Fclk_ss	Fclk -0.5%	--	Fclk +0.5%	MHz	8
	Receiver Clock : Spread Spectrum Modulation frequency	Fss		30		KHz	8
	ALN Training	T_{RALN}	--	40960	--	UI	5
	PDX active to hot plug enable	T_{RHPD0}	--	--	1.0	us	5
	Intra-pair skew	T_{INTRA}	--	--	0.3	UI	6
	Inter-pair skew	T_{INTER}	--	--	5	UI	7
	Eye diagram at receiver	A_X	--	0.25	--	UI	8
		A_Y	--	0	--	mV	
		B_X	--	0.3	--	UI	
		B_Y	--	50	--	mV	
		C_X	--	0.7	--	UI	
		C_Y	--	50	--	mV	
		D_X	--	0.75	--	UI	
		D_Y	--	0	--	mV	
		E_X	--	0.7	--	UI	
		E_Y	--	-50	--	mV	
		F_X	--	0.3	--	UI	
		F_Y	--	-50	--	mV	
I2C Interface1	SCL clock frequency	fSCL	-	-	400	kHz	9
	Clock Pulse Width Low	tLOW	1.3	-	-	us	
	Clock Pulse Width High	tHIGH	0.6	-	-	us	
	Clock Low to Data Output Valid	tAA	1.1	-	-	us	
	Start Setup Time	tSTASU	0.6	-	-	us	
	Start Hold Time	tSTAHD	0.6	-	-	us	
	Stop Setup Time	tSTOSU	0.6	-	-	us	
	Data In Setup Time	tDSU	0.2	-	-	us	
	Data In Hold Time	tDHD	0	-	-	us	
	SCL/SDA Rise Time	tR	-	-	0.3	us	
	SCL/SDA Fall Time	tF	-	-	0.3	us	

3.1.3 DRIVER CHARACTERISTICS

Item	Symbol	Min	Max	Unit	condition
Driver Surface Temperature	DST		100	[℃]	Note

Note : Any point on the driver surface must be less than 100℃ under any conditions.

3.1.4 TCON Characteristics

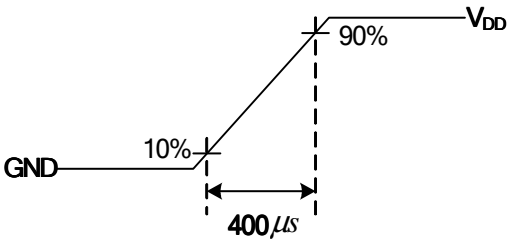
Item	Symbol	Min	Max	Unit	condition
TCON Surface Temperature	TST		85	[℃]	Note

Note : Any point on the TCON surface must be less than 85℃ under any conditions.

Note :

1. Test Condition:
   (1) V_{DD} = 12.0V
   (2) Frame rate = 60Hz
   (3) Fclk= Max freq.
   (4) Temperature = 25 ℃
   (5) Typ. Input current : White Pattern
   Max. Input current: Heavy loading pattern defined by AUO

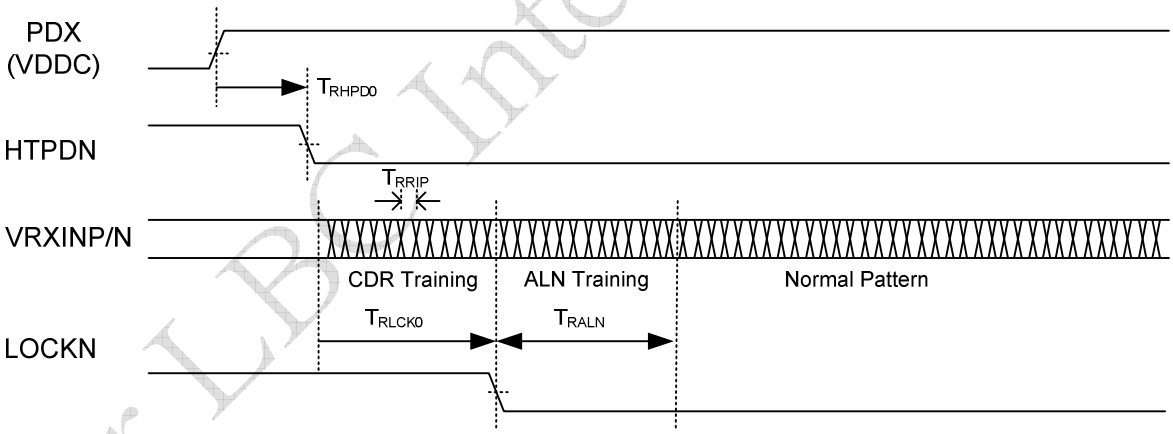
2. Measurement condition : Rising time = 400us



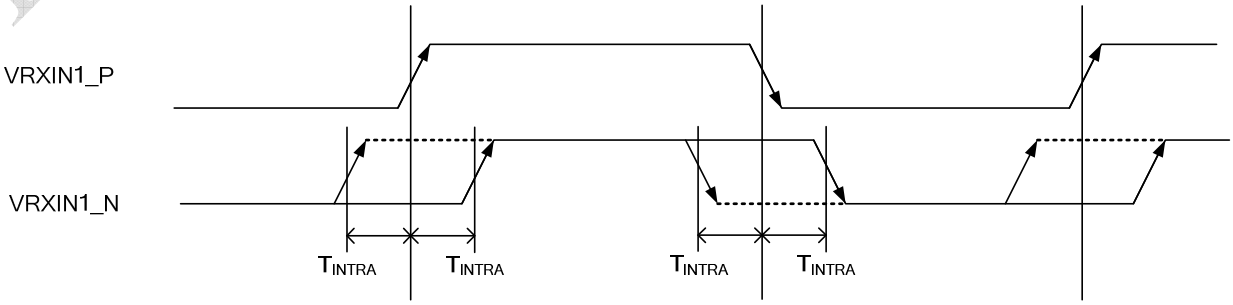
3. Test Condition:
   (1) The measure point of V_{RP} is in LCM side after connecting the System Board and LCM.
   (2) Under Max. Input current spec. condition.

4. The measure points of V_{IH} and V_{IL} are in LCM side after connecting the System Board and LCM.

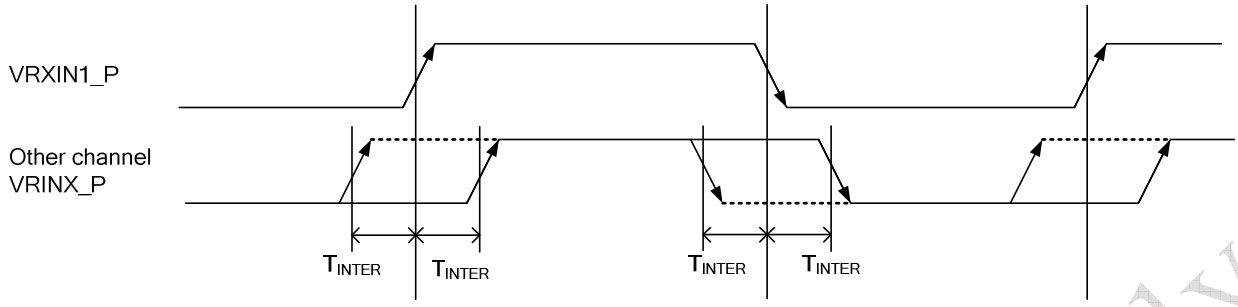
5. V-by-one Receiver start up timing waveform



6. V-by-one Intra-pair Skew

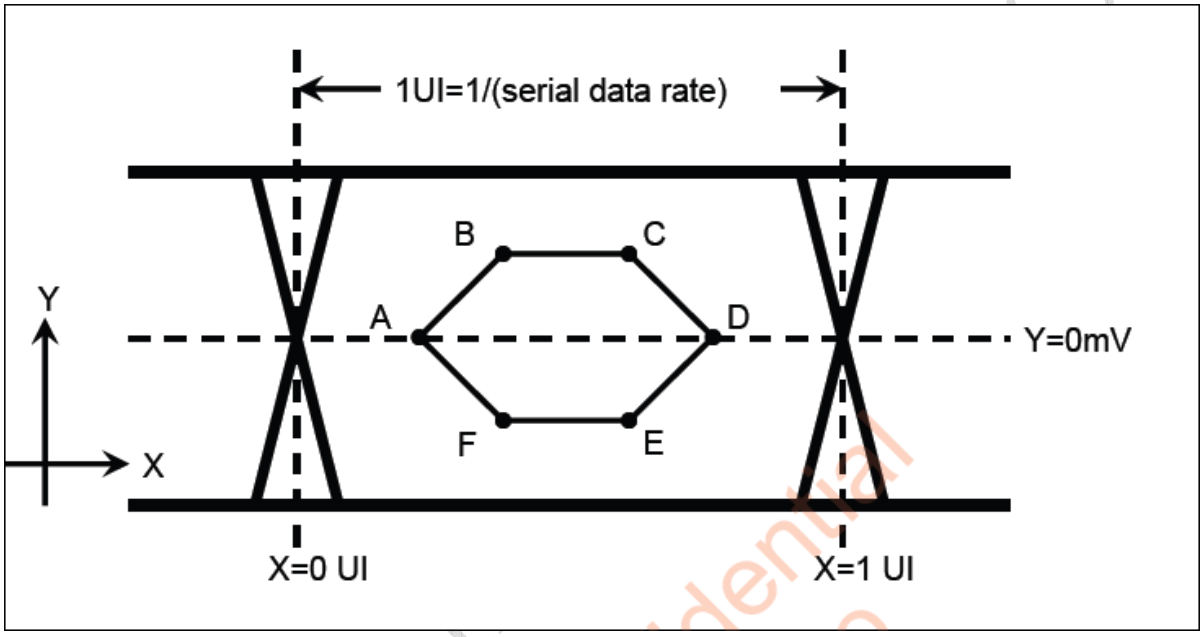


7. V-by-one Inter-pair Skew

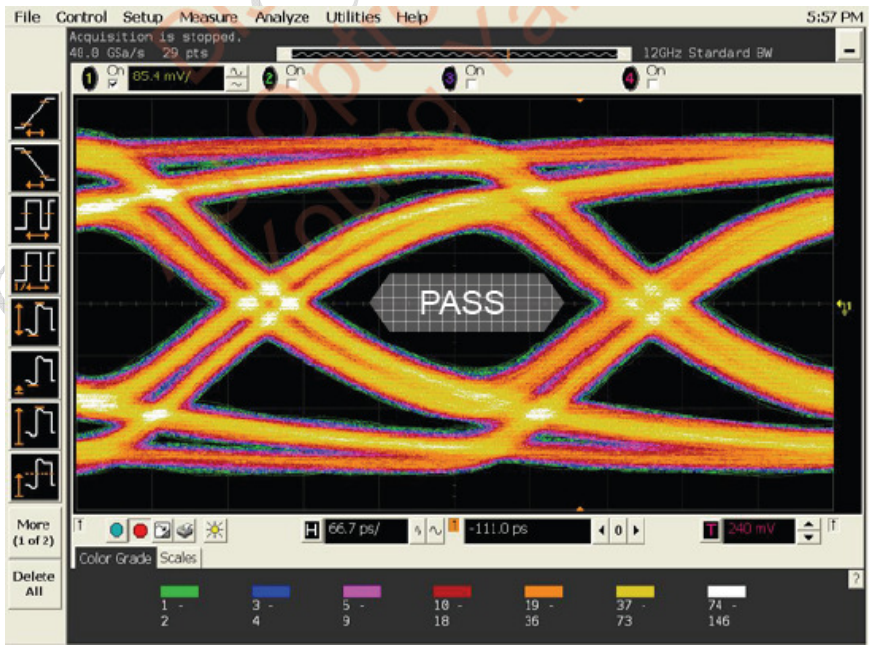


8. Eye diagram at receiver

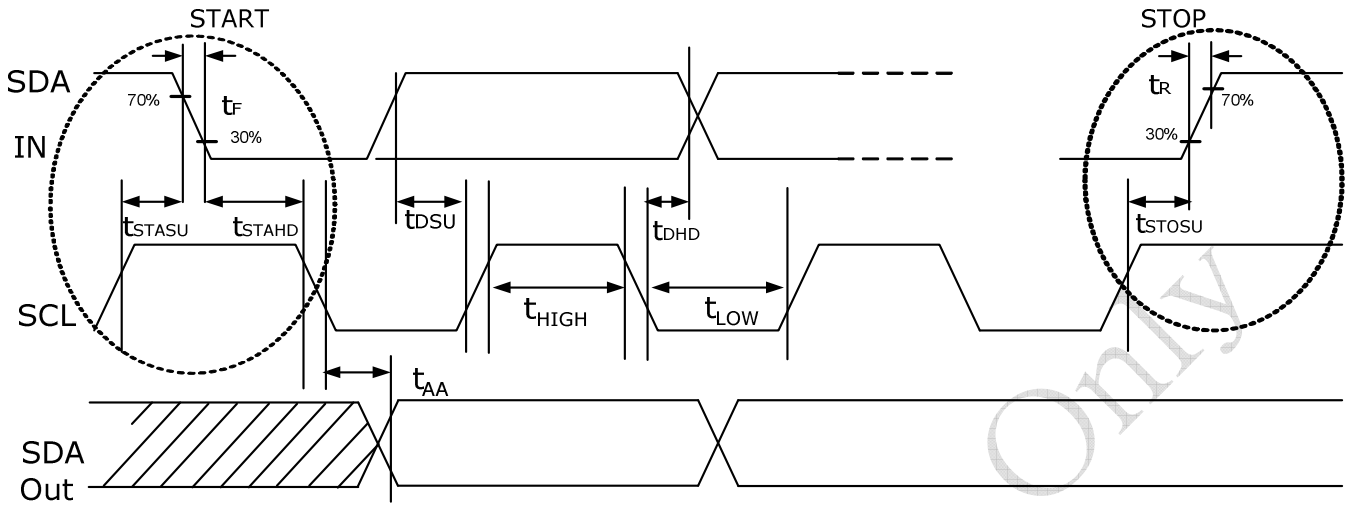
Eye Mask



Example of Eye diagram



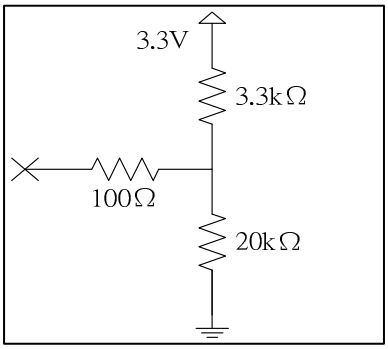
9. I2C Read/Write Timing



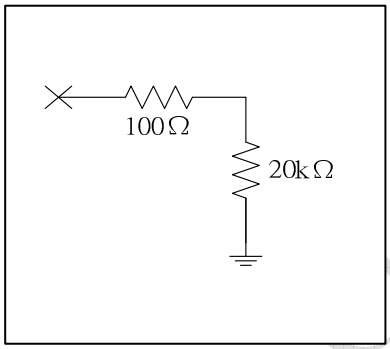
3.2 Interface Connections

3.2.1 connector control and I2C pin description

Note * : Open/High(3.3V)

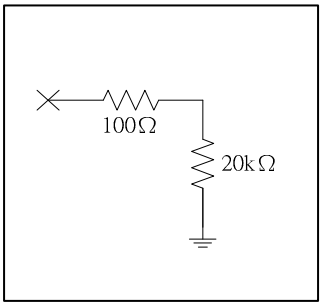


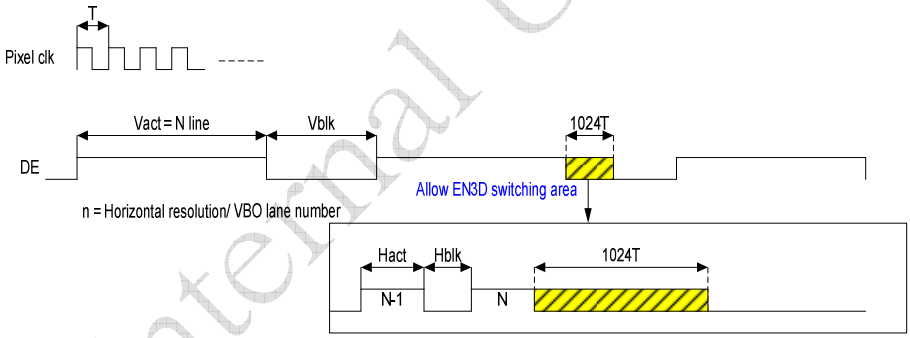
Note ** : Open/Low(GND)



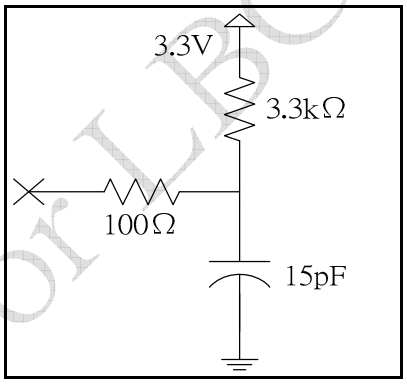
Note * : Open/Low(GND)**

The switch range of 3D_EN control signal is from the last DE falling to 1024T. (T is a pixel clk)

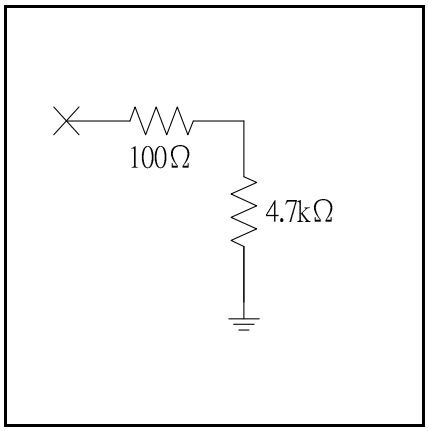




Note ** : SCL/SDA**



Note *** : WP**



3.2.2 T-Con Board Pin Map

- LCD connector: JAE FI-RTE51SZ-HF
- Mating connector:

PIN	Symbol	Description	PIN	Symbol	Description
1	VIN	12V	26	LOCKN	Vx1 LOCK
2	VIN	12V	27	GND	Ground
3	VIN	12V	28	RX0N	Vx1 lane 0
4	VIN	12V	29	RX0P	Vx1 lane 0
5	VIN	12V	30	GND	Ground
6	VIN	12V	31	RX1N	Vx1 lane 1
7	VIN	12V	32	Rx1P	Vx1 lane 1
8	VIN	12V	33	GND	Ground
9	N.C.	No connection (for AUO test only. Do not connect)	34	RX2N	Vx1 lane 2
10	GND	Ground	35	RX2P	Vx1 lane2
11	GND	Ground	36	GND	Ground
12	GND	Ground	37	RX3N	Vx1 lane 3
13	GND	Ground	38	RX3P	Vx1 lane 3
14	GND	Ground	39	GND	Ground
15	3D_Sync_out	3D_Sync_out	40	RX4N	Vx1 lane 4
16	3D_Sync_In	3D_Sync_In	41	RX4P	Vx1 lane 4
17	3D_EN	3D Function Enable High(3.3V) : 3D Open/Low(GND) : 2D	42	GND	Ground
18	SDA	I2C SDA	43	RX5N	Vx1 lane 5
19	SCL	I2C SCL	44	RX5P	Vx1 lane 5
20	WP	EEPROM Write Protection High(3.3V) for Writable, Low(GND) for protection	45	GND	Ground
21	N.C.	No connection (for AUO test only. Do not connect)	46	RX6N	Vx1 lane 6
22	N.C.	No connection (for AUO test only. Do not connect)	47	RX6P	Vx1 lane 6
23	N.C.	No connection (for AUO test only. Do not connect)	48	GND	Ground
24	GND	Ground	49	RX7N	Vx1 lane 7
25	HTPDN	Vx1 HTPDN	50	RX7P	Vx1 lane 7
			51	GND	Ground

Note: N.C.: please leave this pin unoccupied. It can not be connected by any signal (Low/GND/High).
Note: Open / High (3.3V) / Low (GND)/ WP / SDA / SCL described in 3.1.2

3.2.4: V by one color data mapping

Mode		Packer input & Unpacker output		30bpp RGB /YCbCr444 (10bit)
4byte mode	3byte mode	Byte0	D[0]	R/Cr[2]
			D[1]	R/Cr[3]
			D[2]	R/Cr[4]
			D[3]	R/Cr[5]
			D[4]	R/Cr[6]
			D[5]	R/Cr[7]
			D[6]	R/Cr[8]
			D[7]	R/Cr[9]
		Byte1	D[8]	G/Y[2]
			D[9]	G/Y[3]
			D[10]	G/Y[4]
			D[11]	G/Y[5]
			D[12]	G/Y[6]
			D[13]	G/Y[7]
			D[14]	G/Y[8]
			D[15]	G/Y[9]
		Byte2	D[16]	B/Cb[2]
			D[17]	B/Cb[3]
			D[18]	B/Cb[4]
			D[19]	B/Cb[5]
			D[20]	B/Cb[6]
			D[21]	B/Cb[7]
			D[22]	B/Cb[8]
			D[23]	B/Cb[9]
		Byte3	D[24]	--
			D[25]	--
			D[26]	B/Cb[0]
			D[27]	B/Cb[1]
			D[28]	G/Y[0]

		D[29]	G/Y[1]
		D[30]	R/Cr[0]
		D[31]	R/Cr[1]

3.3 Signal Timing Specification

This is the signal timing required at the input of the user connector. All of the interface signal timing should be satisfied with the following specifications for its proper operation.

Timing Table (DE only Mode)

Signal	Item	Symbol	Min.	Typ.	Max	Unit
Vertical Section	Period	Tv	2200	2250	2715	Th
	Active	Tdisp (v)		2160		
	Blanking	Tblk (v)	40	90	555	Th
Horizontal Section	Period	Th	530	550	600	Tclk
	Active	Tdisp (h)		480		
	Blanking	Tblk (h)	50	70	120	Tclk
Clock	Frequency	Fclk=1/Tclk	66	74.25	77	MHz
Vertical Frequency	Frequency	Fv	47	60	63	Hz
Horizontal Frequency	Frequency	Fh	120	135	139.2	KHz

For 3D application (4K1K_120Hz)

Signal	Item	Symbol	Min.	Typ.	Max	Unit
Vertical Section	Period	Tv	1120	1125	1356	Th
	Active	Tdisp (v)		1080		
	Blanking	Tblk (v)	40	45	276	Th
Horizontal Section	Period	Th	530	550	600	Tclk
	Active	Tdisp (h)		480		
	Blanking	Tblk (h)	50	70	120	Tclk
Clock	Frequency	Fclk=1/Tclk	66	74.25	77	MHz
Vertical Frequency	Frequency	Fv	94	120	122	Hz
Horizontal Frequency	Frequency	Fh	120	135	139.2	KHz

Notes:

(1) Display position is specific by the rise of DE signal only.
Horizontal display position is specified by the rising edge of 1st DCLK after the rise of 1st DE, is displayed on the left edge of the screen.

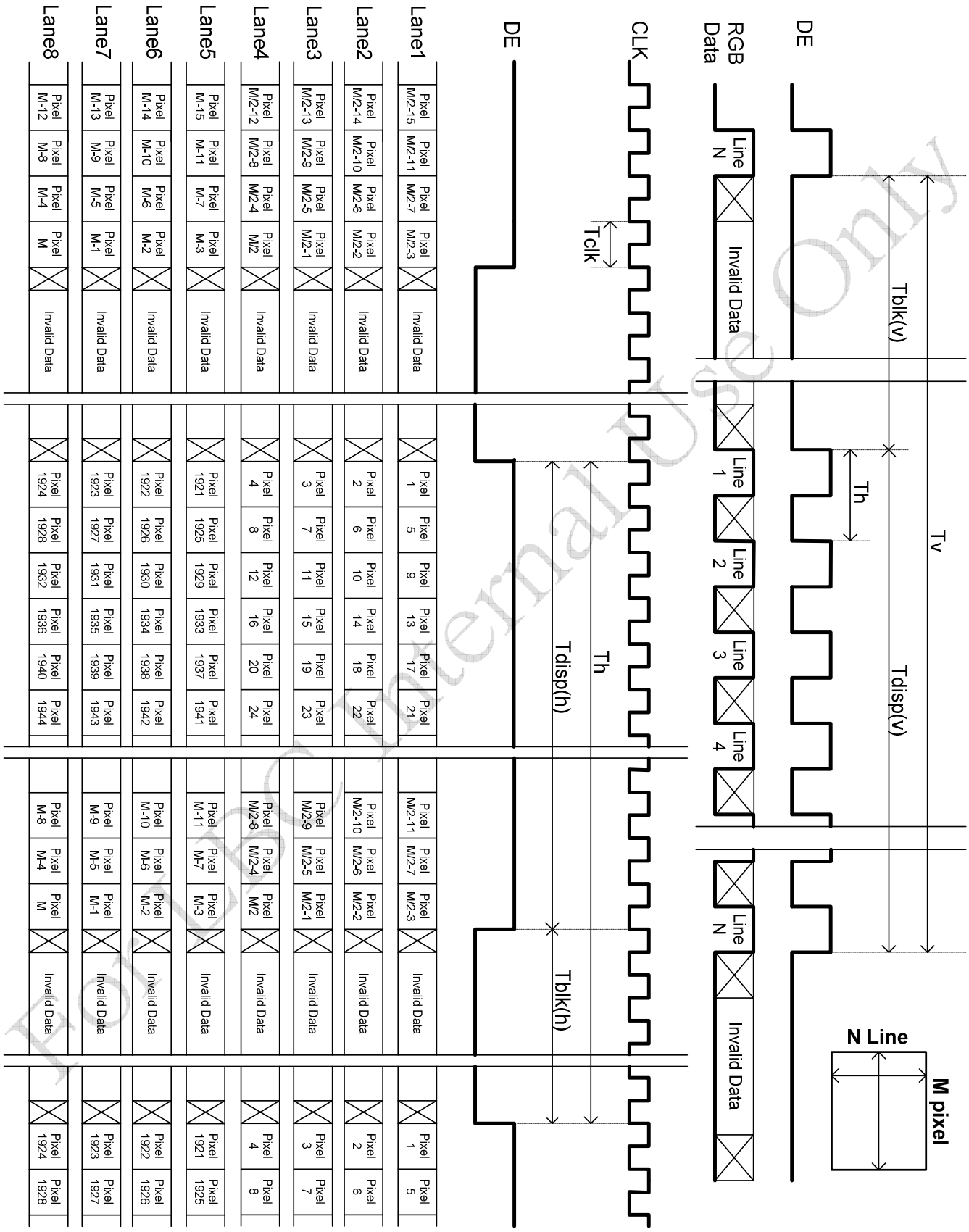
(2) Vertical display position is specified by the rise of DE after a “Low” level period equivalent to eight times of horizontal period. The 1st data corresponding to one horizontal line after the rise of 1st DE is displayed at the top line of screen.

(3) If a period of DE “High” is less than 3840 DCLK or less than 2160 lines, the rest of the screen displays black.

(4) The display position does not fit to the screen if a period of DE “High” and the effective data period do not synchronize with each other.

3.4 Signal Timing Waveforms

TWO Section Mode (Lane1~8 V-by one data:1, 2, 3, 4, 1921, 1922, 1923, 1924)



3.5 Color Input Data Reference

The brightness of each primary color (red, green, blue) is based on the 10 bit (8 bit+FRC) gray scale data input for the color; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

COLOR DATA REFERENCE

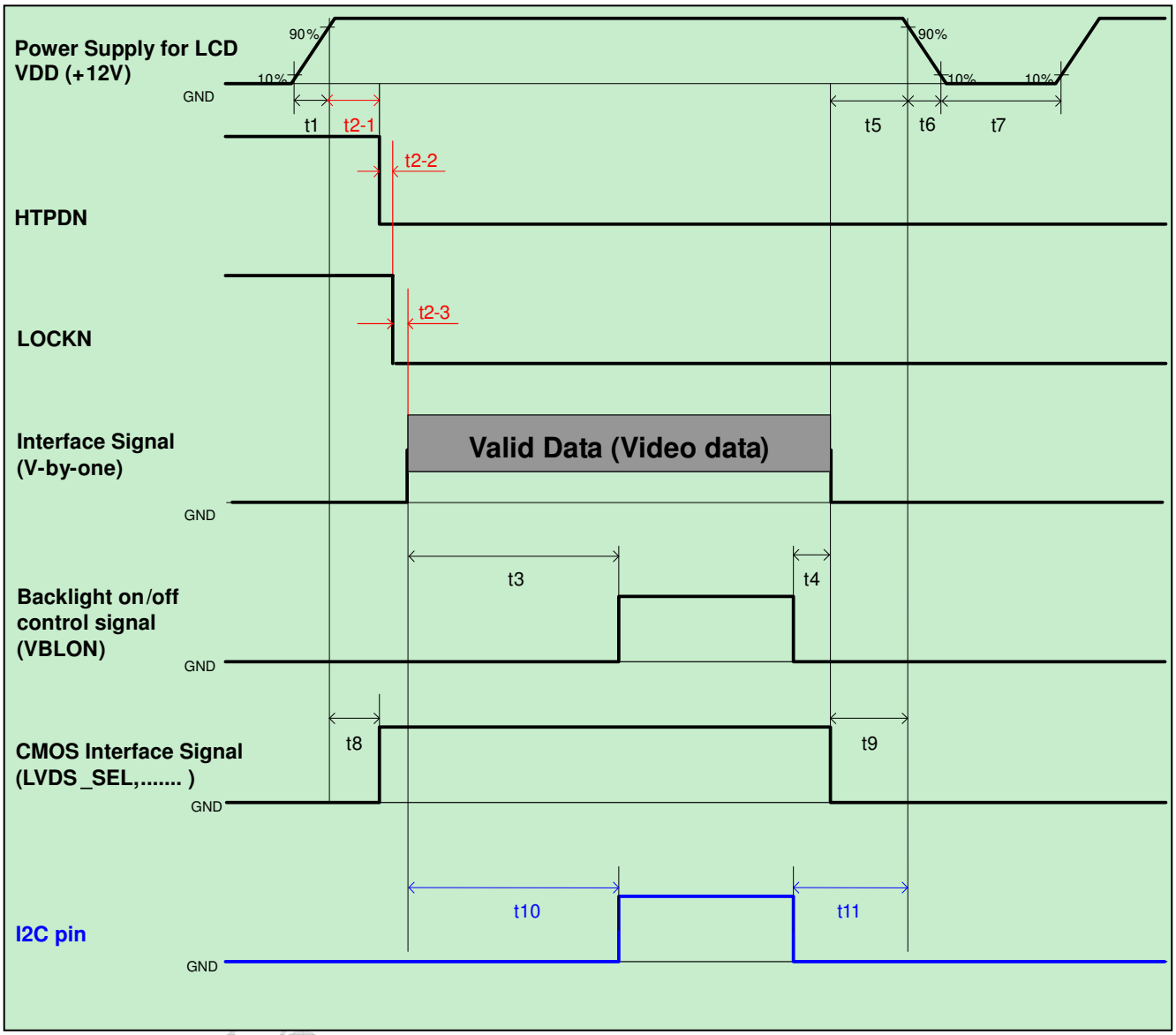
Color		Input Color Data																													
		RED										GREEN										BLUE									
		MSB									LSB	MSB									LSB	MSB									LSB
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue(1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R	RED(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(001)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	RED(1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
G	GREEN(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

	GREEN(1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	GREEN(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
B	BLUE(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

	BLUE(1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	BLUE(1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

3.6 Power Sequence for LCD



Parameter	Values			Unit
	Min.	Type.	Max.	
t1	0.4	---	30	ms
t2-1	10	---	---*1	ms
t2-2	---	---	---*2	ms
t2-3	---	---	1	ms
t3	640	---	---	ms
t4	0*3	---	---	ms
t5	0	---	---	ms
t6	---	---	---*4	ms
t7	500	---	---	ms
t8	10*5	---	50	ms
t9	0	---	---	ms
t10	640	---	---	ms
t11	150	---	---	ms

Note:

(1) t2-1: The maximum timing of VDD rising(90%) to HTPDN falling edge decided by customer system.

(2) t2-2: V by One training time after power-on. The timing of HTPDN falling edge to LOCKN falling edge decided by customer system.

(3) t4 = 0 : concern for residual pattern before BLU turn off.

(4) t6: voltage of VDD must decay smoothly after power-off. (customer system decide this value)

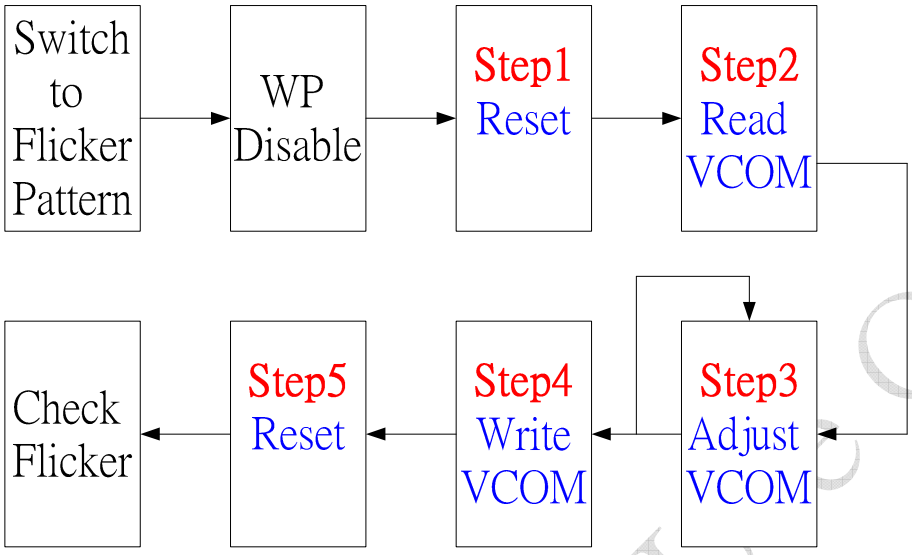
(5) When CMOS Interface signal is N.C. (no connection), opened in Transmitted end, t8 timing spec can be negligible.

(6) t2-1: VDD rising(90%) to HTPDN falling edge
t2-2: CDR lock time (CDR training)
t2-3: ALN training

3.7 VCOM Adjust SOP

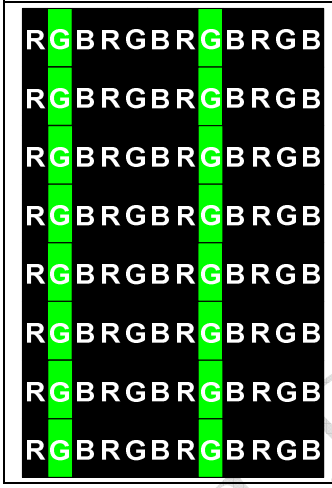
If you need below pattern or more detail information, please directly contact AUO for engineer service.

3.7.1 VCOM I2C Tuning Step



3.7.2 Flicker Pattern

☐ V-stripe
Green (L128)



3.7.3 WP (Write Protect) Disable

		Write Enable	Write Protect
WP Pin	☐	L	H and Open
	■	H	L and Open

3.7.4 Adjust SOP

Step1 Reset

* Device Address is 0x74 (7Bits)

S	Slave Address	W	A	Index Address 0	A	Control Byte	A	P
	1 1 1 0 1 0 0	0		0 0 0 0 0 0 0 0		0 0 0 1 0 0 1 0		
	0xE8			0x00		0x12		
	Device Address + W			Control Address		Reset + OUT_EN		

Step2 Read VCOM

* Data = 7Bits

S	Slave Address	W	A	Index Address 1	A	S	Slave Address	R	A	DATA	NA	P
	1 1 1 0 1 0 0	0		0 0 0 0 0 0 0 1			1 1 1 0 1 0 0	1		X X X X X X X X		
	0xE8			0x01			0xE9			Data		
	Device Address + W			VCOM Address			Device Address + R					

Step3 Adjust VCOM

* DVCOM = 8Bits

S	Slave Address	W	A	Index Address 1	A	DVCOM	A	P
	1 1 1 0 1 0 0	0		0 0 0 0 0 0 0 1		0000000X~1111111X		
	0xE8			0x01		0x00~0xFF		
	Device Address + W			VCOM Address		VCOM value		

Step4 Write VCOM

S	Slave Address	W	A	Index Address 0	A	Control Byte	A	P
	1 1 1 0 1 0 0	0		0 0 0 0 0 0 0 0		0 0 0 0 1 0 1 0		
	0xE8			0x00		0x0A		
	Device Address + W			Control Address		Write DAC to NVM+ OUT_EN		

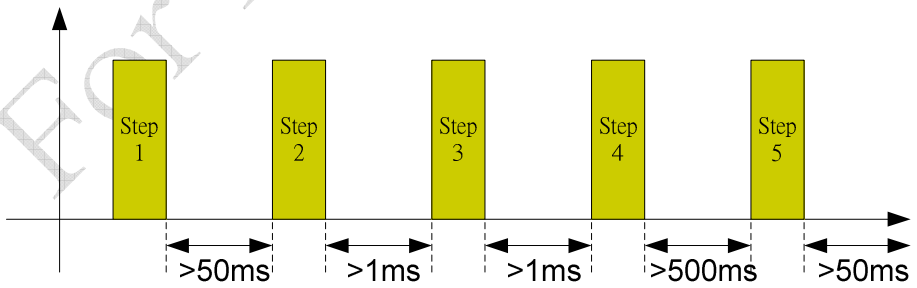
Step5 Reset

* Device Address is 0x74 (7Bits)

S	Slave Address	W	A	Index Address 0	A	Control Byte	A	P
	1 1 1 0 1 0 0	0		0 0 0 0 0 0 0 0		0 0 0 1 0 0 1 0		
	0xE8			0x00		0x12		
	Device Address + W			Control Address		Reset + OUT_EN		

3.7.5 Interval of Step to Step

Step to step interval must follow below figure

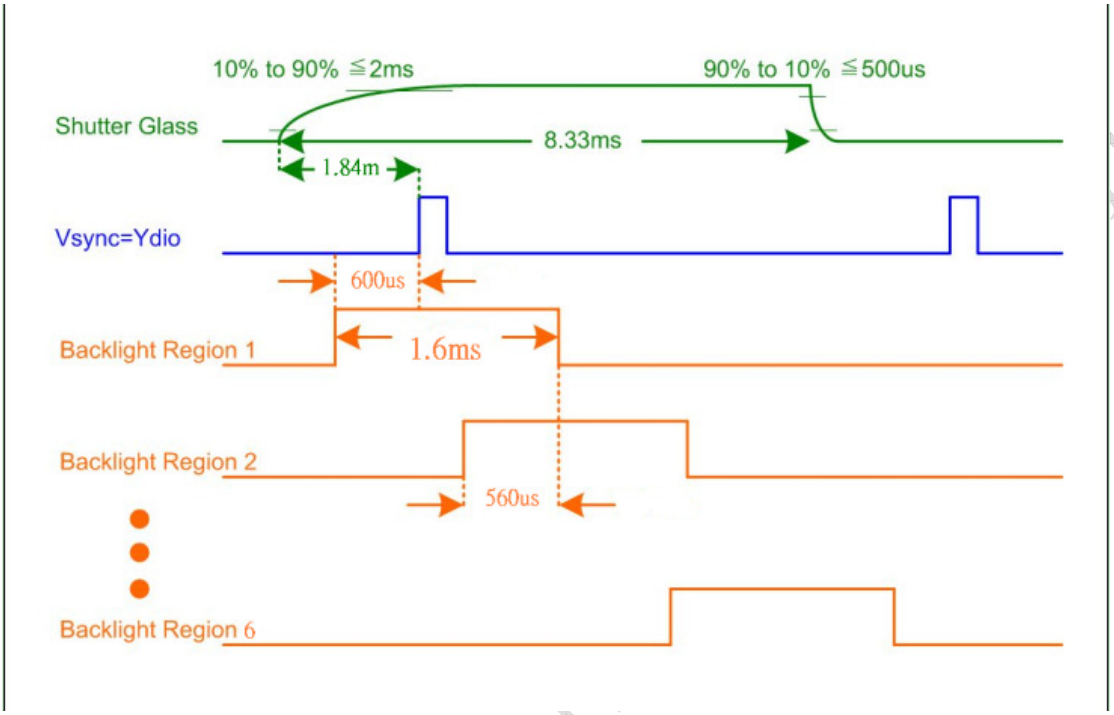


3.8 3D Shutter Glasses Synchronous Timing

Glasses and BL Control Timing

(AUO module setting, for customer reference only)

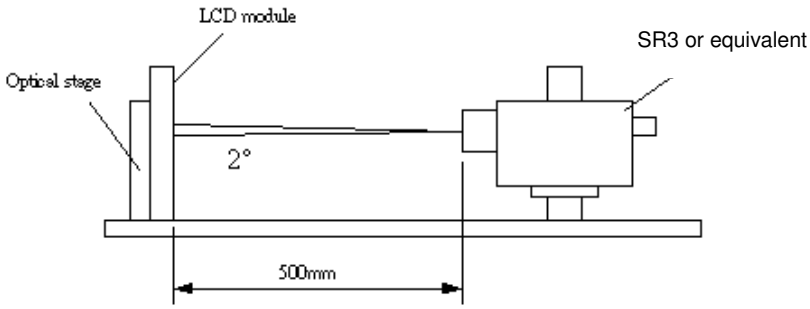
2X6 sections



4. Optical Specification

Optical characteristics are determined after the open cell unit and light source has been 'ON' and stable for approximately 45 minutes in a dark environment at 25℃. The values specified are at an approximate distance 50cm from the LCD surface at a viewing angle of φ and θ equal to 0°.

Fig.1 presents additional information concerning the measurement equipment and method.



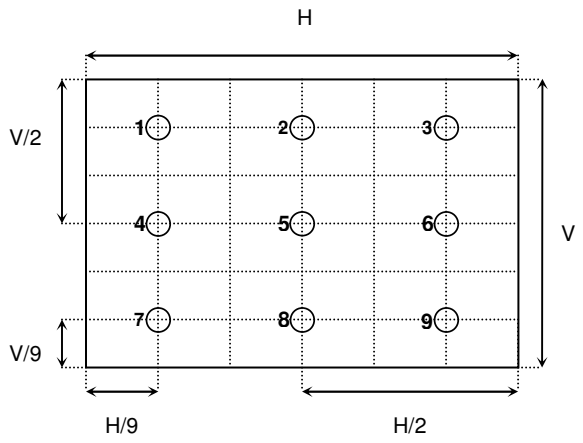
Parameter		Symbol	Condition	Values			Unit	Notes
				Min.	Typ.	Max		
Contrast Ratio		CR	With AUO Module	3200	4000	--		1, 2
White Variation		$\delta_{WHITE(9P)}$		--	--	1.33		1, 3
Response Time (G to G)		T_{γ}		--	6.5	--	ms	4
Center Transmittance		T%			4.5		%	1, 7
Color Chromaticity			With SR3 Standard light source "C"					5
	Red	R_X		Typ.-0.03	0.662	Typ.+0.03		
		R_Y			0.325			
	Green	G_X			0.274			
		G_Y			0.590			
	Blue	B_X			0.138			
		B_Y			0.115			
	White	W_X			0.293			
		W_Y			0.342			
Viewing Angle			With AUO Module					1, 6
	x axis, right(φ=0°)	θ_r		--	89	--	degree	
	x axis, left(φ=180°)	θ_l		--	89	--	degree	
	y axis, up(φ=90°)	θ_u		--	89	--	degree	
	y axis, down (φ=270°)	θ_d		--	89	--	degree	

1. Light source here is the BLU of AUO P420HVN02.0 module.
2. Contrast Ratio (CR) is defined mathematically as:

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance of } L_{on5}}{\text{Surface Luminance of } L_{off5}}$$

3. The white variation, δWHITE is defined as:

$\delta_{WHITE(9P)}$= Maximum(L_{on1}, L_{on2},…,L_{on9})/ Minimum(L_{on1}, L_{on2},…L_{on9})



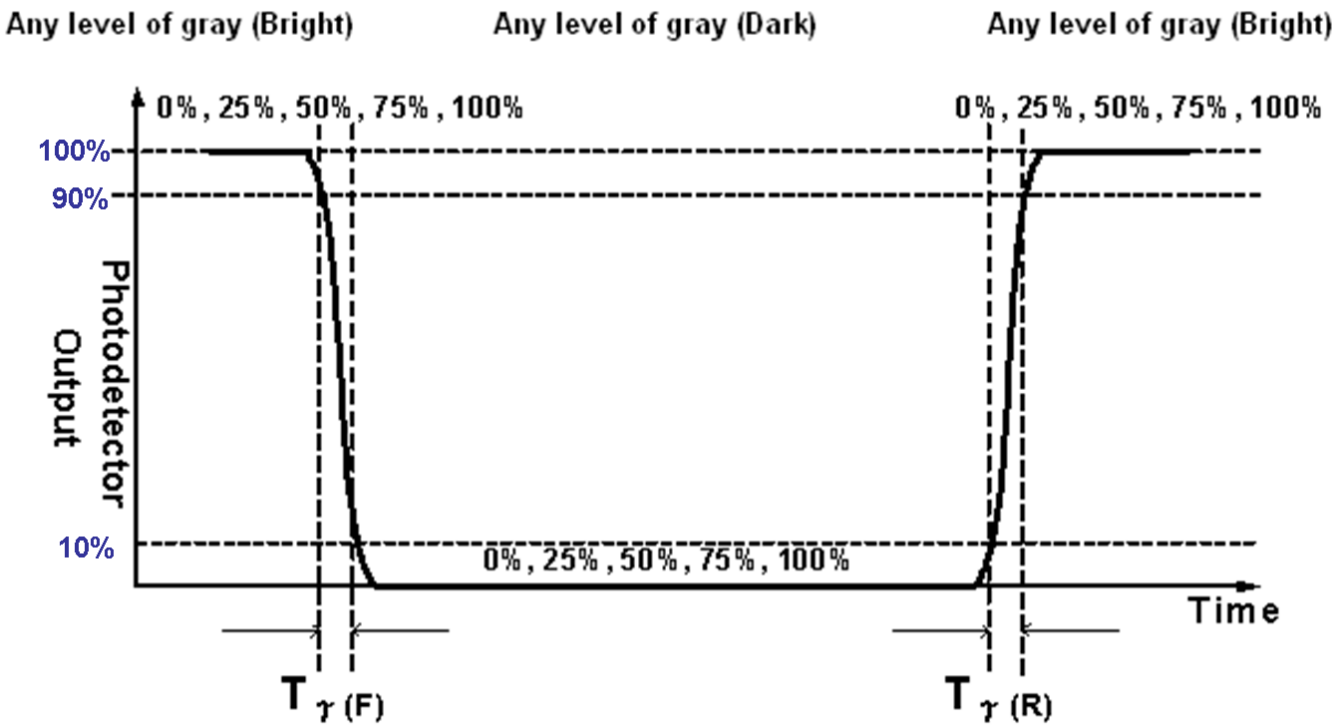
4. Response time T_γ is the average time required for display transition by switching the input signal for five luminance ratio (0%,25%,50%,75%,100% brightness matrix) and is based on Frame rate = 60Hz to optimize.

Measured Response Time		Target				
		0%	25%	50%	75%	100%
Start	0%		0% to 25%	0% to 50%	0% to 75%	0% to 100%
	25%	25% to 0%		25% to 50%	25% to 75%	25% to 100%
	50%	50% to 0%	50% to 25%		50% to 75%	50% to 100%
	75%	75% to 0%	75% to 25%	75% to 50%		75% to 100%
	100%	100% to 0%	100% to 25%	100% to 50%	100% to 75%	

T_γ is determined by 10% to 90% brightness difference of rising or falling period. (As illustrated)

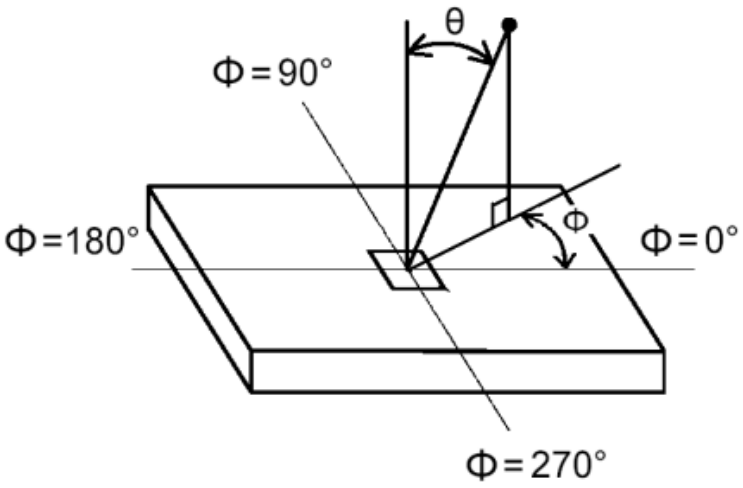
The response time is defined as the following figure and shall be measured by switching the input signal for "any level of gray(bright) " and "any level of gray(dark)".

FIG.3 Response Time



5. Light source here is the standard light source “C” which is defined by CIE and driving voltages are based on suitable gamma voltages. The calculating method is as following：
   A. Measure the “Module” and “BLU” optical spectrums (W, R, G, B).
   B. Calculate cell spectrum from “Module” and “BLU” spectrums.
   C. Calculate color chromaticity by using cell spectrum and the spectrum of standard light source “C”.
6. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG4.

FIG.4 Viewing Angle



7. Definition of Transmittance (T%):

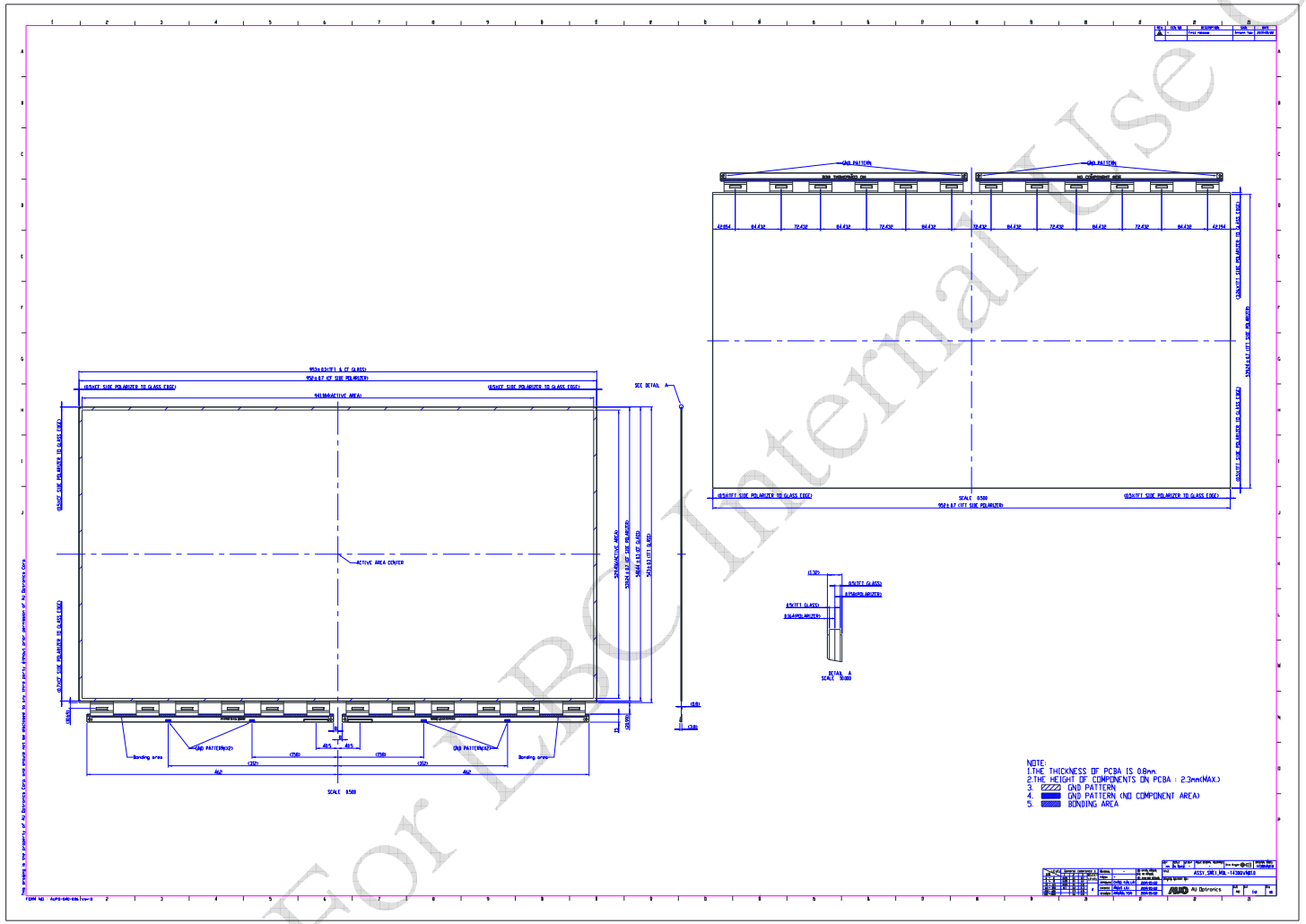
$$\text{Transmittance} = \frac{\text{Luminance of LCD module}}{\text{Luminance of backlight}} * 100\%$$

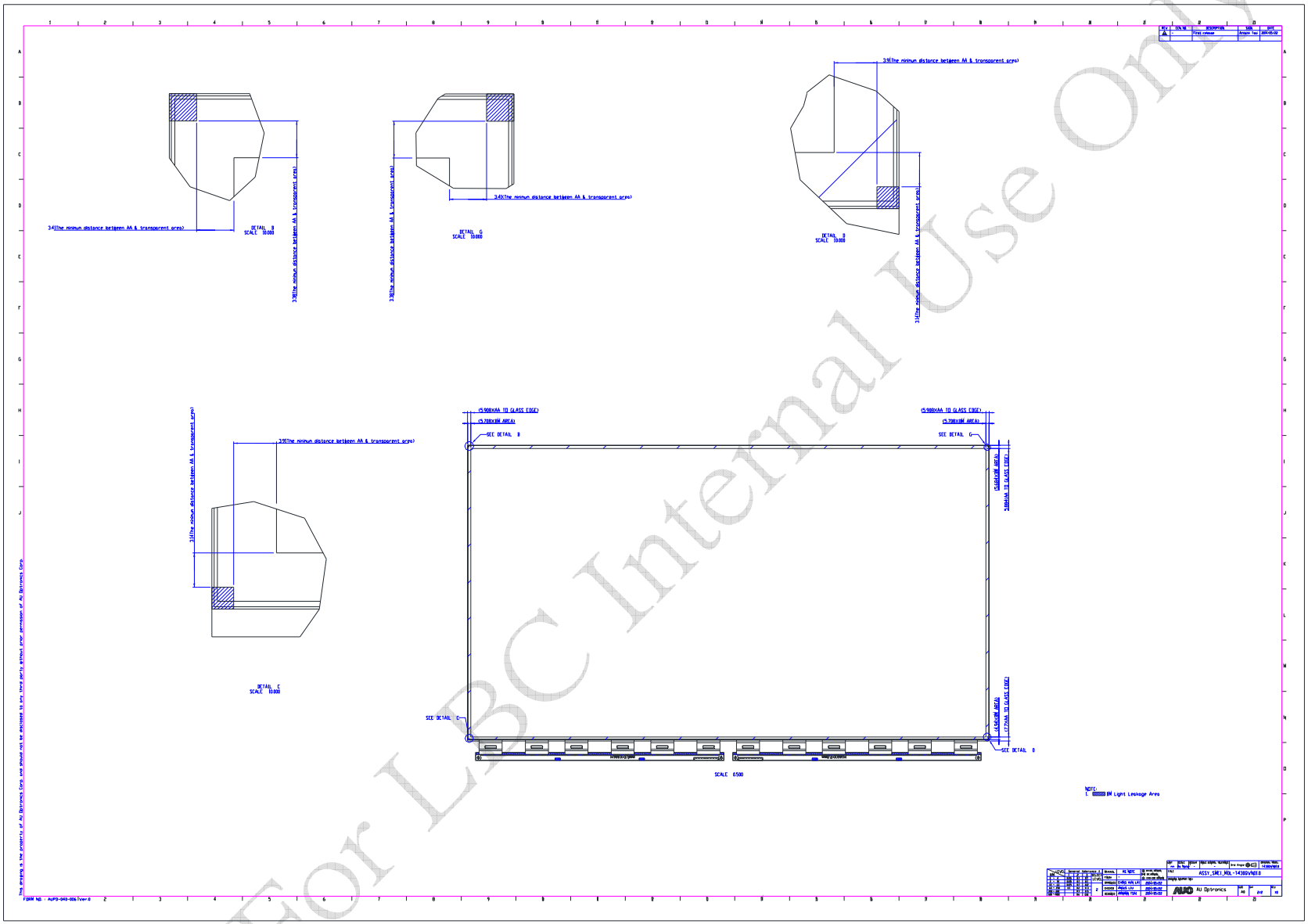
During transmittance measurement, the backlight of LCD module contains no brightness enhancement film. Two diffuser sheets which diffuse the light source uniformly are suggested to use for transmittance measurement.

5. Mechanical Characteristics

FFC CNT pin pitch requirement: 0.5mm

FFC CNT thickness requirement: 1.8mm (FFC 含補強板厚度 0.3mm)





6. Packing

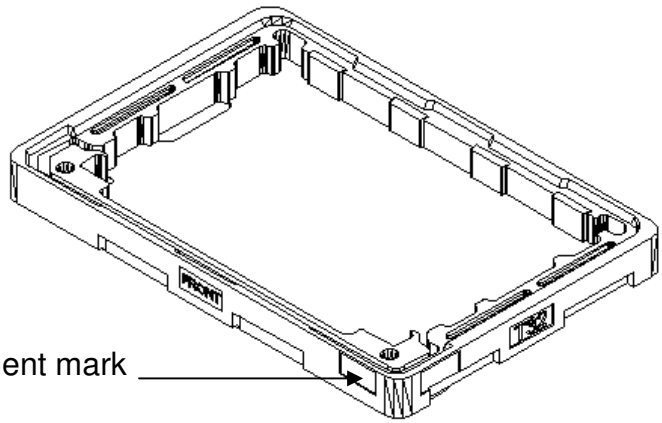
Open cell shipping label (35*7mm)

XXXXXXXXXXXX – XXXXXX – XXXX – XXXXXXXXXXX

1 2 3 4

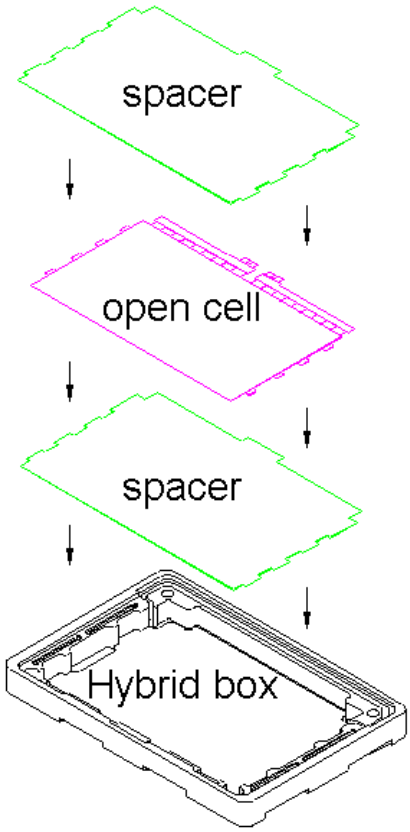
1. S/N Number
2. AUO internal use
3. Manufactured week
4. Model name

Carton Label:



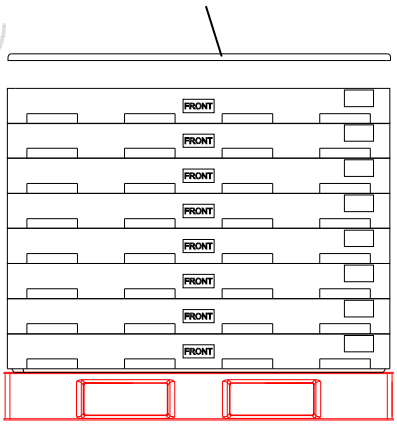
Carton label alignment mark

Packing Process:



Box for 12pcs open cells & 13pcs spacers

EPP Top Cover



Pallet Dimension:1100*800*140 mm

8 Boxes/Pallet, after stack 8 boxes, then put EPP top cover on it.

7. Precautions

Please pay attention to the followings when you use this TFT LCD Open Cell unit and strongly recommended to contact AUO if module process advice is required.

7.1 Mounting Precautions

(1) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the cell. And the frame on which a cell is mounted should have sufficient strength so that external force is not transmitted directly to the cell.

(2) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.

(3) You should adopt radiation structure to satisfy the temperature specification.

(3) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
(4) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of polarizer for bare hand or greasy cloth. (Some cosmetics are detrimental to the polarizer.)
(5) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front/ rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
(6) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
(7) Do not open the case because inside circuits do not have sufficient strength.

7.2 Operating Precautions

(1) The open cell unit listed in the product specification sheets was designed and manufactured for TV application

(2) The spike noise causes the mis-operation of circuits. It should be lower than following voltage: V=±200mV(Over and under shoot voltage)

(3) Response time depends on the temperature. (In lower temperature, it becomes longer.)

(4) Transmittance depends on the temperature. (In lower temperature, it becomes lower.) And in lower temperature, response time (required time that brightness is stable after turned on) becomes longer.

(5) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.

(6) When fixed patterns are displayed for a long time, remnant image is likely to occur.

(7) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interface.

7.3 Electrostatic Discharge Control

Since a open cell unit is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

7.4 Precautions for Strong Light Exposure

Strong light exposure causes degradation of polarizer and color filter.

7.5 Storage

When storing open cell units as spares for a long time, the following precautions are necessary.

(1) Store them in a dark place. Do not expose the open cell unit to sunlight or fluorescent light. Keep the temperature between 5℃ and 35℃ at normal humidity.

(2) The polarizer surface should not come in contact with any other object. It is recommended that they be stored in the container in which they were shipped.

7.6 Handling Precautions for Protection Film of Polarizer

The protection film of polarizer is still attached on the surface as you receive open cell units. When the protection film is peeled off, static electricity is easily generated on the polarizer surface. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.

