

## Medium Power Phase Control Thyristors (Power Modules), 50 A/70 A/90 A



D-55

**FEATURES**

- Electrically isolated base plate
- Types up to 1200 V<sub>RRM</sub>
- 3500 V<sub>RMS</sub> isolating voltage
- Simplified mechanical designs, rapid assembly
- High surge capability
- Large creepage distances
- UL E78996 approved
- RoHS compliant
- Designed and qualified for industrial level


**RoHS  
COMPLIANT**
**PRODUCT SUMMARY**

$I_{T(AV)}$	50 A/70 A/90 A
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**DESCRIPTION**

These series of T-modules are intended for general purpose applications such as battery chargers, welders and plating equipment, regulated power supplies and temperature and speed control circuits. The semiconductors are electrically isolated from the metal base, allowing common heatsinks and compact assemblies to be built.

**MAJOR RATINGS AND CHARACTERISTICS**

SYMBOL	CHARACTERISTICS	T50RIA	T70RIA	T90RIA	UNITS
$I_{T(AV)}$	70 °C	50	70	90	A
$I_{T(RMS)}$		80	110	141	A
$I_{TSM}$	50 Hz	1310	1660	1780	A
	60 Hz	1370	1740	1870	
$I^2t$	50 Hz	8550	13 860	15 900	A <sup>2</sup> s
	60 Hz	7800	12 650	14 500	
$I^2\sqrt{t}$		85 500	138 500	159 100	A <sup>2</sup> /s
V <sub>RRM</sub>	Range	100 to 1200			V
T <sub>J</sub>		- 40 to 125			°C

**ELECTRICAL SPECIFICATIONS**
**VOLTAGE RATINGS**

TYPE NUMBER	VOLTAGE CODE	V <sub>RRM</sub> /V <sub>DRM</sub> , MAXIMUM REPETITIVE PEAK REVERSE AND PEAK OFF-STATE VOLTAGE V	V <sub>RSM</sub> , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I <sub>RRM</sub> /I <sub>DRM</sub> MAXIMUM AT T <sub>J</sub> = 25 °C μA
T50RIA T70RIA T90RIA	10	100	150	100
	20	200	300	
	40	400	500	
	60	600	700	
	80	800	900	
	100	1000	1100	
	120	1200	1300	

ON-STATE CONDUCTION								
PARAMETER	SYMBOL	TEST CONDITIONS		T50RIA	T70RIA	T90RIA	UNITS	
Maximum average on-state current at case temperature	$I_{T(AV)}$	180° conduction, half sine wave		50	70	90	A	
				70	70	70	°C	
Maximum RMS on-state current	$I_{T(RMS)}$			80	110	141	A	
Maximum peak, one-cycle on-state, non-repetitive surge current	$I_{TSM}$	t = 10 ms	No voltage reappplied	Sine half wave, initial $T_J = T_J$ maximum	1310	1660	1780	A
		t = 8.3 ms			1370	1740	1870	
		t = 10 ms	100 % $V_{RRM}$ reappplied		1100	1400	1500	
		t = 8.3 ms			1150	1460	1570	
Maximum $I^2t$ for fusing	$I^2t$	t = 10 ms	No voltage reappplied		8550	13 860	15 900	A <sup>2</sup> s
		t = 8.3 ms			7800	12 650	14 500	
		t = 10 ms	100 % $V_{RRM}$ reappplied		6050	9800	11 250	
		t = 8.3 ms			5520	8950	10 270	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 to 10 ms, no voltage reappplied		85 500	138 500	159 100	A <sup>2</sup> √s	
Low level value of threshold voltage	$V_{T(TO)1}$	(16.7 % $\times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)}$ ), $T_J$ maximum		0.97	0.77	0.78	V	
High level value of threshold voltage	$V_{T(TO)2}$	(I $> \pi \times I_{T(AV)}$ ), $T_J$ maximum		1.13	0.88	0.88		
Low level value of on-state slope resistance	$r_{t1}$	(16.7 % $\times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)}$ ), $T_J$ maximum		4.1	3.6	2.9	mΩ	
High level value of on-state slope resistance	$r_{t2}$	(I $> \pi \times I_{T(AV)}$ ), $T_J$ maximum		3.3	3.2	2.6		
Maximum on-state voltage drop	$V_{TM}$	$I_{TM} = \pi \times I_{T(AV)}$ , $T_J = 25$ °C, $t_p = 400$ μs square Average power = $V_{T(TO)} \times I_{T(AV)} + r_f \times (I_{T(RMS)})^2$		1.60	1.55	1.55	V	
Maximum forward voltage drop	$V_{FM}$	$I_{TM} = \pi \times I_{T(AV)}$ , $T_J = 25$ °C, $t_p = 400$ μs square Average power = $V_{T(TO)} \times I_{T(AV)} + r_f \times (I_{T(RMS)})^2$		1.60	1.55	1.55	V	
Maximum holding current	$I_H$	Anode supply = 6 V, initial $I_T = 30$ A, $T_J = 25$ °C		200	200	200	mA	
Maximum latching current	$I_L$	Anode supply = 6 V, resistive load = 10 Ω Gate pulse: 10 V, 100 μs, $T_J = 25$ °C		400	400	400		

SWITCHING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Typical turn-on time	$t_{gd}$	$T_J = 25$ °C, $V_d = 50$ % $V_{DRM}$ , $I_{TM} = 50$ A $I_g = 500$ mA, $t_r \leq 0.5$ , $t_p \geq 6$ μs	0.9	μs
Typical reverse recovery time	$t_{rr}$	$T_J = 125$ °C, $I_{TM} = 50$ A, $t_p = 300$ μs, $di/dt = 10$ A/μs	3	
Typical turn-off time	$t_q$	$T_J = T_J$ maximum, $I_{TM} = 50$ A, $t_p = 300$ μs $-di/dt = 15$ A/μs, $V_R = 100$ V, linear to 80 % $V_{DRM}$	110	



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BLOCKING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak reverse and off-state leakage current	$I_{RRM}$ , $I_{DRM}$	$T_J = T_J$ maximum	15	mA
RMS isolation voltage	$V_{ISOL}$	50 Hz, circuit to base, all terminals shorted, $T_J = 25\text{ °C}$ , $t = 1\text{ s}$	3500	V
Critical rate of rise of off-state voltage	$dV/dt$	$T_J = T_J$ maximum, linear to 80 % rated $V_{DRM}$ <sup>(1)</sup>	500	V/ $\mu$ s

### Note

<sup>(1)</sup> Available with  $dV/dt = 1000\text{ V}/\mu\text{s}$ , to complete code add S90 i.e. T90RIA80S90

TRIGGERING						
PARAMETER	SYMBOL	TEST CONDITIONS	T50RIA	T70RIA	T90RIA	UNITS
Maximum peak gate power	$P_{GM}$	$T_J = T_J$ maximum, $t_p \leq 5\text{ ms}$	10	12	12	W
Maximum average gate power	$P_{G(AV)}$	$T_J = T_J$ maximum, $f = 50\text{ Hz}$	2.5	3	3	
Maximum peak gate current	$I_{GM}$	$T_J = T_J$ maximum, $t_p \leq 5\text{ ms}$	2.5	3	3	A
Maximum peak negative gate voltage	$-V_{GT}$		10	10	10	V
Maximum required DC gate voltage to trigger	$V_{GT}$	$T_J = -40\text{ °C}$	4.0	4.0	4.0	V
		$T_J = 25\text{ °C}$	2.5	2.5	2.5	
		$T_J = T_J$ maximum	1.5	1.5	1.5	
Maximum required DC gate current to trigger	$I_{GT}$	$T_J = -40\text{ °C}$	250	270	270	mA
		$T_J = 25\text{ °C}$	100	120	120	
		$T_J = T_J$ maximum	50	60	60	
Maximum gate voltage that will not trigger	$V_{GD}$	$T_J = T_J$ maximum, rated $V_{DRM}$ applied	0.2	0.2	0.2	V
Maximum gate current that will not trigger	$I_{GD}$		5.0	6.0	6.0	mA
Maximum rate of rise of turned-on current	$dI/dt$	$V_D = 0.67$ rated $V_{DRM}$ , $I_{TM} = 2 \times$ rated $dI/dt$ $I_g = 400\text{ mA}$ for T50RIA and $I_g = 500\text{ mA}$ for T70RIA/T90RIA; $t_r < 0.5\ \mu\text{s}$ , $t_p \geq 6\ \mu\text{s}$ For repetitive value use 40 % non-repetitive Per JEDEC STD. RS397, 5.2.2.6	200	200	200	A/ $\mu$ s
			180	180	180	
			160	160	160	
			150	150	150	

THERMAL AND MECHANICAL SPECIFICATIONS							
PARAMETER	SYMBOL	TEST CONDITIONS		T50RIA	T70RIA	T90RIA	UNITS
Maximum junction operating temperature range	$T_J$			- 40 to 125			°C
Maximum storage temperature range	$T_{Stg}$			- 40 to 150			
Maximum thermal resistance, junction to case per junction	$R_{thJC}$	DC operation		0.65	0.50	0.38	K/W
Maximum thermal resistance, case to heatsink	$R_{thCS}$	Mounting surface, smooth, flat and greased		0.2			
Mounting torque, $\pm 10\%$ to heatsink terminals		Non-lubricated threads	M3.5 mounting screws <sup>(1)</sup>	1.3 $\pm$ 10 %			Nm
			M5 screw terminals	3 $\pm$ 10 %			
Approximate weight				54			g
Case style		T-module		D-55			

**Note**

<sup>(1)</sup> A mounting compound is recommended and the torque should be rechecked after a period of 3 hours to allow for the spread of the compound

$\Delta R$ CONDUCTION PER JUNCTION											
DEVICES	SINUSOIDAL CONDUCTION AT $T_J$ MAXIMUM					RECTANGULAR CONDUCTION AT $T_J$ MAXIMUM					UNITS
	180°	120°	90°	60°	30°	180°	120°	90°	60°	30°	
T50RIA	0.08	0.10	0.13	0.19	0.31	0.06	0.10	0.14	0.20	0.32	K/W
T70RIA	0.07	0.08	0.10	0.14	0.24	0.05	0.08	0.11	0.15	0.24	
T90RIA	0.05	0.06	0.08	0.12	0.20	0.04	0.06	0.09	0.12	0.20	

**Note**

- Table shows the increment of thermal resistance  $R_{thJC}$  when devices operate at different conduction angles than DC



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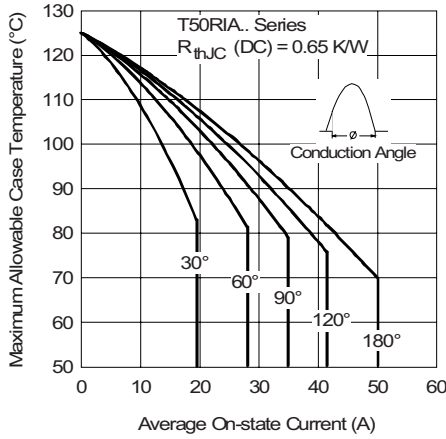


Fig. 1 - Current Ratings Characteristics

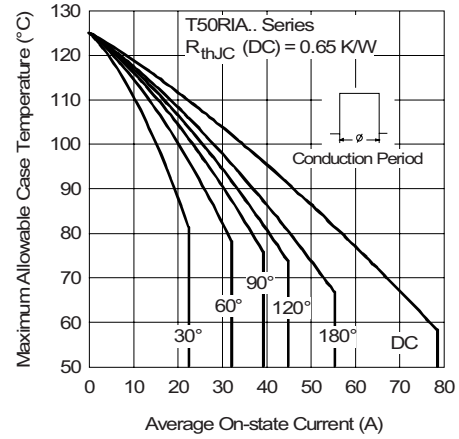


Fig. 2 - Current Ratings Characteristics

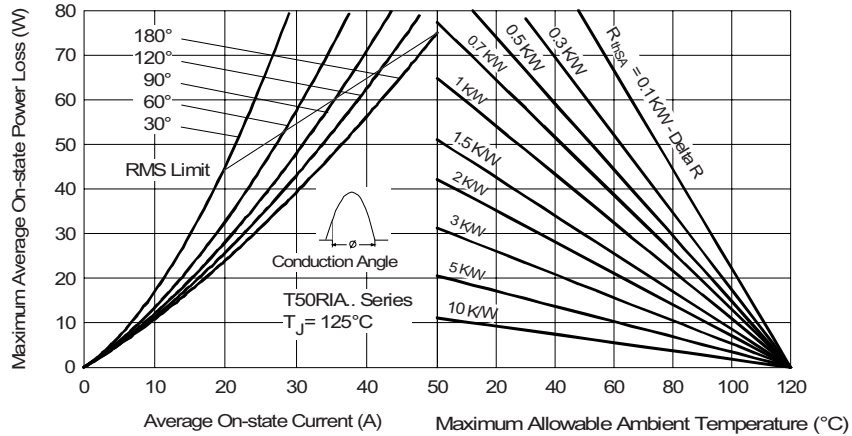


Fig. 3 - On-State Power Loss Characteristics

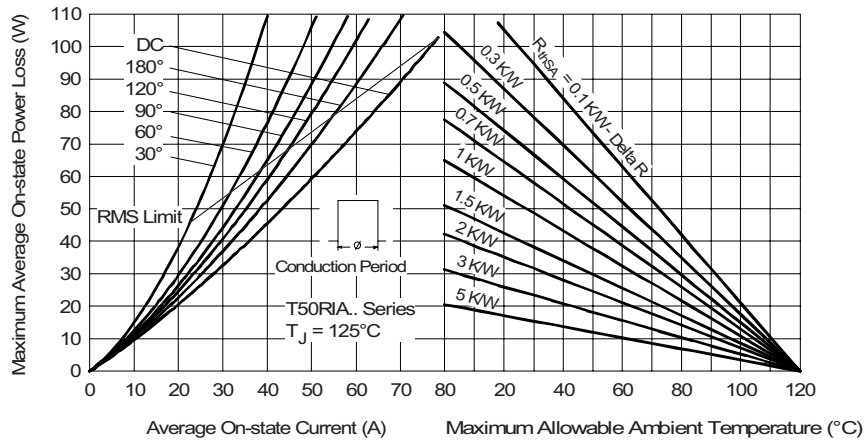


Fig. 4 - On-State Power Loss Characteristics

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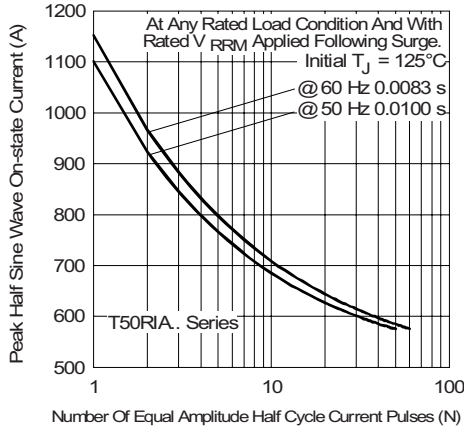


Fig. 5 - Maximum Non-Repetitive Surge Current

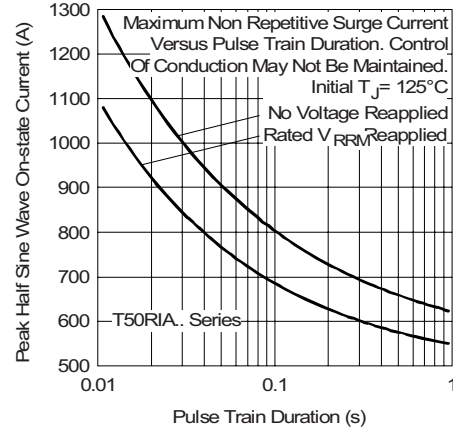


Fig. 6 - Maximum Non-Repetitive Surge Current

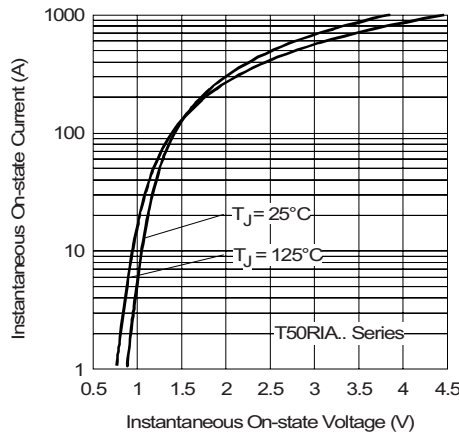


Fig. 7 - On-State Voltage Drop Characteristics

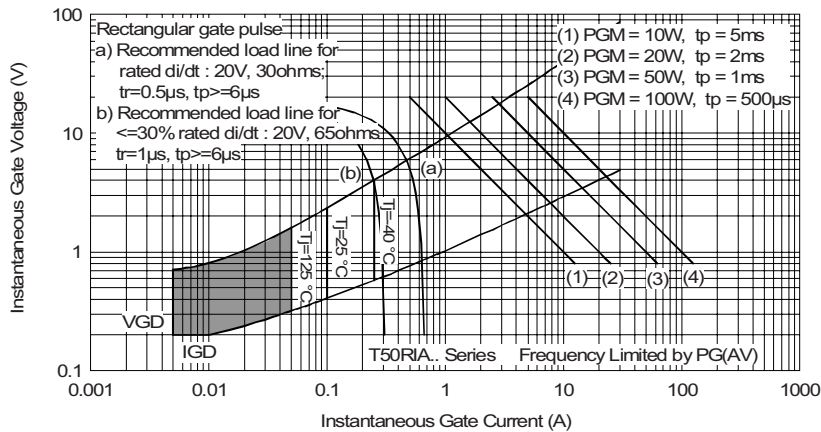


Fig. 8 - Gate Characteristics



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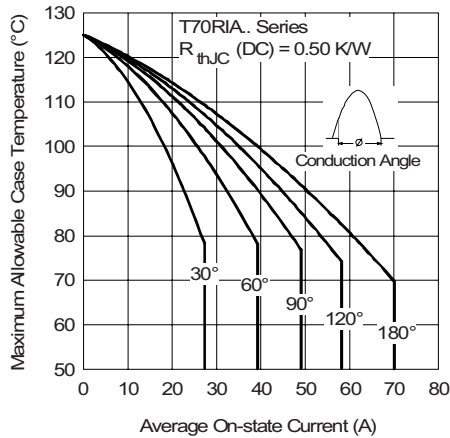


Fig. 9 - Current Ratings Characteristics

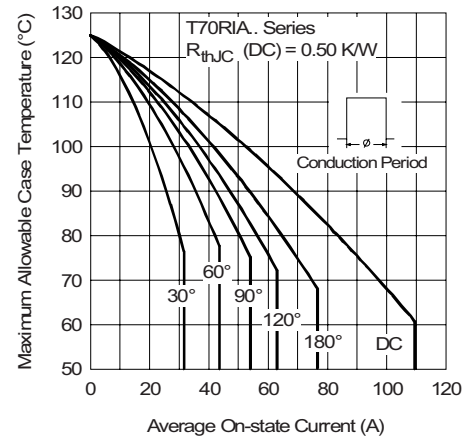


Fig. 10 - Current Ratings Characteristics

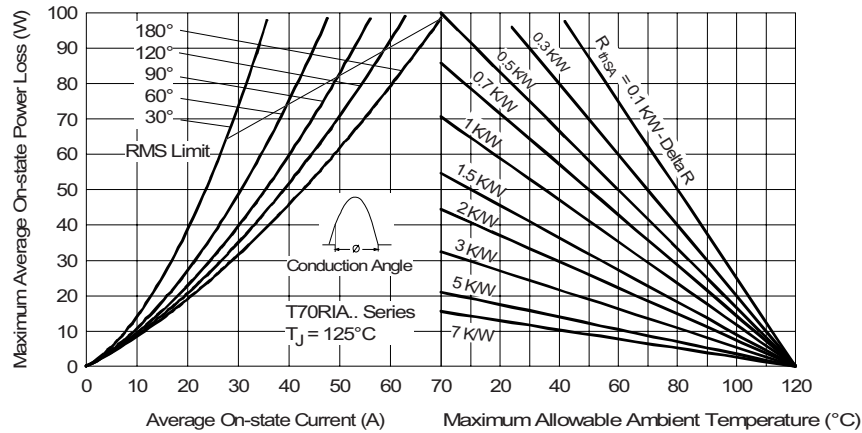


Fig. 11 - On-State Power Loss Characteristics

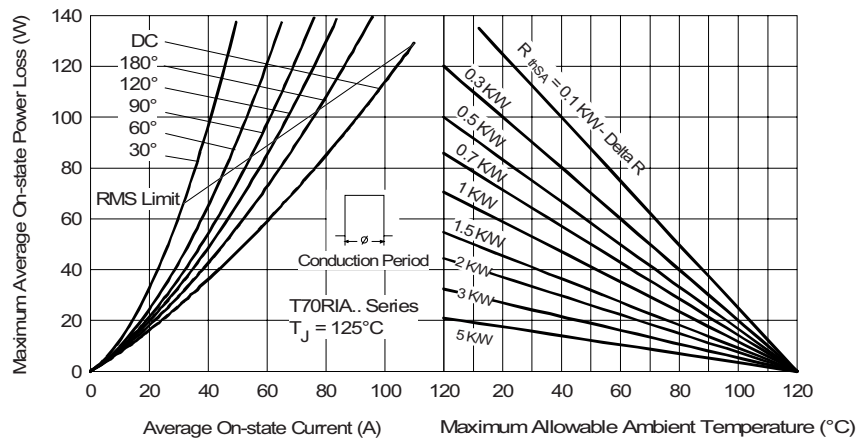


Fig. 12 - On-State Power Loss Characteristics

## Vishay High Power Products Medium Power Phase Control Thyristors (Power Modules), 50 A/70 A/90 A

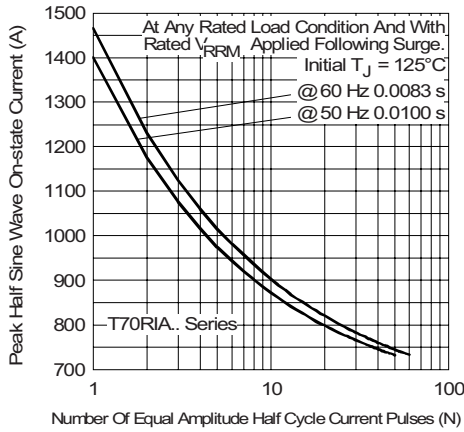


Fig. 13 - Maximum Non-Repetitive Surge Current

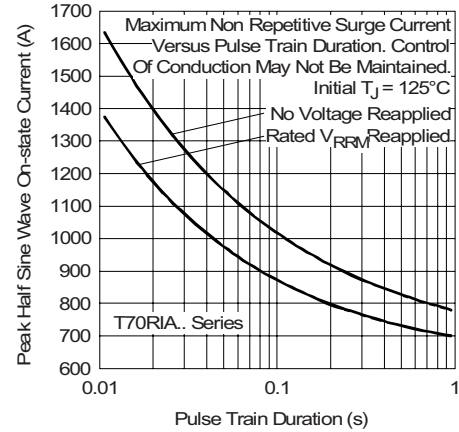


Fig. 14 - Maximum Non-Repetitive Surge Current

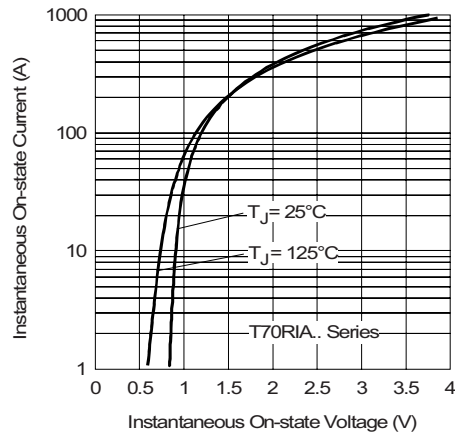


Fig. 15 - On-State Voltage Drop Characteristics

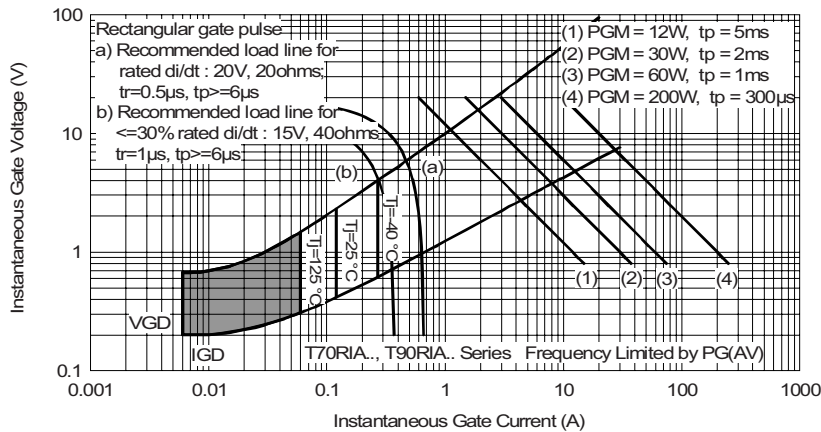


Fig. 16 - Gate Characteristics





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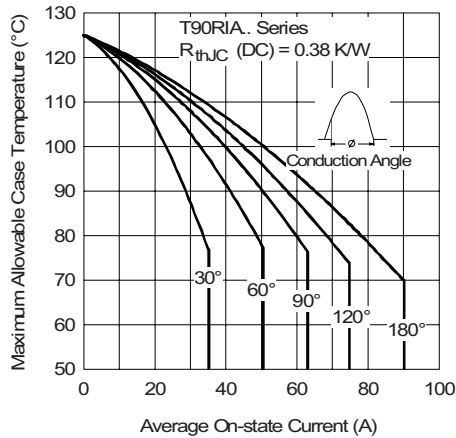


Fig. 17 - Current Ratings Characteristics

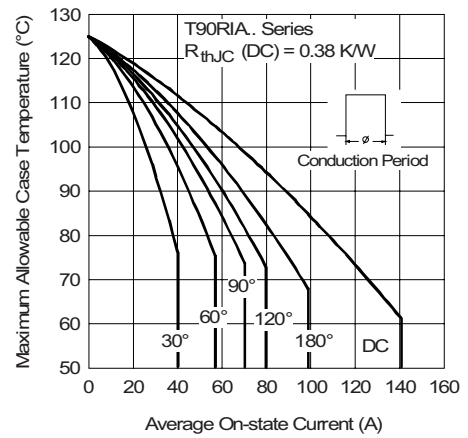


Fig. 18 - Current Ratings Characteristics

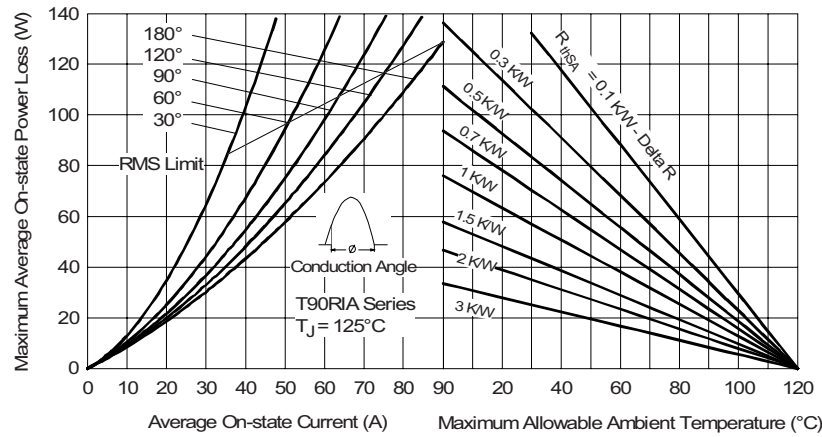


Fig. 19 - On-State Power Loss Characteristics

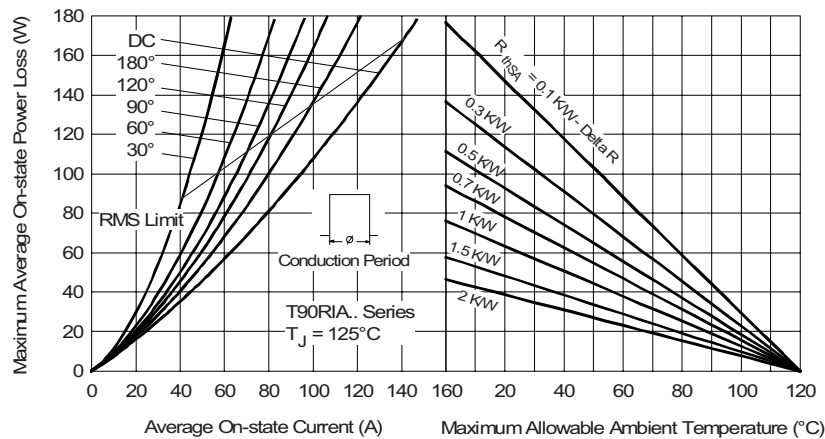


Fig. 20 - On-State Power Loss Characteristics

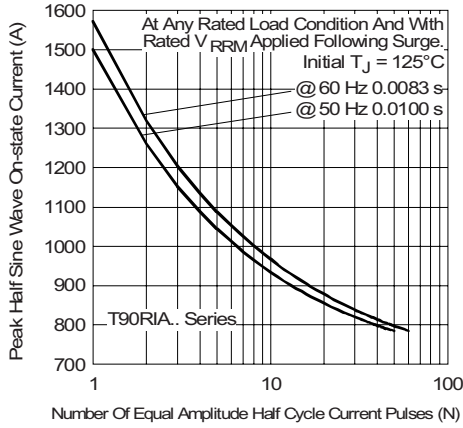


Fig. 21 - Maximum Non-Repetitive Surge Current

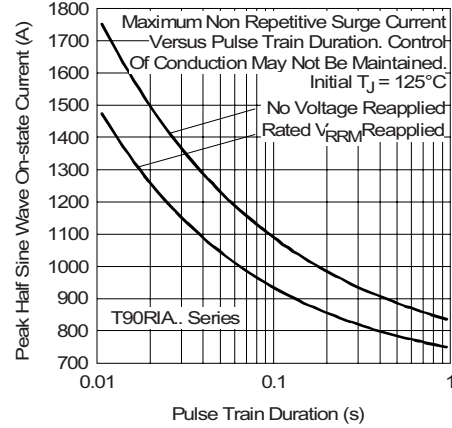


Fig. 22 - Maximum Non-Repetitive Surge Current

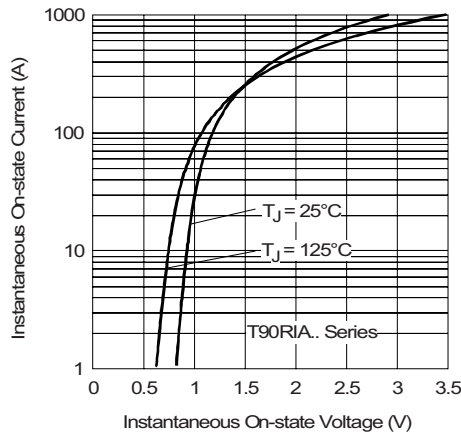


Fig. 23 - On-State Voltage Drop Characteristics

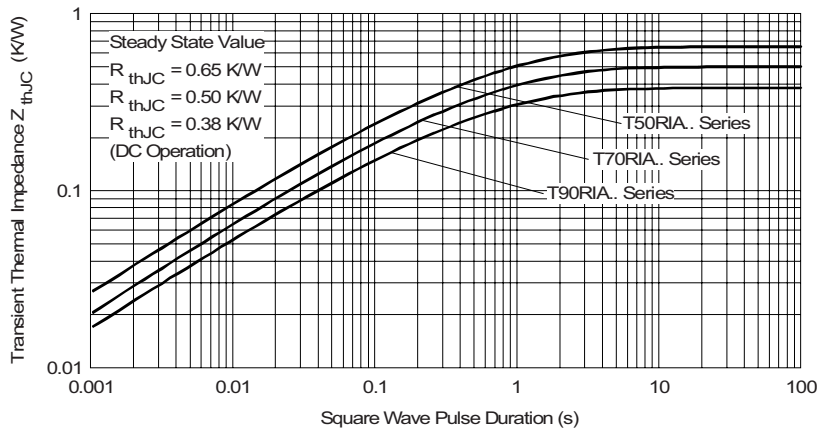


Fig. 24 - Thermal Impedance  $Z_{thJC}$  Characteristics

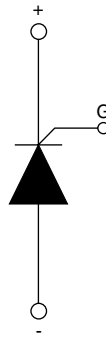


## ORDERING INFORMATION TABLE

Device code	<b>T</b>	<b>50</b>	<b>RIA</b>	<b>120</b>
	①	②	③	④

- 1** - Module type
- 2** - Current rating
- 3** - Circuit configuration
- 4** - Voltage code x 10 =  $V_{RRM}$

## CIRCUIT CONFIGURATION



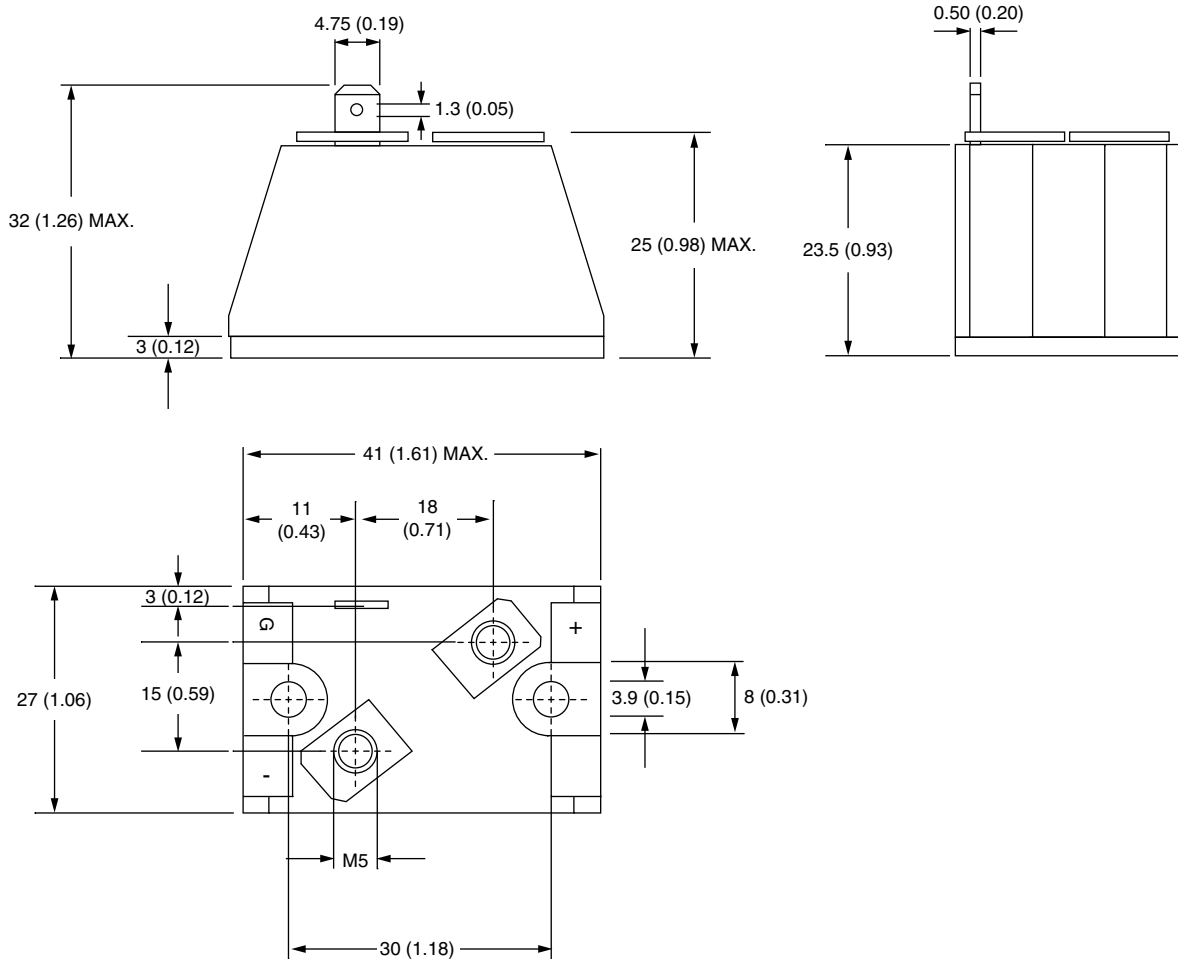
### LINKS TO RELATED DOCUMENTS

Dimensions

<http://www.vishay.com/doc?95336>

## D-55 T-Module Thyristor Standard

**DIMENSIONS** in millimeters (inches)





## Disclaimer

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