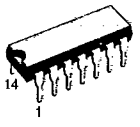
LOW POWER SCHOTTKY INTEGRATED CIRCUITS

T54LS164
T74LS164

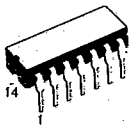
SERIAL-IN PARALLEL-OUT SHIFT REGISTER

DESCRIPTION

The T54LS164/T74LS164 is a 8-Bit Serial-In Parallel-Out Shift Register. Serial data is entered through a 2-Input AND gate synchronous with the LOW to HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register setting all outputs LOW indipendent of the clock. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all SGS TTL products.



B1
Plastic Package



D1/D2
Ceramic Package

M1
Micro Package

C1
Plastic Chip Carrier

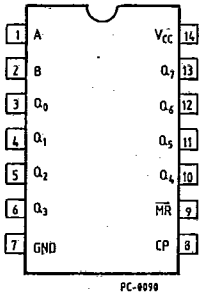
ORDERING NUMBERS:

T54LS164 D2	T74LS164 C1
T74LS164 D1	T74LS164 M1
T74LS164 B1	

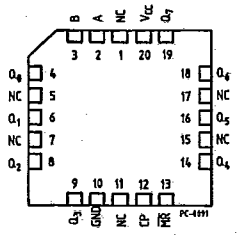
- TYPICAL SHIFT FREQUENCY OF 35 MHz
- ASYNCHRONOUS MASTER RESET
- GATED SERIAL DATA INPUT
- FULLY SYNCHRONOUS DATA TRANSFERS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

PIN CONNECTION
(top view)

DUAL IN LINE



CHIP CARRIER



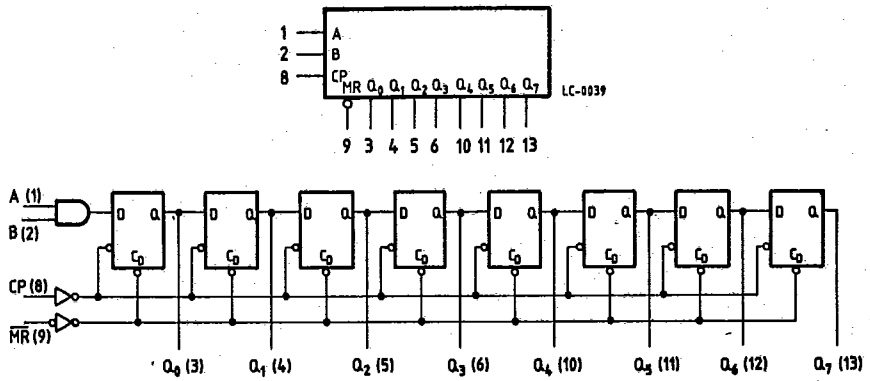
NC = No Internal Connection

PIN NAMES

A, B	Data input
CP	Clock (Active HIGH Going Edge) Input
MR	Master Reset (Active LOW) Input
Q_0-Q_7	Outputs

T54LS164
T74LS164

LOGIC SYMBOL AND LOGIC DIAGRAM



V_{CC} = Pin 14
GND = Pin 7
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	Input Voltage, Applied to Input	−0.5 to 15	V
V_O	Output Voltage, Applied to Output	−0.5 to 10	V
I_I	Input Current, Into Inputs	−30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS164D2	4.5 V	5.0 V	5.5 V	−55°C to +125°C
T74LS164XX	4.75 V	5.0 V	5.25 V	0°C to +70°C

XX = package type.

T54LS164
T74LS164

FUNCTIONAL DESCRIPTION

The LS164 is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active HIGH Enable for data entry through the other input. An unused input must be tied HIGH, or both inputs connected together.

Each LOW-to-HIGH transition on the Clock (CP) input shifts data one place to the right and enters into Q_0 the logical AND of the two inputs (A•B) that existed before the rising clock edge.
A LOW level on the Master Reset (MR) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs LOW.

TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{MR}$	A	B	Q_0	Q_1-Q_7
Reset (Clear)	L	X	X	L	L-L
Shift	H	l	l	L	q_0-q_6
	H	l	h	L	q_0-q_6
	H	h	l	L	q_0-q_6
	H	h	h	H	q_0-q_6

L (l) = LOW Voltage Levels
H (h) = HIGH Voltage Levels
X = Don't Care
q_n = Lower case letters indicate the state of the referenced input or output one set-up time prior to the LOW to HIGH clock transition.

AC WAVEFORMS

Fig. 1 - Clock to Output Delays and Clock Pulse Width

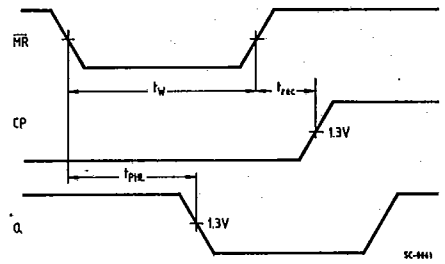
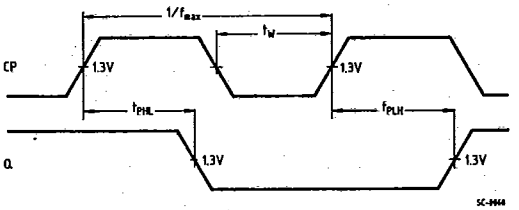
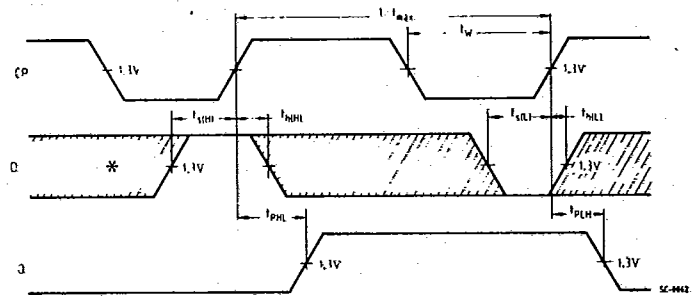


Fig. 2 - Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



Conditions: $\overline{MR}$ = H

Fig. 3 - Data Set-up and Hold Time



* The shaded areas indicate when the input is permitted to change for predictable output performance

T54LS164
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DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Test Conditions (Note 1)	Units
V_{IH}	Input HIGH Voltage		2.0			Guaranteed input HIGH Voltage for all Inputs	V
V_{IL}	Input LOW Voltage	54			0.7	Guaranteed input LOW Voltage for all Inputs	V
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V_{CC} = MIN, I_{IN} = −18mA	V
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V_{CC} = MIN, I_{OH} = −400μA, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	I_{OL} = 4.0mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74		0.35	0.5	I_{OL} = 8.0mA	
I_{IH}	Input HIGH Current				20 0.1	V_{CC} = MAX, V_{IN} = 2.7V V_{CC} = MAX, V_{IN} = 7.0V	μA mA
I_{IL}	Input LOW Current				−0.4	V_{CC} = MAX, V_{IN} = 0.4V	mA
I_{OS}	Output Short Circuit Current (Note 2)		−20		−100	V_{CC} = MAX, V_{OUT} = 0V	mA
I_{CC}	Power Supply Current (Note 3)			16	27	V_{CC} = MAX	mA

AC CHARACTERISTICS: T_A = 25°C

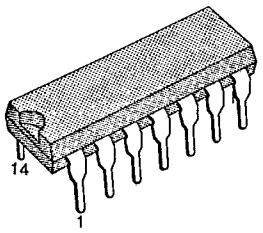
Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Test Conditions		Units
f_{MAX}	Maximum Clock Frequency	25	36		Fig. 1	V_{CC} = 5.0V, C_L = 15pF	MHz
t_{PLH} t_{PHL}	Propagation Delay, Positive-Going Clock to Outputs		17 21	27 32	Fig. 1		ns
t_{PHL}	Propagation Delay, Negative-Going MR to Outputs		24	36	Fig. 2		ns

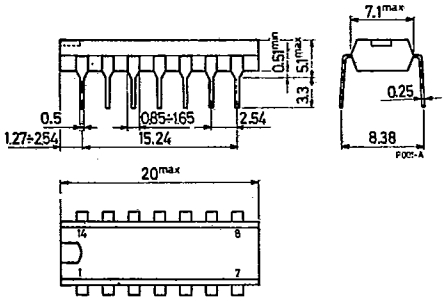
Notes:
1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "wrost case" conditions.
2) Not more than one output should be shorted at a time.
3) I_{CC} is measured with outputs open serial input at 2.4V, and a momentary ground, then 4.5V applied to clear.
4) Typical values are at V_{CC} = 5.0V, T_A = 25°C.

AC SET-UP REQUIREMENTS: $T_A = 25°C$

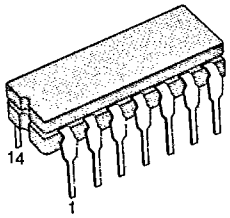
Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
t_s	Set-Up Time, A or B Input to Positive-Going CP	15			Fig. 3	$V_{CC} = 5.0V$ $C_L = 15pF$	ns
t_h	Hold Time, A or B Input to Positive-Going CP	5			Fig. 3		ns
$t_W CP(H)$	CP Pulse Width (HIGH)	20			Fig. 1		ns
$t_W CP(L)$	CP Pulse Width (LOW)	20			Fig. 1		ns
$t_W MR(L)$	MR Pulse Width (LOW)	20			Fig. 2		ns
t_{rec}	Recovery Time, Positive-Going MR to Positive-Going CP	20			Fig. 2		ns

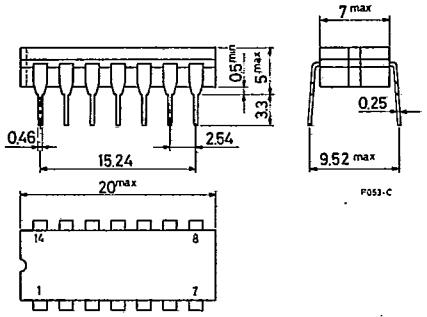
14-LEAD PLASTIC DIP





14-LEAD CERAMIC DIP





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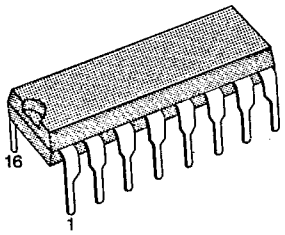
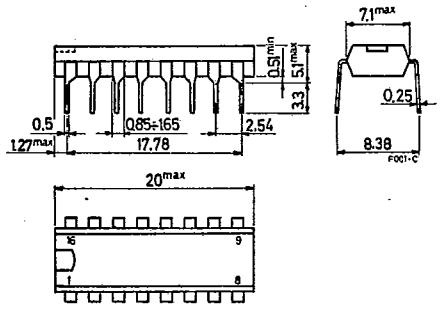
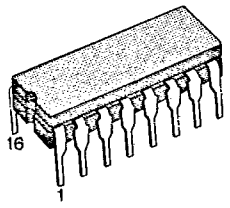
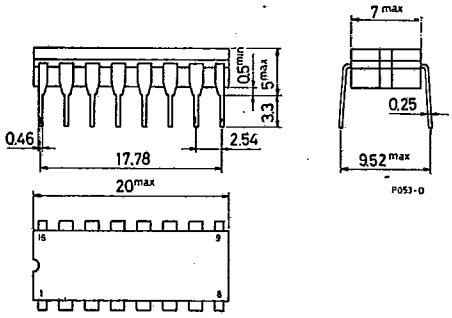




Packages

16-LEAD CERAMIC DIP





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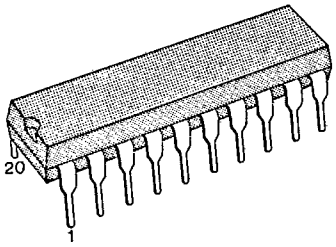

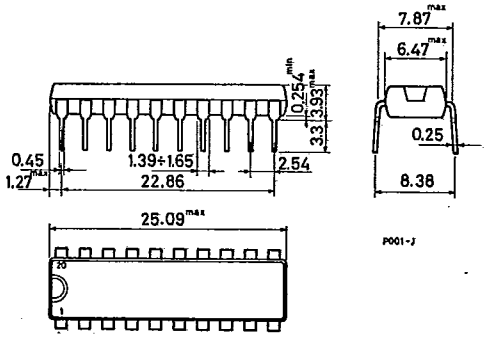

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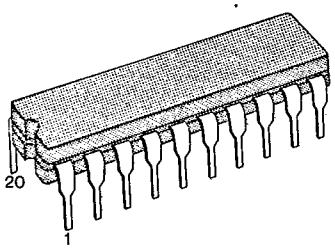
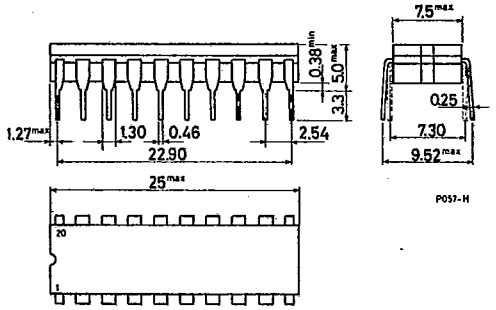
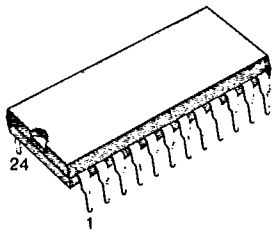
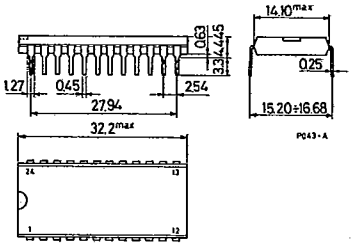




Packages

24-LEAD PLASTIC DIP





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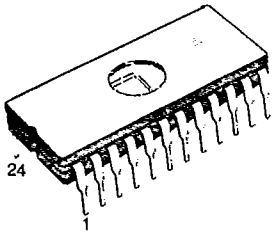
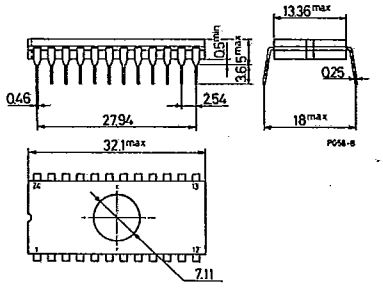
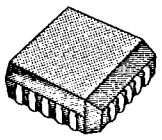
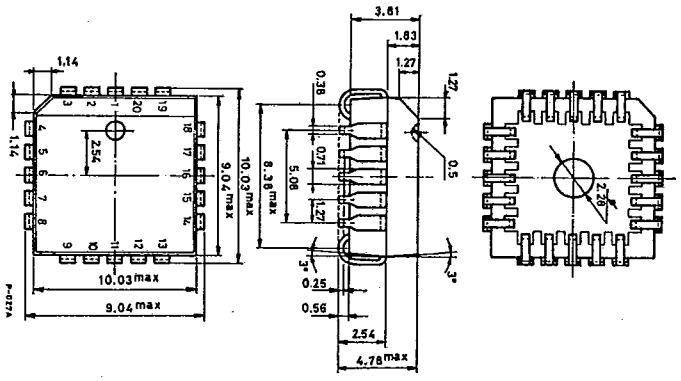




CHIP CARRIER 20 LEAD PLASTIC

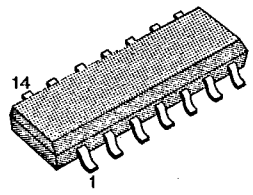


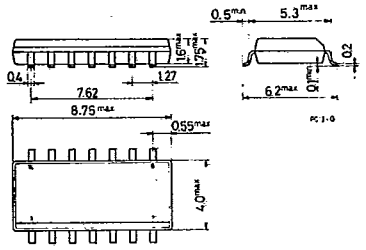


Packages

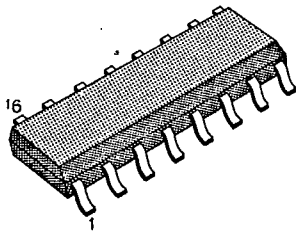
T-90-20

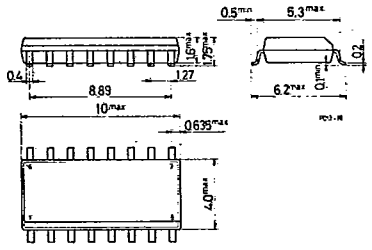
14-LEAD PLASTIC DIP MICROPACKAGE





16-LEAD PLASTIC DIP MICROPACKAGE





NOTE: FOR 20-LEAD PLASTIC DIP MICROPACKAGE CONTACT SGS