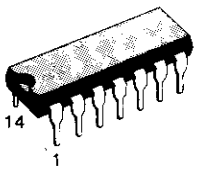
T54LS95B
T74LS95B

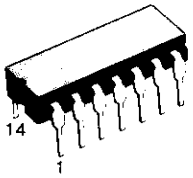
4-BIT SHIFT REGISTER

DESCRIPTION

The T54LS95B/T74LS95B is a 4-Bit Shift Register with serial and parallel synchronous operating modes. The serial shift right and parallel load are activated by separate clock inputs which are selected by a mode control input. The data is transferred from the serial or parallel D inputs to the Q outputs synchronous with the HIGH to LOW transition of the appropriate clock input.
The LS95B is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all SGS TTL families.

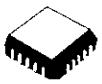


B1
Plastic Package



D1/D2
Ceramic Package

M1
Micro Package



C1
Plastic Chip Carrier

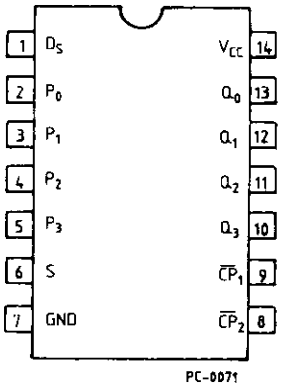
ORDERING NUMBERS:

T54LS95B D2	T74LS95B C1
T74LS95B D1	T74LS95B M1
T74LS95B B1	

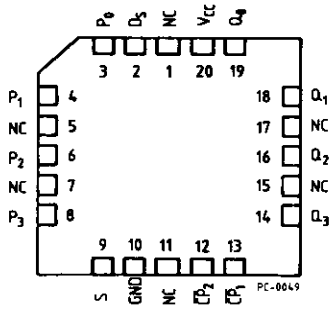
- SYNCHRONOUS, EXPANDABLE SHIFT RIGHT
- SYNCHRONOUS, SHIFT LEFT CAPABILITY
- SYNCHRONOUS, PARALLEL LOAD
- SEPARATE SHIFT AND LOAD CLOCK INPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

PIN CONNECTION
(top view)

DUAL IN LINE



CHIP CARRIER

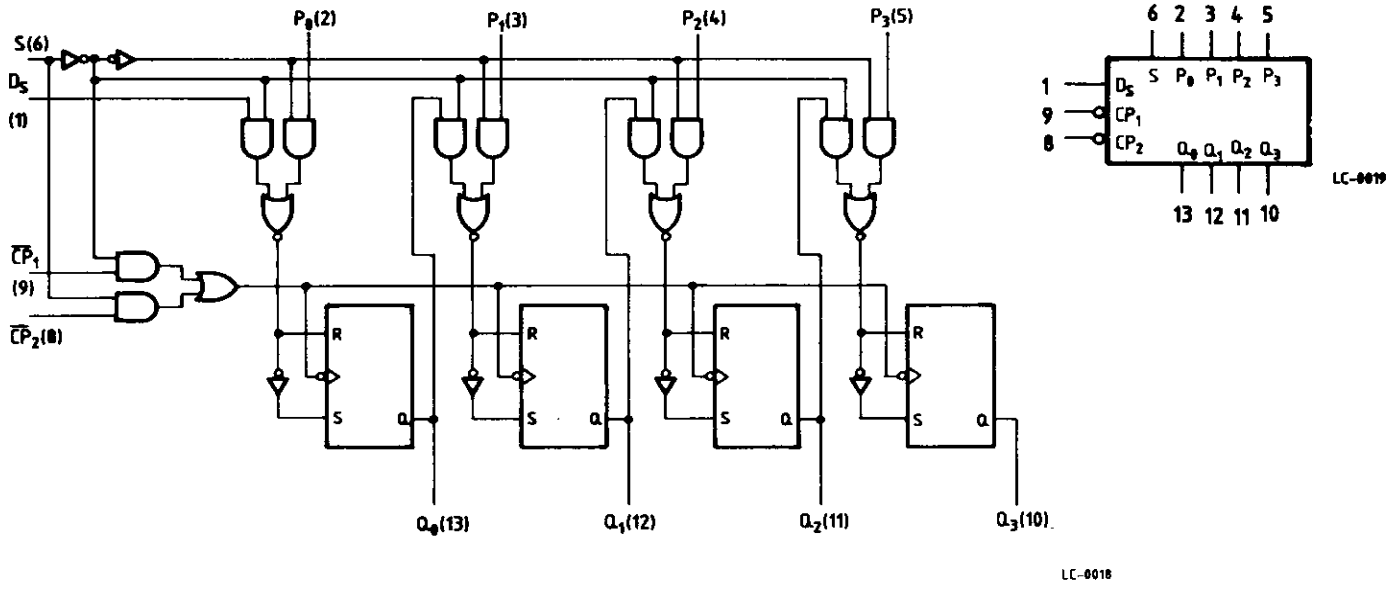


NC = No Internal Connection

PIN NAMES

S	Mode Control Input
D_S	Serial Data Input
P_0-P_3	Parallel Data Inputs
$\overline{CP}_1$	Serial Clock (Active LOW Going Edge) Input
$\overline{CP}_2$	Parallel Clock (Active LOW Going Edge) Input
Q_0-Q_3	Parallel Outputs

LOGIC DIAGRAM AND LOGIC SIMBOL



( ) = Pin numbers, V_{CC} = Pin 14, GND = Pin 7

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	Input Voltage, Applied to Input	−0.5 to 15	V
V_O	Output Voltage, Applied to Output	−0.5 to 10	V
I_I	Input Current, Into Inputs	−30 to 5	mA
I_O	Output Current, Into Outputs	60	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS95BD2	4.5 V	5.0 V	5.5 V	−55°C to +125°C
T74LS95BXX	4.75 V	5.0 V	5.25 V	0°C to +70°C

XX = package type.

TRUTH TABLE

OPERATING MODE	INPUTS					OUTPUTS			
	S	$\overline{CP}_1$	$\overline{CP}_2$	D_S	P_n	Q_0	Q_1	Q_2	Q_3
Shift	L	⌐└	X	l	X	L	q_0	q_1	q_2
	L	⌐└	X	h	X	H	q_0	q_1	q_2
Parallel Load	H	X	⌐└	X	p_n	p_0	p_1	p_2	p_3
Mode Change	⌐└	L	L	X	X	No Change			
	└⌐	L	L	X	X	No Change			
	⌐└	H	L	X	X	No Change			
	└⌐	H	L	X	X	Undetermined			
	⌐└	L	H	X	X	Undetermined			
	└⌐	L	H	X	X	No Change			
	⌐└	H	H	X	X	Undetermined			
	└⌐	H	H	X	X	No Change			

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
l = LOW Voltage Level one set-up time prior to the HIGH to LOW clock transition.
h = HIGH Voltage Level one set-up time prior to the HIGH to LOW clock transition.
p_n = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock Transition

FUNCTIONAL DESCRIPTION

The LS95B is a 4-Bit Shift Register with serial and parallel synchronous operating modes. It has a Serial (D_S) and four Parallel (P_0-P_3) Data inputs and four Parallel Data outputs (Q_0-Q_3). The serial or parallel mode of operation is controlled by a Mode Control input (S) and two Clock inputs ($\overline{CP}_1$) and ($\overline{CP}_2$). The serial (right-shift) or parallel data transfers occur synchronous with the HIGH to LOW transition of the selected clock input.

When the Mode Control input (S) is HIGH, $\overline{CP}_2$ is enabled. A HIGH to LOW transition on enabled $\overline{CP}_2$ transfers parallel data from the P_0-P_3 inputs to the Q_0-Q_3 outputs.

When the Mode Control input (S) is LOW, $\overline{CP}_1$ is enable. A HIGH to LOW transition on enabled $\overline{CP}_1$ transfers the data from seral input (D_S) to Q_0 and shifts the data in Q_0 to Q_1, Q_1 to Q_2, and Q_2 to Q_3 respectively (righ-shift). A left-shift is accomplished by externally connecting Q_3 to P_2, Q_2 to P_1, and Q_1 to P_0, and operating the LS95B in the parallel mode (S = HIGH).

For normal operation, S should only change states when both Clock inputs are LOW. However, changing S from LOW to HIGH while $\overline{CP}_2$ is HIGH, or changing S from HIGH to LOW while $\overline{CP}_1$ is HIGH and $\overline{CP}_2$ is LOW will not cause any changes on the register outputs.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits			Test Conditions (Note 1)		Units
			Min.	Typ.	Max.			
V_{IH}	Input HIGH Voltage		2.0			Guaranteed input HIGH Threshold Voltage for all Inputs		V
V_{IL}	Input LOW Voltage	54			0.7	Guaranteed input LOW Threshold Voltage for all Inputs		V
		74			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V_{CC} = MIN, I_{IN} = −18mA		V
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V_{CC} = MIN, I_{OH} = −400μA, V_{IN} = V_{IH} or V_{IL} per Truth Table		V
		74	2.7	3.4				
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	I_{OL} = 4.0mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74		0.35	0.5	I_{OL} = 8.0mA		
I_{IH}	Input HIGH Current D_S,P_0,P_1,P_2,P_3,$\overline{CP}_1$,$\overline{CP}_2$				20	V_{CC} = MAX, V_{IN} = 2.7V		μA
	D_S,P_0,P_1,P_2,P_3,$\overline{CP}_1$,$\overline{CP}_2$ S				40			
	D_S,P_0,P_1,P_2,P_3,$\overline{CP}_1$,$\overline{CP}_2$				0.1	V_{CC} = MAX, V_{IN} = 7.0V		mA
	S				0.2			
I_{IL}	Input LOW Current D_S,P_0,P_1,P_2,P_3,$\overline{CP}_1$,$\overline{CP}_2$				−0.4	V_{CC} = MAX, V_{IN} = 0.4V		mA
	S				−0.8			
I_{OS}	Output Short Circuit Current (Note 2)		−20		−100	V_{CC} = MAX, V_{OUT} = 0V		mA
I_{CC}	Power Supply Current			13	21	V_{CC} = MAX		mA

AC CHARACTERISTICS: T_A = 25°C

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
f_{MAX}	Shift Frequency	25	36		Fig. 1	V_{CC} = 5.0V, C_L = 15pF	MHz
t_{PLH}	Propagation Delay,		18	27	Fig. 2		ns
t_{PHL}	Clock to Output		21	32			

Notes:
1) For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2) Not more than one output should be shorted at a time.
3) Typical values are at V_{CC} = 5.0V, T_A = 25°C

AC SET-UP REQUIREMENTS: $T_A = 25°C$

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
t_W(CP)	Clock Pulse Width	25			Fig. 1	$V_{CC} = 5.0V$ $C_L = 15pF$	ns
t_s(Data)	Set-up Time, Data to Clock	20			Fig. 1		ns
t_h(Data)	Hold Time, Data to Clock	20					ns
t_{sL}	Set-up Time LOW Mode Control to Clock	20			Fig. 1		ns
t_{hL}	Hold Time, LOW Mode Control to Clock	0					ns
t_{sH}	Set-up Time, HIGH Mode Control to Clock	20			Fig. 1		ns
t_{hH}	Hold Time, HIGH Mode Control to Clock	0					ns

SET-UP TIME (t_s) - is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transfered to the output.

HOLD TIME (t_h) - is defined as the minimum time following the clock transition from HIGH to LOW that the logic level must be mantained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be relased prior to the clock transition from HIGH to LOW and still be recognized.

AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 1

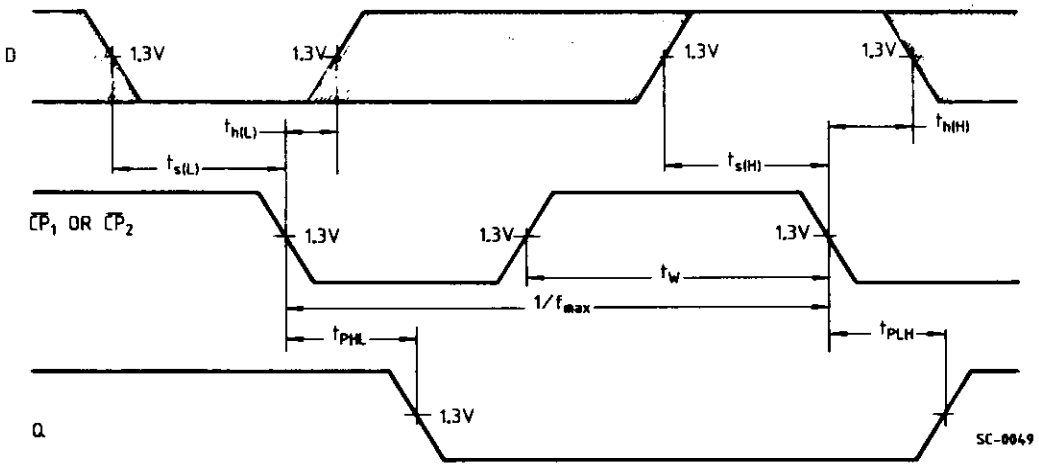
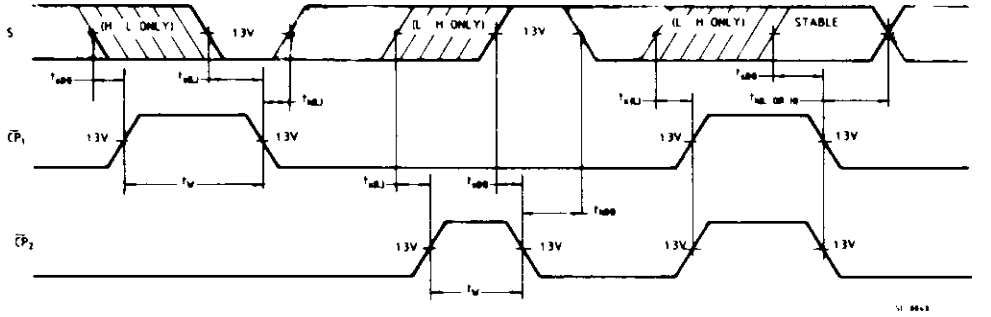


Fig. 2



* The Data Input is (D_S for $\overline{CP}_1$) or (P_n for $\overline{CP}_2$).