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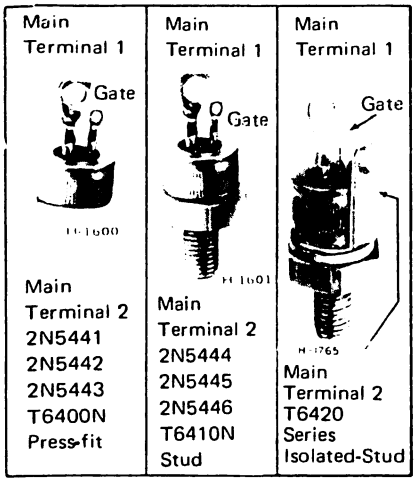
Thyristors
2N5441 2N5442 2N5443
2N5444 2N5445 2N5446
T6400 T6410 T6420 Series



40-A Silicon Triacs

Press-Fit, Stud, and Isolated-Stud Packages

For 120-V Line Operation . . . 2N5441, 2N5444, T6420B
For 240-V Line Operation . . . 2N5442, 2N5445, T6420D
For High-Voltage Operation . . 2N5443, 2N5446, T6420M
T6400N, T6410N, T6420N

Features:

- di/dt Capability = 100 A/μs
- Shorted-Emitter, Center-Gate Design
- Low Switching Losses
- Low On-State Voltage at High Current Levels
- Low Thermal Resistance

triacs are gate-controlled, full-wave silicon ac switches. They are designed to switch from an off-state to an on-state for either polarity of applied voltage with positive or negative gate-triggering voltages.

MAXIMUM RATINGS, *Absolute-Maximum Values:*
For Operation with Sinusoidal Supply Voltage at Frequencies up to 50/60 Hz and with Resistive or Inductive Load.

		2N5441 2N5444 T6420B	2N5442 2N5445 T6420D	2N5443 2N5446 T6420M	T6400N T6410N T6420N	
***REPETITIVE PEAK OFF-STATE VOLTAGE:•** Gate open, T_J = -65 to 110°C	V_{DROM}	200	400	600	800	V
RMS ON-STATE CURRENT (Conduction angle = 360°): Case temperature	$I_{T(RMS)}$					
* T_C = 70°C (Press-fit types)		40				A
* = 65°C (Stud types)		40				A
= 60°C (Isolated-stud types)		40				A
For other conditions		See *Fig. 3*				
PEAK SURGE (NON-REPETITIVE) ON-STATE CURRENT: For one cycle of applied principal voltage	I_{TSM}					
* 60 Hz (sinusoidal)		300				A
50 Hz (sinusoidal)		265				A
For more than one cycle of applied principal voltage		See *Fig. 4*				
RATE OF CHANGE OF ON-STATE CURRENT: V_{DM} = V_{DROM}, I_{GT} = 200 mA, t_r = 0.1 μs (See *Fig. 13*)	di/dt	100				A/μs
FUSING CURRENT (for Triac Protection): T_J = -65 to 110°C, t = 1.25 to 10 ms	I^2t	350				A^2s
***PEAK GATE-TRIGGER CURRENT:▪** For 1 μs max., See *Fig. 7*	I_{GTM}	12				A
***GATE POWER DISSIPATION:** PEAK (For 10 μs max., $I_{GTM} \leq$ 4 A, See *Fig. 7*)	P_{GM}	40				W
AVERAGE	$P_{G(AV)}$	0.75				W
***TEMPERATURE RANGE:▲** Storage	T_{stg}	-65 to 150				°C
Operating (Case)	T_C	-65 to 110				°C
***TERMINAL TEMPERATURE** (During soldering): For 10 s max. (terminals and case)	T_T	225				°C

* In accordance with JEDEC registration data format (JS-14, RDF2) filed for the JEDEC (2N-Series) types.
• For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.
▪ For either polarity of gate voltage (V_G) with reference to main terminal 1.
▲ For temperature measurement reference point, see Dimensional Outline.

ELECTRICAL CHARACTERISTICS

At Maximum Ratings Unless Otherwise Specified and at Indicated Case Temperature (T_C)

CHARACTERISTIC	SYMBOL	LIMITS FOR ALL TYPES UNLESS OTHERWISE SPECIFIED			UNITS
		MIN.	TYP.	MAX.	
Peak Off-State Current:♦ Gate open, T_J = 110°C, V_{DROM} = Max. rated value	I_{DROM}	–	0.2	4*	mA
Maximum On-State Voltage:♦ For i_T = 100 A (peak), T_C = 25°C	V_{TM}	–	1.7	2	V
For i_T = 56 A (peak), T_C = 25°C		–	1.5	1.85*	
DC Holding Current:♦ Gate open, Initial principal current = 500 mA (dc), v_D = 12V:					
T_C = 25°C	I_{HO}	–	25	60	mA
T_C = -65°C		–	–	100*	
For other case temperatures		See *Fig. 6*			
Critical Rate of Rise of Commutation Voltage:♦ For v_D = V_{DROM}, $I_{T(RMS)}$ = 40 A, commutating di/dt = 22 A/ms, gate unenergized, (See *Fig. 14*):					
T_C = 70°C (Press-fit types)	dv/dt	5*	30	–	v/μs
= 65°C (Stud types)		5*	30	–	
= 60°C (Isolated-stud types)		5	30	–	
Critical Rate of Rise of Off-State Voltage:♦ For v_D = V_{DROM}, exponential voltage rise, gate open, T_C = 110°C:					
2N5441, 2N5444, T6420B	dv/dt	50*	200	–	V/μs
2N5442, 2N5445, T6420D		30*	150	–	
2N5443, 2N5446, T6420M		20*	100	–	
T6400N, T6410N, T6420N		10	75	–	
DC Gate-Trigger Current:♦♦ For v_D = 12 V (dc), R_L = 30 Ω, T_C = 25°C	I_{GT}				mA
Mode I+ V_{MT2} positive V_G positive		–	15	50	
Mode III- V_{MT2} negative V_G negative		–	20	50	
Mode I- V_{MT2} positive V_G negative		–	30	80	
Mode III+ V_{MT2} negative V_G positive		–	40	80	
For v_D = 12 V (dc), R_L = 30 Ω, T_C = -65°C					
Mode I+ V_{MT2} positive V_G positive		–	–	125*	
Mode III- V_{MT2} negative V_G negative		–	–	125*	
Mode I- V_{MT2} positive V_G negative		–	–	240*	
Mode III+ V_{MT2} negative V_G positive		–	–	240*	
For other case temperatures		See *Figs. 8 & 9*			
DC Gate-Trigger Voltage:♦♦ For v_D = 12 V (dc), R_L = 30 Ω,					
T_C = 25°C	V_{GT}	–	1.35	2.5	V
= -65°C		–	1.8	3.4*	
For other case temperatures		See *Fig. 10*			
For v_D = V_{DROM}, R_L = 125 Ω, T_C = 110°C		0.2	–	–	
Gate-Controlled Turn-On Time: (Delay Time + Rise Time) For v_D = V_{DROM}, I_{GT} = 200 mA, t_r = 0.1 μs, i_T = 60 A (peak), T_C = 25°C (See *Figs. 11 & 15*)	t_{gt}	–	1.7	3	μs
Thermal Resistance, Junction-to-Case: Steady-State					
Press-fit types	$R_{\theta JC}$	–	–	0.8*	°C/W
Stud types		–	–	0.9*	
Isolated-stud types		–	–	1	
Transient (Press-fit & stud types)		See *Fig. 12*			

* In accordance with JEDEC registration data format (JS-14, RDF 2) filed for the JEDEC (2N-Series) types.

♦ For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.

♦ For either polarity of gate voltage (V_G) with reference to main terminal 1.

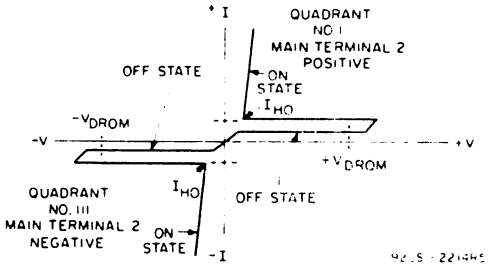


Fig. 1—Principal voltage-current characteristic.

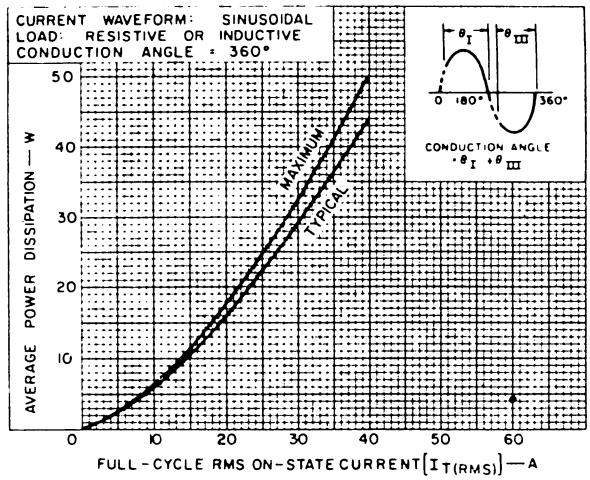


Fig. 2—Power dissipation vs. on-state current.

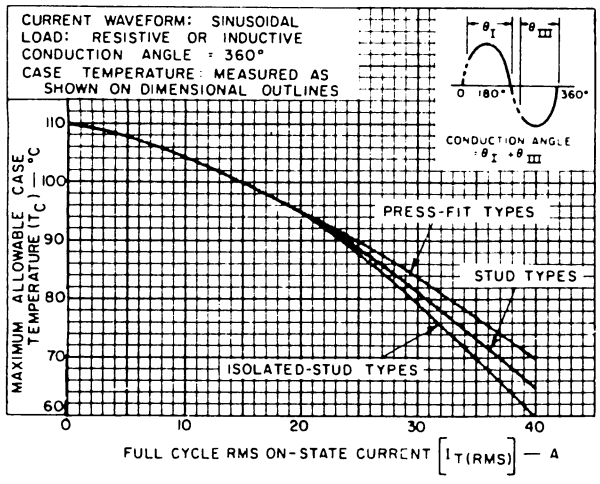


Fig. 3—Maximum allowable case temperature vs. on-state current.

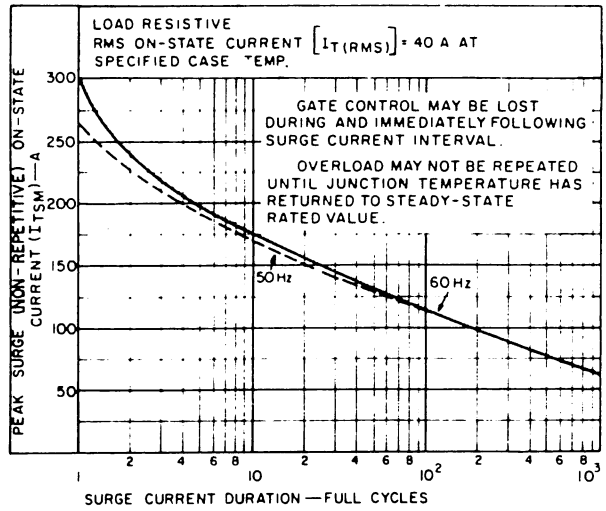


Fig. 4—Peak surge on-state current vs. surge current duration.

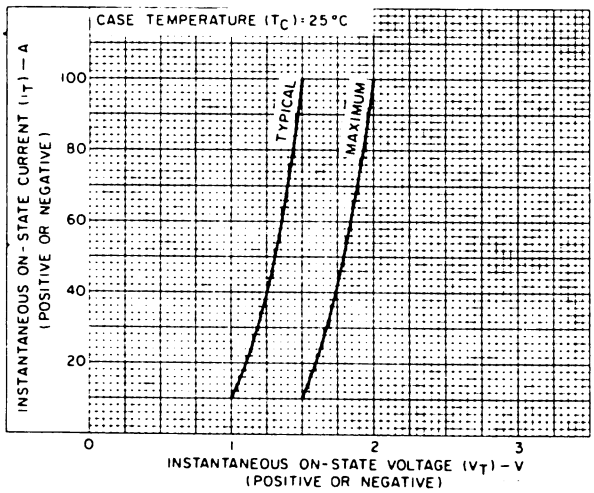


Fig. 5—On-state current vs. on-state voltage.

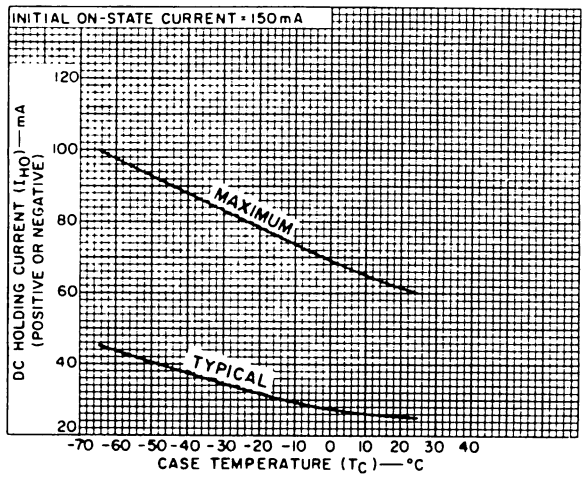


Fig. 6—DC holding current vs. case temperature.

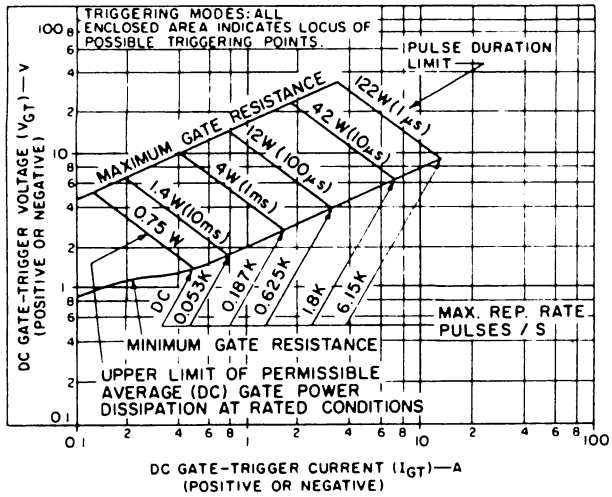


Fig.7—Gate-trigger characteristics and limiting conditions for determination of permissable gate-trigger pulses.

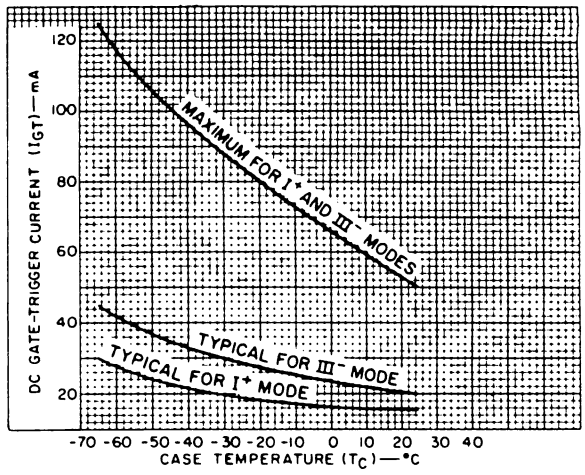


Fig.8—DC gate-trigger current vs. case temperature (I^+ & III^- modes).

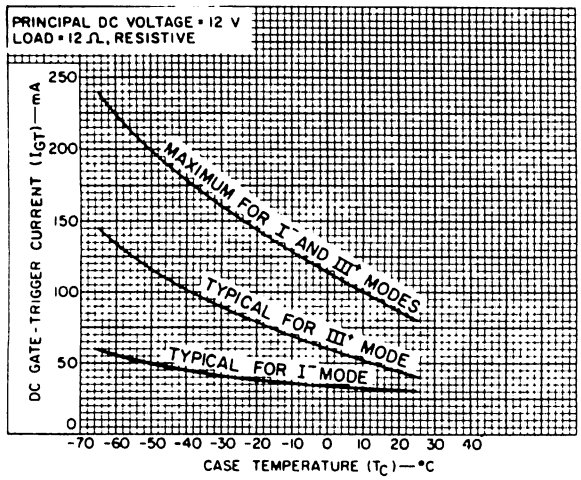


Fig.9—DC gate-trigger current vs. case temperature (I^- & III^+ modes).

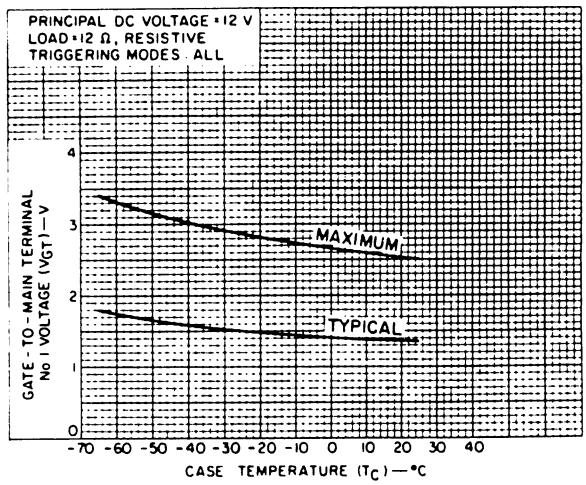


Fig.10—DC gate-trigger voltage vs. case temperature.

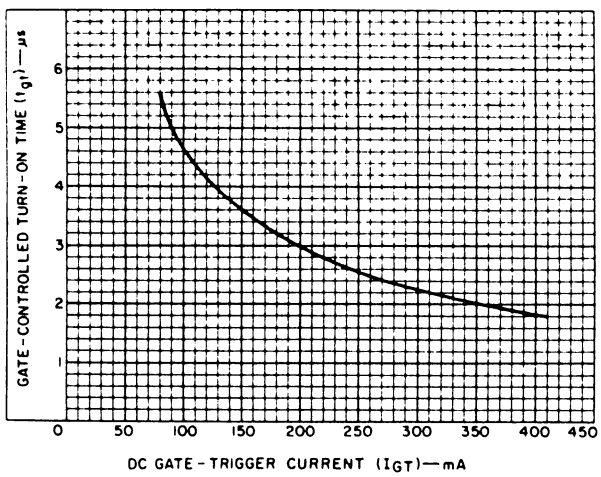


Fig.11—Turn-on time vs. gate-trigger current.

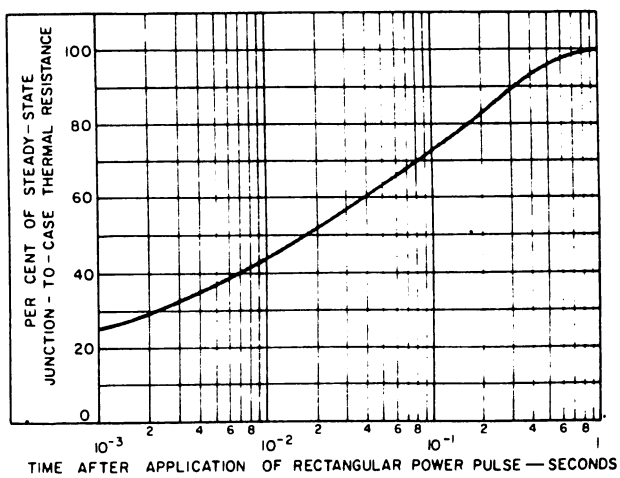


Fig.12—Transient junction-to-case thermal resistance vs. time for press-fit and stud types.

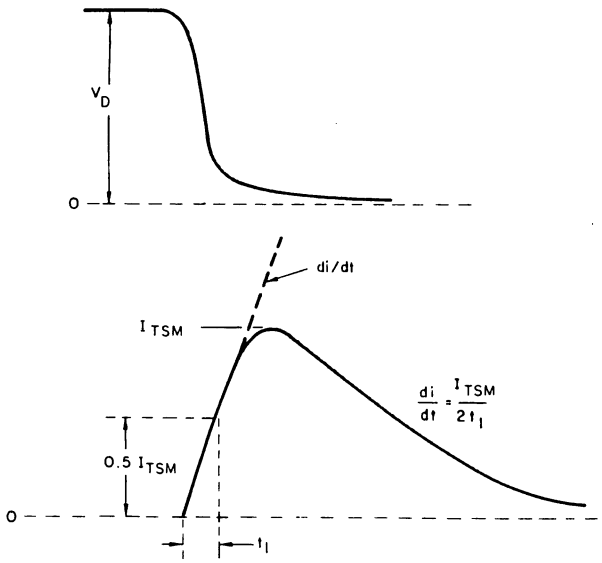


Fig. 13—Rate of change of on-state current with time (defining di/dt).

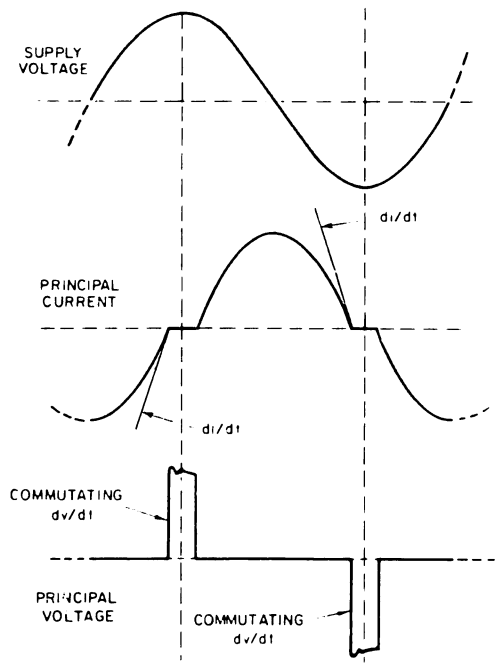


Fig. 14—Relationship between supply voltage and principal current (inductive load) showing reference points for definition of commutating voltage (dv/dt).

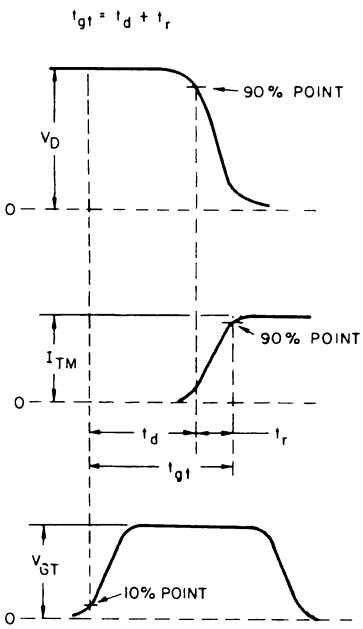


Fig. 15—Relationship between off-state voltage, on-state current, and gate-trigger voltage showing reference points for definition of turn-on time (t_{gt}).

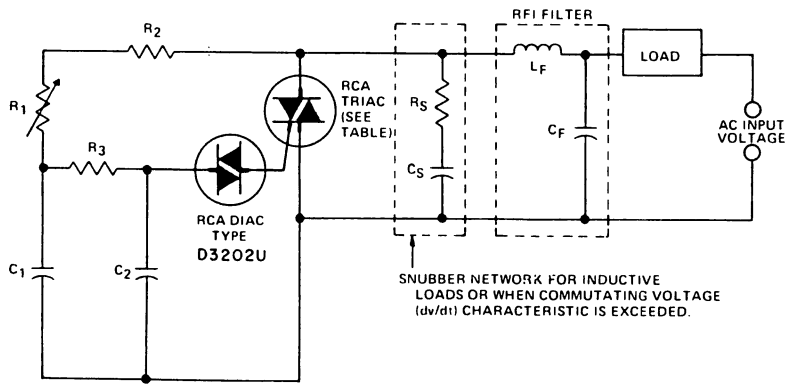


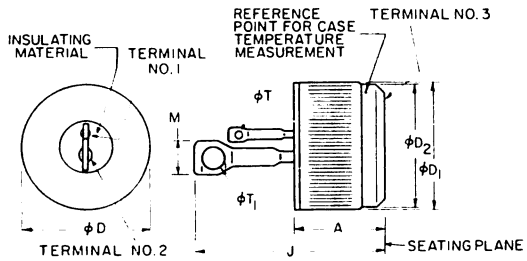
Fig. 16—Typical phase-control circuit for lamp dimming, heat control, and universal-motor speed control.

AC INPUT VOLTAGE		120V 60Hz	240V 60Hz	240V 50Hz
C_1		0.1μF 200V	0.1μF 400V	0.1μF 400V
C_2		0.1μF 100V	0.1μF 100V	0.1μF 100V
R_1		100KΩ 1/2W	200KΩ 1W	250KΩ 1W
R_2		2.2KΩ 1/2W	3.3KΩ 1/2W	3.3KΩ 1/2W
R_3		15KΩ 1/2W	15KΩ 1/2W	15KΩ 1/2W
SNUBBER NETWORK FOR 40-A (RMS)* INDUCTIVE LOAD	C_S	0.18-0.22μF 200V	0.18-0.22μF 400V	0.18-0.22μF 400V
	R_S	330-390Ω 1/2W	330-390Ω 1/2W	330-390Ω 1/2W
RFI FILTER	C_F*	0.1μF 200V	0.1μF 400V	0.1μF 400V
	L_F*	100μH	200μH	200μH
RCA TRIACS		2N5441 2N5444 T6420B	2N5442 2N5445 T6420D	2N5442 2N5445 T6420D

* For other RMS current values refer to RCA Application Note AN-4745.

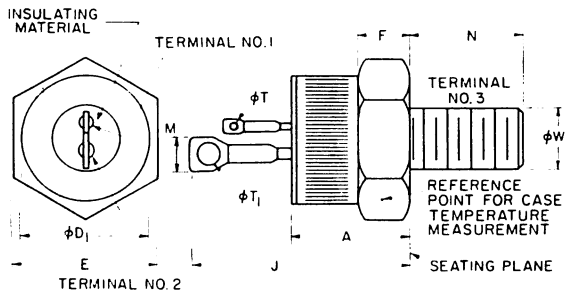
* Typical values for lamp dimming circuits.

DIMENSIONAL OUTLINE FOR TYPES 2N5441, 2N5442, 2N5443, T6400N PRESS-FIT



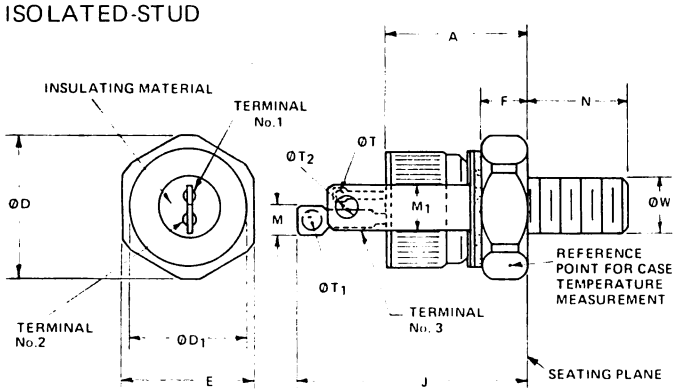
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	–	0.380	–	9.65	
ϕD	0.501	0.510	12.73	12.95	
ϕD_1	–	0.505	–	12.83	
ϕD_2	0.465	0.475	11.81	12.07	
J	0.825	1.000	20.95	25.40	
M	0.215	0.225	5.46	5.71	
ϕT	0.058	0.068	1.47	1.73	
ϕT_1	0.138	0.148	3.51	3.75	

DIMENSIONAL OUTLINE FOR TYPES 2N5444, 2N5445, 2N5446, T6410N STUD



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.330	0.505	8.4	12.8	
ϕD_1	–	0.544	–	13.81	
E	0.544	0.562	13.82	14.28	
F	0.113	0.200	2.87	5.08	
J	0.950	1.100	24.13	27.94	
M	0.215	0.225	5.46	5.71	
N	0.422	0.453	10.72	11.50	
ϕT	0.058	0.068	1.47	1.73	
ϕT_1	0.138	0.148	3.51	3.75	
ϕW	¼-28	UNF-2A	¼-28	UNF-2A	

DIMENSIONAL OUTLINE FOR T6420 SERIES ISOLATED-STUD



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	–	0.673	–	17.09	
ϕD	0.604	0.614	15.34	15.59	
ϕD_1	0.501	0.505	12.72	12.82	
E	0.551	0.557	13.99	14.14	
F	0.100	0.110	2.54	2.79	
J	–	1.298	–	32.96	
M	0.210	0.230	5.33	5.84	
M_1	0.200	0.210	5.08	5.33	
N	0.422	0.452	10.72	11.48	
ϕT	0.058	0.068	1.47	1.73	
ϕT_1	0.138	0.148	3.51	3.75	
ϕT_2	0.138	0.148	3.51	3.75	
ϕW	¼-28	UNF-2A	¼-28	UNF-2A	

TERMINAL CONNECTIONS

No. 1–Gate
No. 2–Main Terminal 1
Case, No. 3–Main Terminal 2