T6401, T6411, T6421 Series

File Number **459**

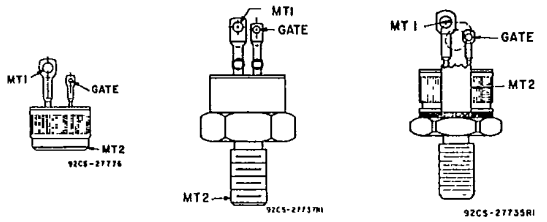
30-A Silicon Triacs

For Power-Switching and Power Control

Features:

- *800V, 125 Deg. C T_J Operating*
- *High dv/dt and di/dt Capability*
- *Low Switching Losses*
- *High Pulse Current Capability*
- *Low Forward and Reverse Leakage*
- *Sipos Oxide Glass Multilayer Passivation System*
- *Advanced Unisurface Construction*
- *Precise Ion Implanted Diffusion Source*

TERMINAL DESIGNATIONS



PRESS-FIT TYPES T6401 SERIES | **STUD TYPES T6411 SERIES** | **ISOLATED-STUD TYPES T6421 SERIES**

These RCA triacs are gate-controlled full-wave silicon ac switches. They are designed to switch from an off-state to an on-state for either polarity of applied voltage with positive or negative gate triggering voltages.

These triacs are intended for control of ac loads in applications such as heating controls, motor controls, arc-welding equipment, light dimmers, and power switching systems. They can also be used in air-conditioning and photocopying equipment.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		T6401B T6411B T6421B	T6401D T6411D T6421D	T6401M T6411M T6421M	T6401N T6411N —	
REPETITIVE PEAK OFF-STATE VOLTAGE:*						
Gate open, T_J = -50 to 125° C	V_{DROM}	200	400	600	800	V
RMS ON-STATE CURRENT (Conduction angle = 360°):	$I_{T(RMS)}$					
Case temperature						
T_C = 90° C (Press-fit types)		30				A
= 85° C (Stud types)		30				A
= 80° C (Isolated-stud types)		30				A
For other conditions		See Fig. 3				
PEAK SURGE (NON-REPETITIVE) ON-STATE CURRENT:	I_{TSM}					
For one cycle of applied principal voltage						
60 Hz (sinusoidal)		300				A
50 Hz (sinusoidal)		265				A
For more than one cycle of applied principal voltage		See Fig. 4				
RATE-OF-CHANGE OF ON-STATE CURRENT:	di/dt					
$V_{DM} = V_{DROM}$, I_{GT} = 200 mA, t_r = 0.1 μs (See Fig. 13)		100				A/μs
FUSING CURRENT (for triac protection):						
T_J = -40 to 100°C, t = 1.25 to 10 ms	I^2t	450				A^2s
PEAK GATE-TRIGGER CURRENT:■	I_{GTM}					
For 1 μs max., See Fig. 7		12				A
GATE POWER DISSIPATION:						
PEAK (For 1 μs max., $I_{GTM} \leq 4$ A, See Fig. 7)	P_{GM}	40				W
AVERAGE	$P_{G(AV)}$	0.75				W
TEMPERATURE RANGE:▲						
Storage	T_{stg}	-65 to 150				°C
Operating (Case)	T_C	-65 to 100				°C
TERMINAL TEMPERATURE (During soldering):	T_T					
For 10 s max. (terminals and case)		225				°C
STUD TORQUE:						
Recommended		35				in-lb
Maximum (DO NOT EXCEED)		50				in-lb

*For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.
■For either polarity to gate voltage (V_G) with reference to main terminal 1.
▲For temperature measurement reference point, see Dimensional Outline.

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ELECTRICAL CHARACTERISTICS, *At Maximum Ratings Unless Otherwise Specified, and at Indicated Temperature*

CHARACTERISTIC	SYMBOL	LIMITS For All Types Unless Otherwise Specified			UNITS
		Min.	Typ.	Max.	
Peak Off-State Current:•					
Gate open, T_J = 125°C, V_{DROM} = Max. rated value	I_{DROM}	—	0.2	4	mA
Maximum On-State Voltage:•					
For i_T = 100 A (peak), T_C = 25°C	V_{TM}	—	2.1	2.5	V
DC Holding Current:•					
Gate open, Initial principal current = 150 mA (DC), v_D = 12V:					
T_C = 25°C	I_{HO}	—	25	60	mA
For other case temperatures			See Fig. 6		
Critical Rate-of-Rise of Commutation Voltage:•					
For $v_D = V_{DROM}$, $I_{T(RMS)}$ = 30 A, commutating di/dt = 16 A/ms, gate unenergized (See Fig. 14):					
T_C = 90°C (Press-fit types)		3	20	—	
= 85°C (Stud types)	dv/dt	3	20	—	V/μs
= 80°C (Isolated-stud types)		3	20	—	
Critical Rate-of-Rise of Off-State Voltage:•					
For $v_D = V_{DROM}$, exponential voltage rise, gate open, T_C = 125°C:					
T6401B, T6411B, T6421B		40	200	—	
T6401D, T6411D, T6421D	dv/dt	25	150	—	V/μs
T6401M, T6411M, T6421M		20	100	—	
T6401N, T6411N		10	50		
DC Gate-Trigger Current:•■					
For v_D = 12 V (DC), R_L = 30 Ω, T_C = 25°C	Mode I+ positive positive	—	15	50	
	III- negative negative	—	20	50	
	I- positive negative	—	30	80	mA
	III+ negative positive	—	40	80	
	I_{GT}				
For other case temperatures			See Figs. 8 & 9		
DC Gate-Trigger Voltage:•■					
For v_D = 12 V(DC), R_L = 30 Ω, T_C = 25°C		—	1.35	2.5	
For other case temperatures	V_{GT}		See Fig. 10		V
For $v_D = V_{DROM}$, R_L = 125 Ω, T_C = 100°C		0.2	—	—	
Gate-Controlled Turn-On Time: (Delay Time = Rise Time) For $v_D = V_{DROM}$, I_{GT} = 200 mA, t_r = 0.1 μs, i_T = 45 A (peak), T_C = 25°C (See Figs. 7 & 12)	t_{gt}	—	1.7	3	μs
Thermal Resistance, Junction-to-Case:					
Steady-State					
Press-fit types		—	—	0.8	
Stud	$R_{\theta JC}$	—	—	0.9	°C/W
Transient (Press-fit & stud types)			See Fig. 2		
Thermal Resistance, Junction-to-Hex (Stud, See Dim. Outline):					
Steady-State (Isolated-stud types)	$R_{\theta JH}$	—	—	1	

•For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.
■For either polarity of gate voltage (V_G) with reference to main terminal 1.

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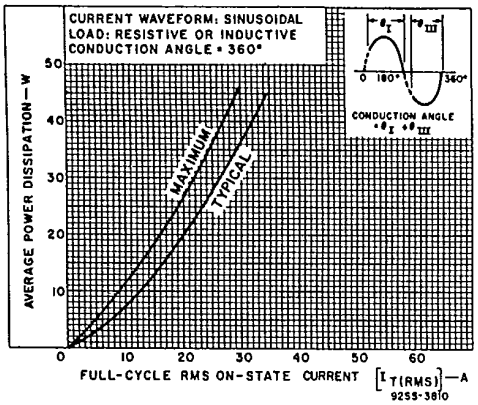

Fig. 1 — Power dissipation vs. on-state current.

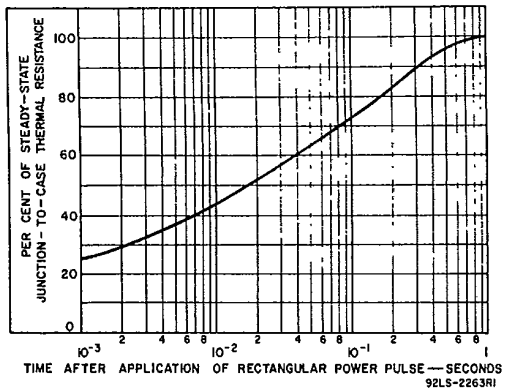

Fig. 2 — Transient junction-to-case thermal resistance vs. time.

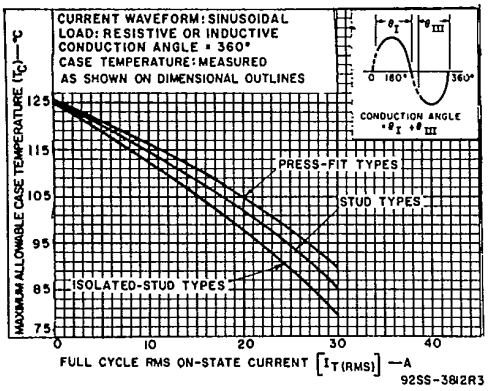

Fig. 3 — Maximum allowable case temperature vs. on-state current.

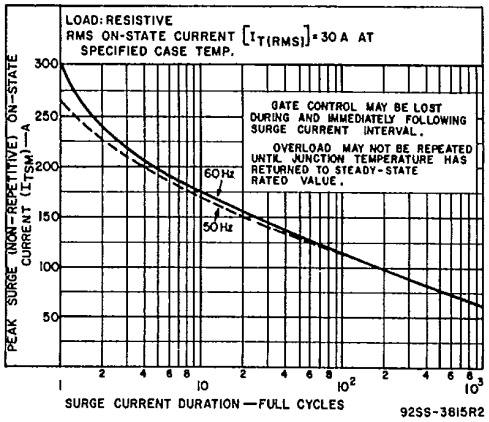

Fig. 4 — Peak surge on-state current vs. surge current duration.

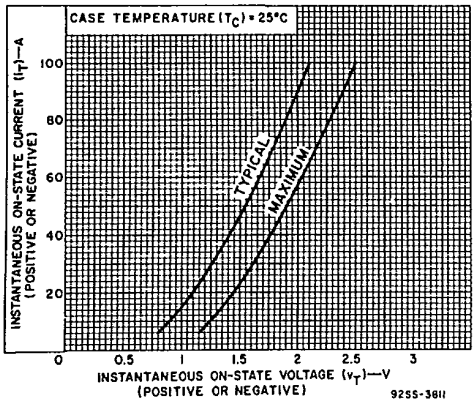

Fig. 5 — On-state current vs. on-state voltage.

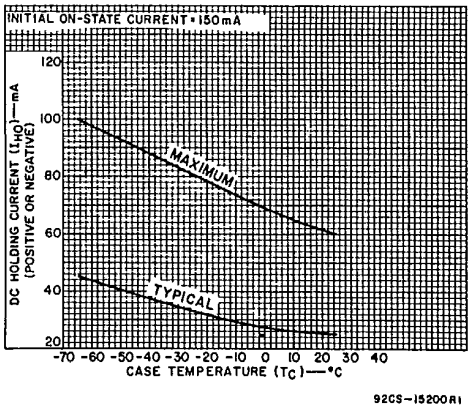

Fig. 6 — DC holding current vs. case temperature.

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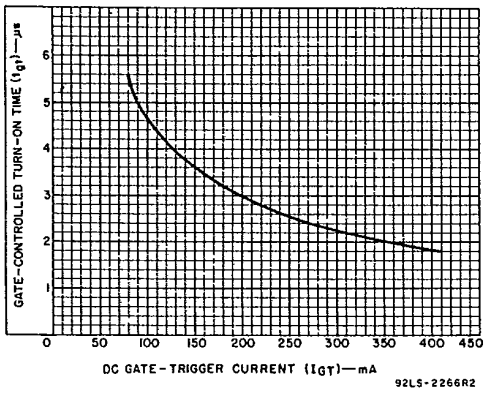

Fig. 7 — Turn-on time vs. gate trigger current.

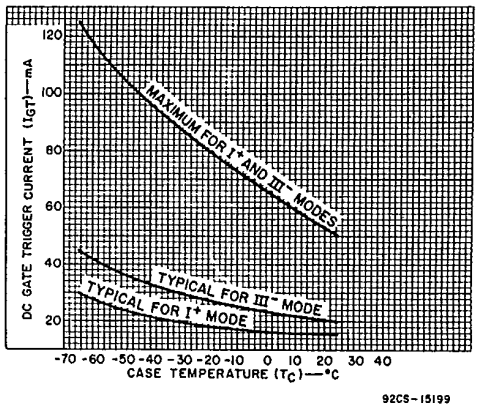

Fig. 8 — DC gate-trigger current vs. case temperature (1⁺ and III⁻ modes).

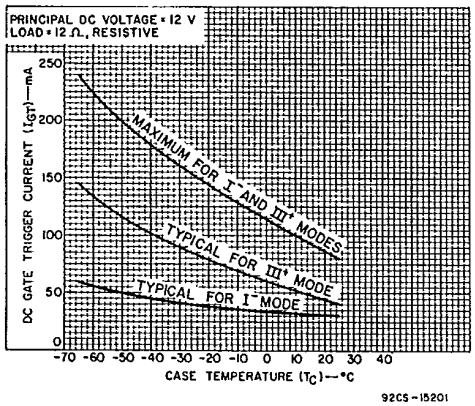

Fig. 9 — DC gate-trigger current vs. case temperature (1⁻ and III⁺ modes).

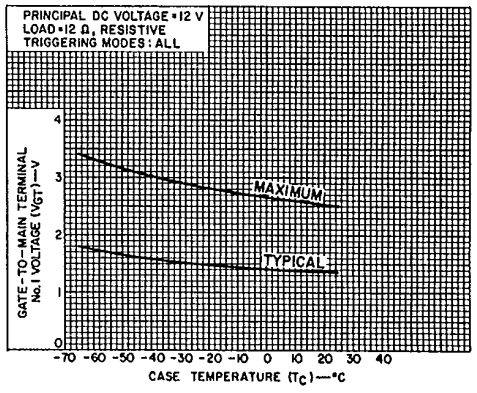

Fig. 10 — DC gate-trigger voltage vs. case temperature.

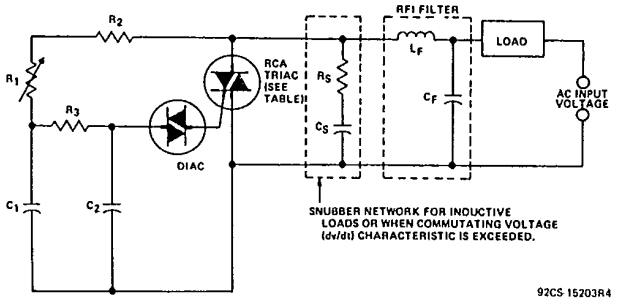

Fig. 11 — Typical phase-control circuit for lamp dimming, heat control, and universal-motor speed control.

AC INPUT VOLTAGE		120V 60Hz	240V 60Hz	240V 50Hz
C_1		0.1μF 200V	0.1μF 400V	0.1μF 400V
C_2		0.1μF 100V	0.1μF 100V	0.1μF 100V
R_1		100KΩ 1/2W	200KΩ 1W	250KΩ 1W
R_2		2.2KΩ 1/2W	3.3KΩ 1/2W	3.3KΩ 1/2W
R_3		15KΩ 1/2W	15KΩ 1/2W	15KΩ 1/2W
SNUBBER NETWORK	C_S	0.1μF 200V	0.1μF 400V	0.1μF 400V
	R_S	100Ω 1/2W	100Ω 1/2W	100Ω 1/2W
RFI FILTER	C_F*	0.1μF 200V	0.1μF 400V	0.1μF 400V
	L_F*	100μH	200μH	200μH
RCA TRIACS		T6401B T6411B T6421B	T6401D T6411D T6421D	T6401D T6411D T6421D

*Typical values for lamp dimming circuits.

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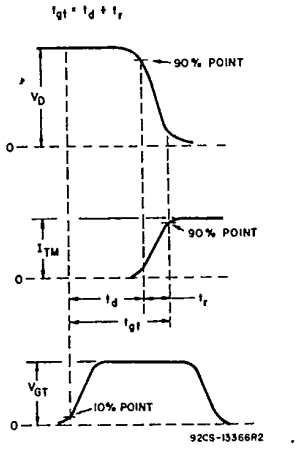

Fig. 12 — Relationship between off-state voltage, on-state current, and gate-trigger voltage showing reference points for definition of turn-on time (t_{gt}).

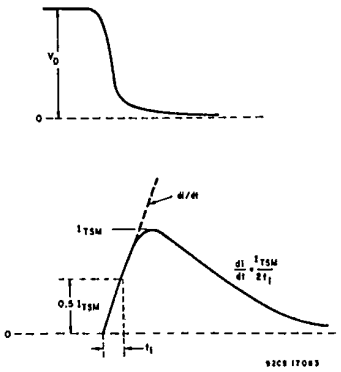

Fig. 13 — Rate of change of on-state current with time (defining di/dt).

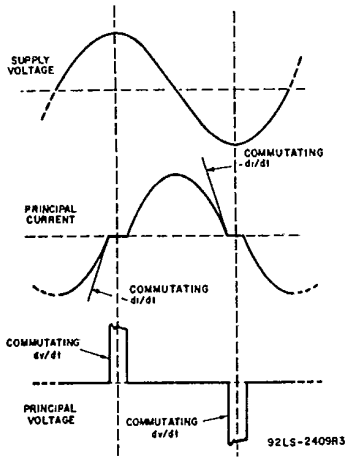

Fig. 14 — Relationship between supply voltage and principle current (inductive load) showing reference points for definition of commutating voltage (dv/dt).

MOUNTING CONSIDERATIONS

Mounting of press-fit package types depends upon an interference fit between the thyristor case and the heat sink. As the thyristor is forced into the heat-sink hole, metal from the heat sink flows into the knurl voids of the thyristor case. The resultant close contact between the heat sink and the thyristor case assures low thermal and electrical resistances.

A recommended mounting method shows press-fit knurl and heat-sink hole dimensions. If these dimensions are maintained, a "worst-case" condition of 0.0085 in. (0.2159 mm) interference fit will allow press-fit insertion below the maximum allowable insertion force of 800 pounds. A slight chamfer in the heat-sink hole will help center and guide the press-fit package properly into the heat sink. The insertion tool should be a hollow shaft having an inner diameter of 0.380 ± 0.010 in. (9.65 ± 0.254 mm) and an outer diameter of 0.500 in. (12.70 mm). These dimensions provide sufficient clearance for the leads and assure that no direct force will be applied to the glass seal of the thyristor.

The press-fit package is not restricted to a single mounting arrangement; direct soldering and the use of epoxy adhesives have been successfully employed. The press-fit case is tin-plated to facilitate direct soldering to the heat sink. A 60-40 solder should be used and heat should be applied only long enough to allow the solder to flow freely.