Model Name: T645HW03 V0

Issue Date : 2010/7/20

( )Preliminary Specifications
(*)Final Specifications

Customer Signature	Date	AUO	Date
Approved By		Approval By PM Director *Yenting Chiu*	
Note		Reviewed By RD Director *Eugene Chen* Reviewed By Project Leader *Hank Chiu*	
		Prepared By PM *Ryan Chung*	

Contents

Record of Revision

Version	Date	Page	Description
1.0	2010/07/20		First release

1. General Description

This specification applies to the 64.5 inch Color TFT-LCD Module T645HW03 V0. This LCD module has a TFT active matrix type liquid crystal panel 1920 x 1080 pixels, and diagonal size of 64.5 inch. This module supports 1920 x 1080 mode. Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 10-bit gray scale signal for each dot.

The T645HW03 V0 has been designed to apply the 10-bit 4 channel LVDS interface method. It is intended to support displays where high brightness, wide viewing angle, high color saturation, and high color depth are very important.

*** General Information**

Items	Specification	Unit	Note
Active Screen Size	64.53	inch	
Display Area	1428.48 (H) x 803.52 (V)	mm	
Outline Dimension	1508.0(H) x 878.0(V) x 60.0(D)	mm	
Driver Element	a-Si TFT active matrix		
Display Colors	10 bit, 1.07B	Colors	
Number of Pixels	1920 x 1080	Pixel	
Pixel Pitch	0.744	mm	
Pixel Arrangement	RGB vertical stripe		
Display Operation Mode	Normally Black		
Surface Treatment	HC, 3H		

2. Absolute Maximum Ratings

The followings are maximum values which, if exceeded, may cause faulty operation or damage to the unit

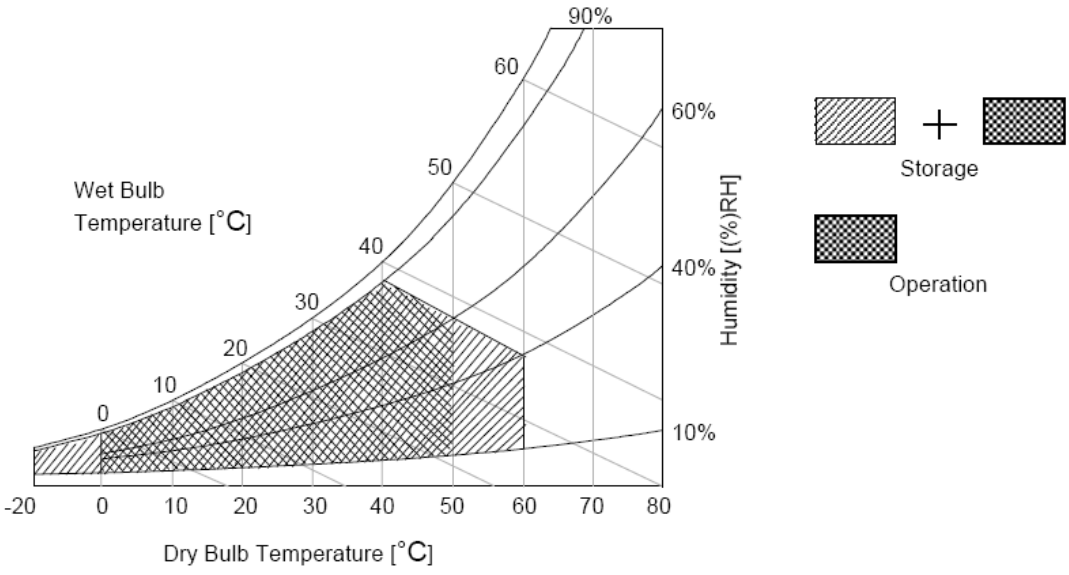
Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	V_{DD}	-0.3	14	[Volt]	Note 1
Input Voltage of Signal	Vin	-0.3	4	[Volt]	Note 1
Operating Temperature	TOP	0	+50	[°C]	Note 2
Operating Humidity	HOP	10	90	[%RH]	Note 2
Storage Temperature	TST	-20	+60	[°C]	Note 2
Storage Humidity	HST	10	90	[%RH]	Note 2
Panel Surface Temperature	PST	-	65	[°C]	Note 3

Note 1: Duration:50 msec.

Note 2 : Maximum Wet-Bulb should be 39℃ and No condensation.

The relative humidity must not exceed 90% non-condensing at temperatures of 40℃ or less. At temperatures greater than 40℃, the wet bulb temperature must not exceed 39℃.

Note 3: Surface temperature is measured at 50℃ Dry condition



3. Electrical Specification

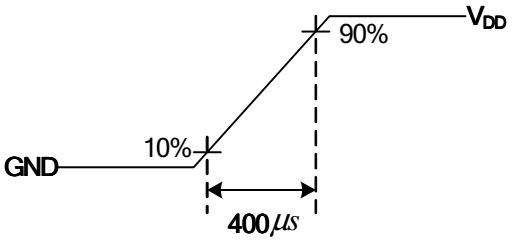
The T645HW03 V0 requires two power inputs. One is employed to power the LCD electronics and to drive the TFT array and liquid crystal. The second input for BLU is to power inverter.

3.1 Electrical Characteristics

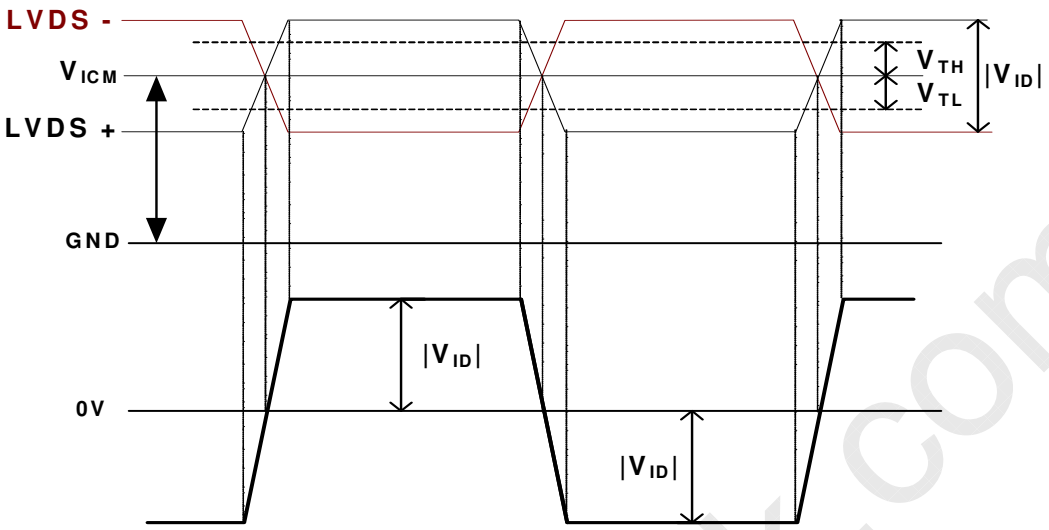
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max		
LCD							
Power Supply Input Voltage		V_{DD}	10.8	12.0	13.2	V_{DC}	1
Power Supply Input Current		I_{DD}	0.6	1.2	1.8	A	2
Power Consumption		P_C	7.92	14.4	19.44	Watt	2
Inrush Current		I_{RUSH}	--	--	16	A	3
LVDS Interface	Input Differential Voltage	$\|V_{ID}\|$	200	400	600	mV_{DC}	4
	Differential Input High Threshold Voltage	V_{TH}	+100	--	+300	4	4
	Differential Input Low Threshold Voltage	V_{TL}	-300	--	-100	4	4
	Input Common Mode Voltage	V_{ICM}	1.10	1.25	1.40	V_{DC}	4
CMOS Interface	Input High Threshold Voltage	V_{IH} (High)	2.7	--	3.3	V_{DC}	--
	Input Low Threshold Voltage	V_{IL} (Low)	0	--	0.6	V_{DC}	--
Backlight Power Consumption		P_{BL}		380		Watt	--
Life Time			50000		--	Hours	--

Note :

1. The ripple voltage should be controlled under 10% of V_{CC}
2. V_{DD} = 12.0V, Fv = 120Hz, F_{CLK} = 82MHz , 25 ℃, Test Pattern : White Pattern
   >> refer to “Section:3.3 Signal Timing Specification, Typical timing”
3. Measurement condition : Rising time = 400us



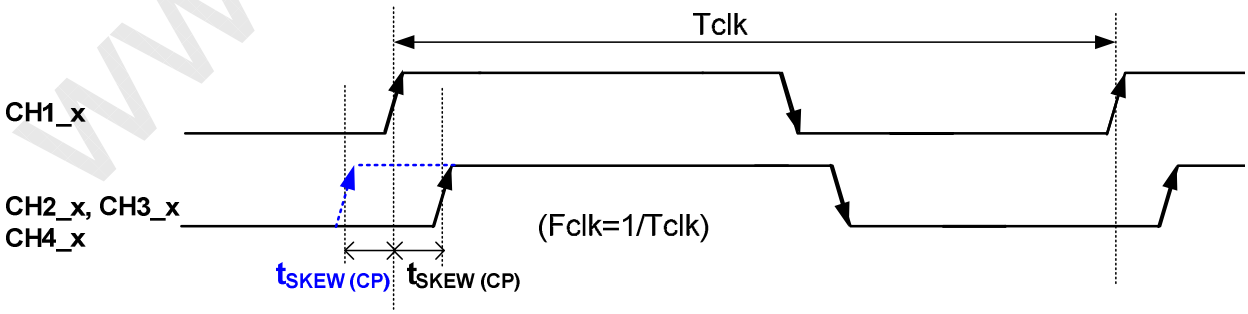
4. V_{ICM} = 1.25V



3.2 AC Electrical Characteristics

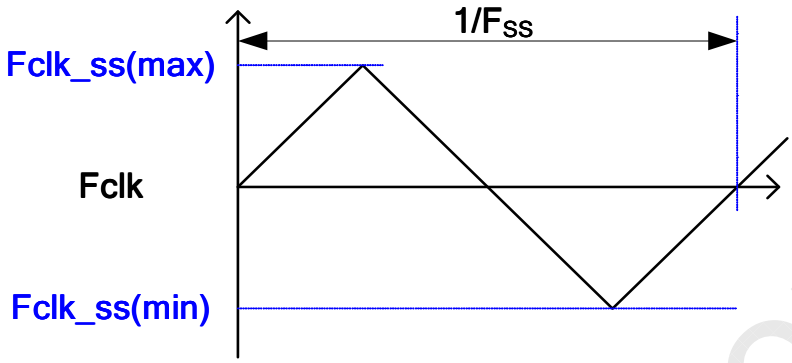
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max		
LVDS Interface	Input Channel Pair Skew Margin	$t_{SKEW\ (CP)}$	-500	--	+500	ps	1
	Receiver Clock : Spread Spectrum Modulation range	Fclk_ss	Fclk -3%	--	Fclk +3%	MHz	2
	Receiver Clock : Spread Spectrum Modulation frequency	Fss	30	--	200	KHz	2
	Receiver Data Input Margin Fclk = 85 MHz Fclk = 65 MHz	tRMG	 -0.4 -0.5	 -- --	 0.4 0.5	ns	3

1. Input Channel Pair Skew Margin



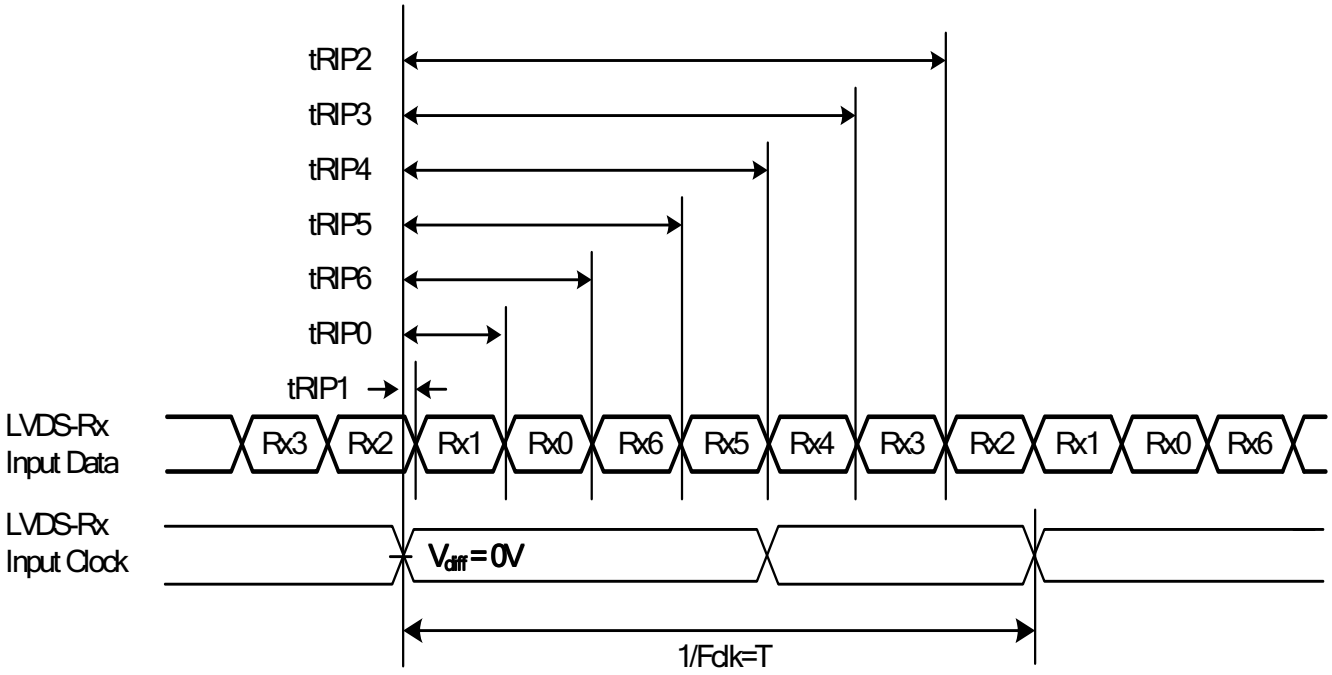
Note: x = 0, 1, 2, 3, 4

2. LVDS Receiver Clock SSCG (Spread spectrum clock generator) is defined as below figures



3. Receiver Data Input Margin

Parameter	Symbol	Rating			Unit	Note
		Min	Type	Max		
Input Clock Frequency	Fclk	Fclk (min)	--	Fclk (max)	MHz	**T=1/Fclk**
Input Data Position0	tRIP1	-|tRMG|	0	|tRMG|	ns	
Input Data Position1	tRIP0	T/7-|tRMG|	T/7	T/7+|tRMG|	ns	
Input Data Position2	tRIP6	2T/7-|tRMG|	2T/7	2T/7+|tRMG|	ns	
Input Data Position3	tRIP5	3T/7-|tRMG|	3T/7	3T/7+|tRMG|	ns	
Input Data Position4	tRIP4	4T/7-|tRMG|	4T/7	4T/7+|tRMG|	ns	
Input Data Position5	tRIP3	5T/7-|tRMG|	5T/7	5T/7+|tRMG|	ns	
Input Data Position6	tRIP2	6T/7-|tRMG|	6T/7	6T/7+|tRMG|	ns	



3.3 Interface Connections

LCD connector: FI-RE51S-HF (Manufactured by JAE)

Mating connector: FI-RE51S-HL (Manufactured by JAE)

PIN	Symbol	Description	PIN	Symbol	Description
1	V_{DD}	Power Supply, +12V DC Regulated	26	CH4_0+	LVDS Channel 4, Signal 0+
2	V_{DD}	Power Supply, +12V DC Regulated	27	CH4_1-	LVDS Channel 4, Signal 1-
3	V_{DD}	Power Supply, +12V DC Regulated	28	CH4_1+	LVDS Channel 4, Signal 1+
4	V_{DD}	Power Supply, +12V DC Regulated	29	CH4_2-	LVDS Channel 4, Signal 2-
5	V_{DD}	Power Supply, +12V DC Regulated	30	CH4_2+	LVDS Channel 4, Signal 2+
6	GND	Ground	31	GND	Ground
7	GND	Ground	32	CH4_CLK-	LVDS Channel 4, Clock -
8	GND	Ground	33	CH4_CLK+	LVDS Channel 4, Clock +
9	GND	Ground	34	GND	Ground
10	CH2_0-	LVDS Channel 2, Signal 0-	35	CH4_3-	LVDS Channel 4, Signal 3-
11	CH2_0+	LVDS Channel 2, Signal 0+	36	CH4_3+	LVDS Channel 4, Signal 3+
12	CH2_1-	LVDS Channel 2, Signal 1-	37	CH4_4-	LVDS Channel 4, Signal 4-
13	CH2_1+	LVDS Channel 2, Signal 1+	38	CH4_4+	LVDS Channel 4, Signal 4+
14	CH2_2-	LVDS Channel 2, Signal 2-	39	GND	Ground
15	CH2_2+	LVDS Channel 2, Signal 2+	40	Reserved	AUO Internal Use Only
16	GND	Ground	41	Reserved	AUO Internal Use Only
17	CH2_CLK-	LVDS Channel 2, Clock -	42	Reserved	AUO Internal Use Only
18	CH2_CLK+	LVDS Channel 2, Clock +	43	Reserved	AUO Internal Use Only
19	GND	Ground	44	Reserved	AUO Internal Use Only
20	CH2_3-	LVDS Channel 2, Signal 3-	45	LVDS_SEL	Open/High(3.3V) for NS, Low(GND) for JEIDA
21	CH2_3+	LVDS Channel 2, Signal 3+	46	Reserved	AUO Internal Use Only
22	CH2_4-	LVDS Channel 2, Signal 4-	47	3D_SEL	Open/High(3.3V) for 2D mode display, Low(GND) for 3D mode display
23	CH2_4+	LVDS Channel 2, Signal 4+	48	BIT_SEL	Open/High(3.3V) for 10 bits LVDS input, Low(GND) for 8 bits LVDS input
24	GND	Ground	49	Reserved	AUO Internal Use Only
25	CH4_0-	LVDS Channel 4, Signal 0-	50	Reserved	AUO Internal Use Only
			51	Reserved	AUO Internal Use Only

LCD connector: FI-RE41S-HF (Manufactured by JAE)

Mating connector: FI-RE41S-HL (Manufactured by JAE)

PIN	Symbol	Description	PIN	Symbol	Description
1	V_{DD}	Power Supply, +12V DC Regulated	21	CH1_3+	LVDS Channel 1, Signal 3+
2	V_{DD}	Power Supply, +12V DC Regulated	22	CH1_4-	LVDS Channel 1, Signal 4-
3	V_{DD}	Power Supply, +12V DC Regulated	23	CH1_4+	LVDS Channel 1, Signal 4+
4	V_{DD}	Power Supply, +12V DC Regulated	24	GND	Ground
5	V_{DD}	Power Supply, +12V DC Regulated	25	CH3_0-	LVDS Channel 3, Signal 0-
6	GND	Ground	26	CH3_0+	LVDS Channel 3, Signal 0+
7	GND	Ground	27	CH3_1-	LVDS Channel 3, Signal 1-
8	GND	Ground	28	CH3_1+	LVDS Channel 3, Signal 1+
9	GND	Ground	29	CH3_2-	LVDS Channel 3, Signal 2-
10	CH1_0-	LVDS Channel 1, Signal 0-	30	CH3_2+	LVDS Channel 3, Signal 2+
11	CH1_0+	LVDS Channel 1, Signal 0+	31	GND	Ground
12	CH1_1-	LVDS Channel 1, Signal 1-	32	CH3_CLK-	LVDS Channel 3, Clock -
13	CH1_1+	LVDS Channel 1, Signal 1+	33	CH3_CLK+	LVDS Channel 3, Clock +
14	CH1_2-	LVDS Channel 1, Signal 2-	34	GND	Ground
15	CH1_2+	LVDS Channel 1, Signal 2+	35	CH3_3-	LVDS Channel 3, Signal 3-
16	GND	Ground	36	CH3_3+	LVDS Channel 3, Signal 3+
17	CH1_CLK-	LVDS Channel 1, Clock -	37	CH3_4-	LVDS Channel 3, Signal 4-
18	CH1_CLK+	LVDS Channel 1, Clock +	38	CH3_4+	LVDS Channel 3, Signal 4+
19	GND	Ground	39	GND	Ground
20	CH1_3-	LVDS Channel 1, Signal 3-	40	NC	No Connect
			41	NC	No Connect

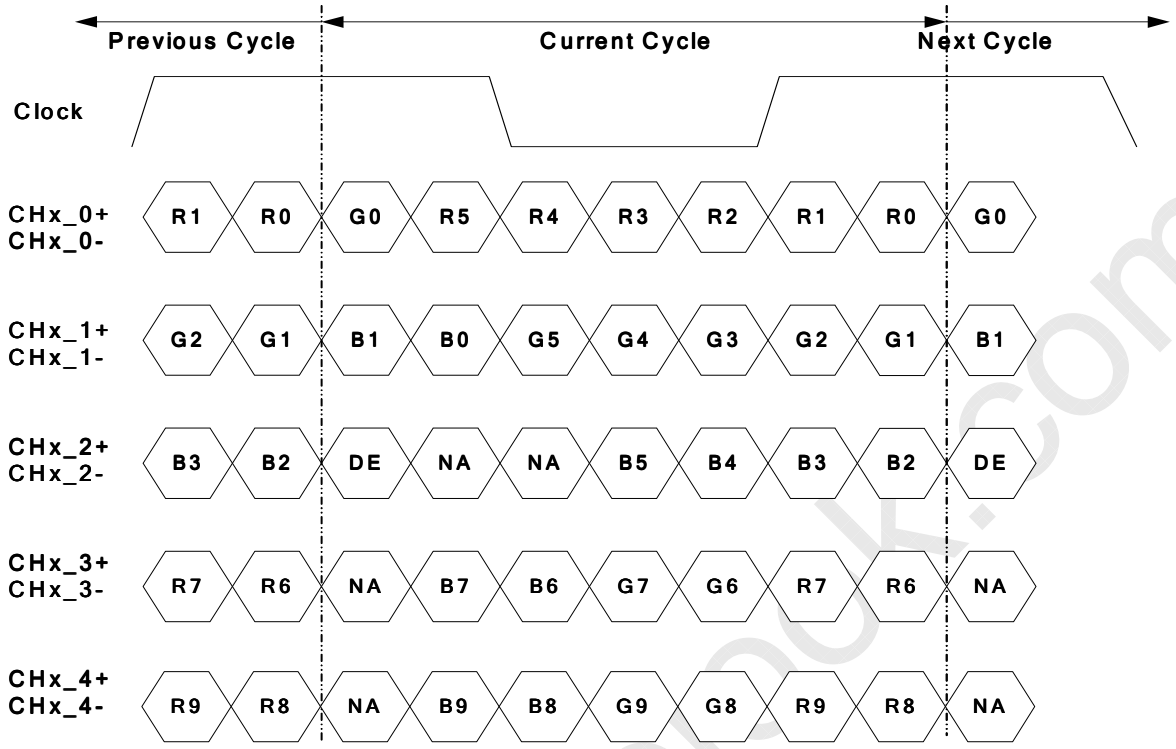
Note 1: All GND (ground) pins should be connected together and should also be connected to the LCD's metal frame.

Note 2: All V_{DD} (power input) pins should be connected together.

Note 3: All Reserved pins should be open without voltage input.

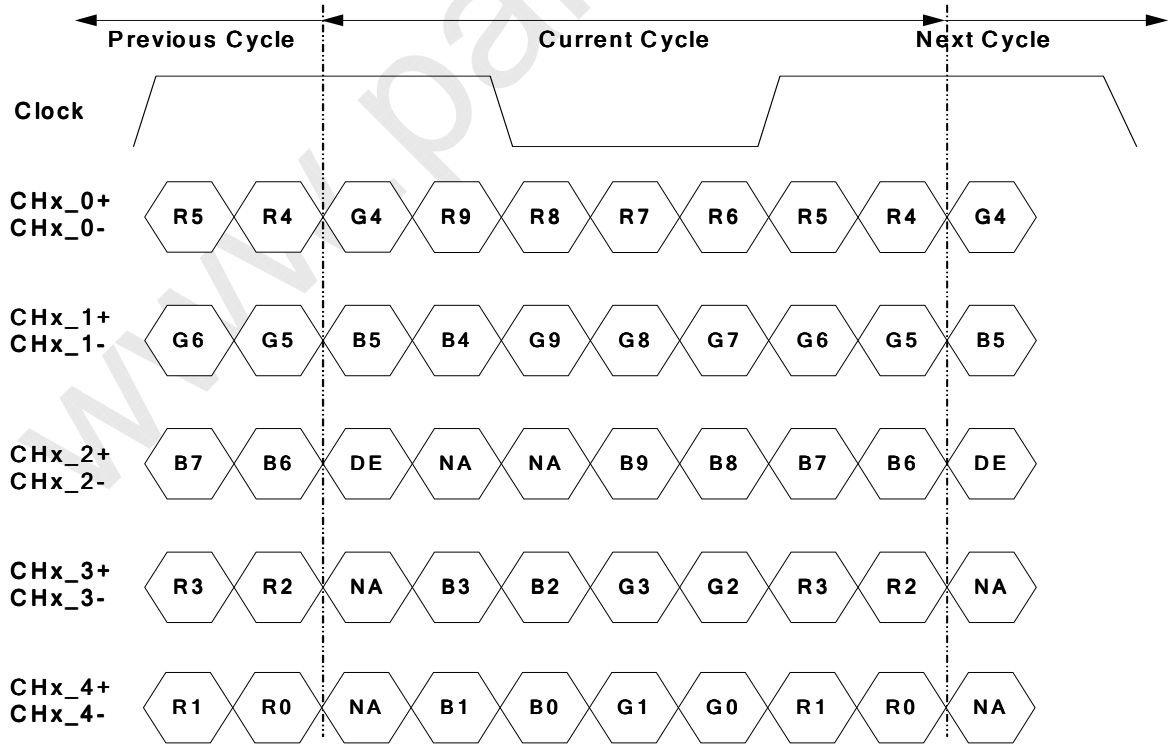
Note 4: All NC pins should be open without voltage input

LVDS Option = High/Open➔NS



Note: x = 1, 2, 3, 4…

LVDS Option = Low➔JEIDA



Note: x = 1, 2, 3, 4…

3.4 Signal Timing Specification

This is the signal timing required at the input of the user connector. All of the interface signal timing should be satisfied with the following specifications for its proper operation.

Signal	Item	Symbol	Min.	Typ.	Max	Unit
Vertical Section	Period	Tv	1090	1130	1160	Th
	Active	Tdisp (v)		1080		Th
	Blanking	Tblk (v)	10	50	80	Th
Horizontal Section	Period	Th	550	570	580	Tclk
	Active	Tdisp (h)		480		Tclk
	Blanking	Tblk (h)	70	90	100	Tclk
Clock	Frequency	Fclk=1/Tclk	71.94	77.29	80.74	MHz
Vertical Frequency	Frequency	Fv	118	120	122	Hz
Horizontal Frequency	Frequency	Fh	130.8	135.6	139.2	KHz

Notes:

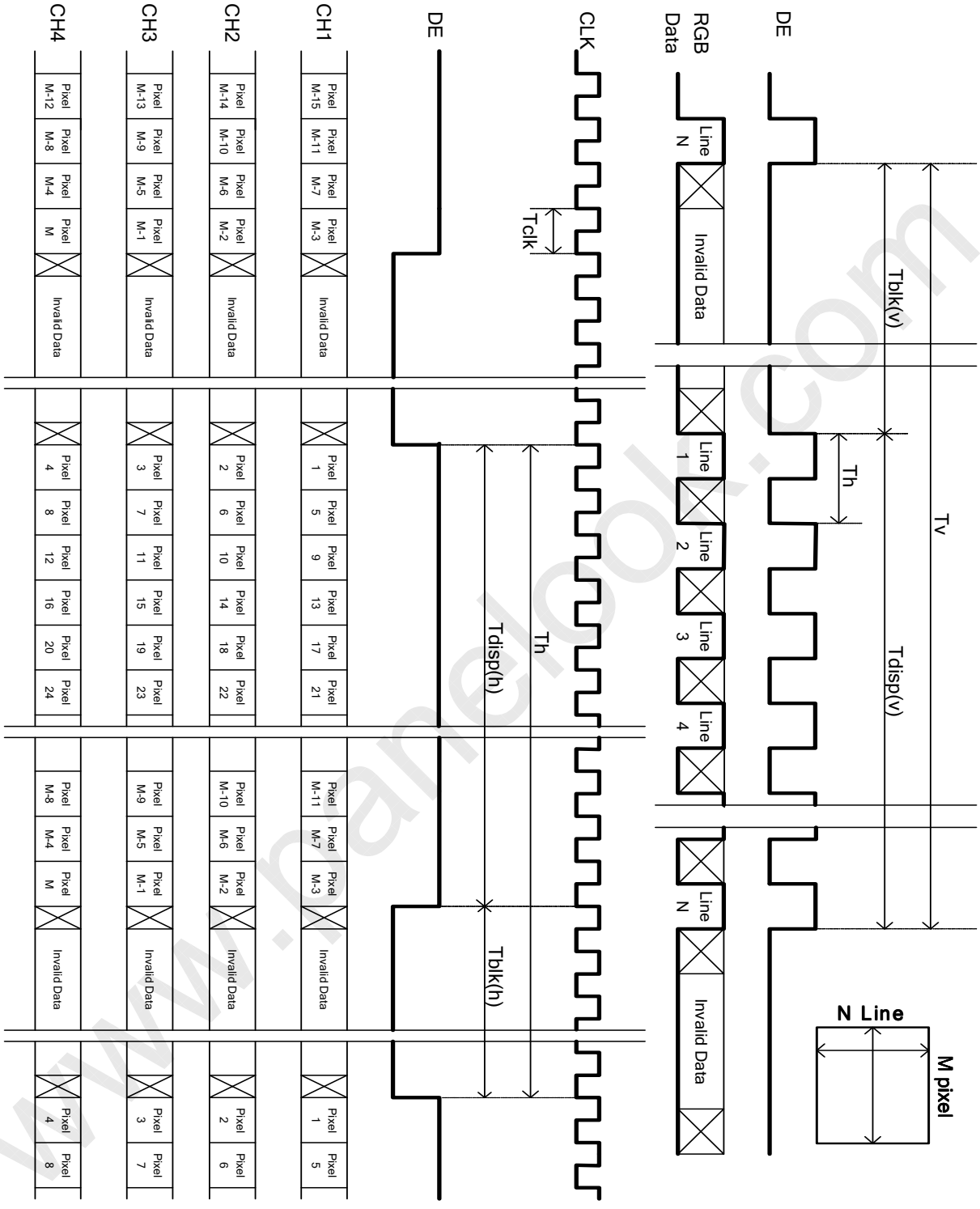
(1) Display position is specific by the rise of DE signal only.
Horizontal display position is specified by the rising edge of 1st DCLK after the rise of 1st DE, is displayed on the left edge of the screen.

(2) Vertical display position is specified by the rise of DE after a “Low” level period equivalent to eight times of horizontal period. The 1st data corresponding to one horizontal line after the rise of 1st DE is displayed at the top line of screen.

(3) If a period of DE “High” is less than 1920 DCLK or less than 1080 lines, the rest of the screen displays black.

(4) The display position does not fit to the screen if a period of DE “High” and the effective data period do not synchronize with each other.

3.5 Signal Timing Waveforms



3.6 Color Input Data Reference

The brightness of each primary color (red, green and blue) is based on the 10 bit gray scale data input for the color; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

Color Data Reference

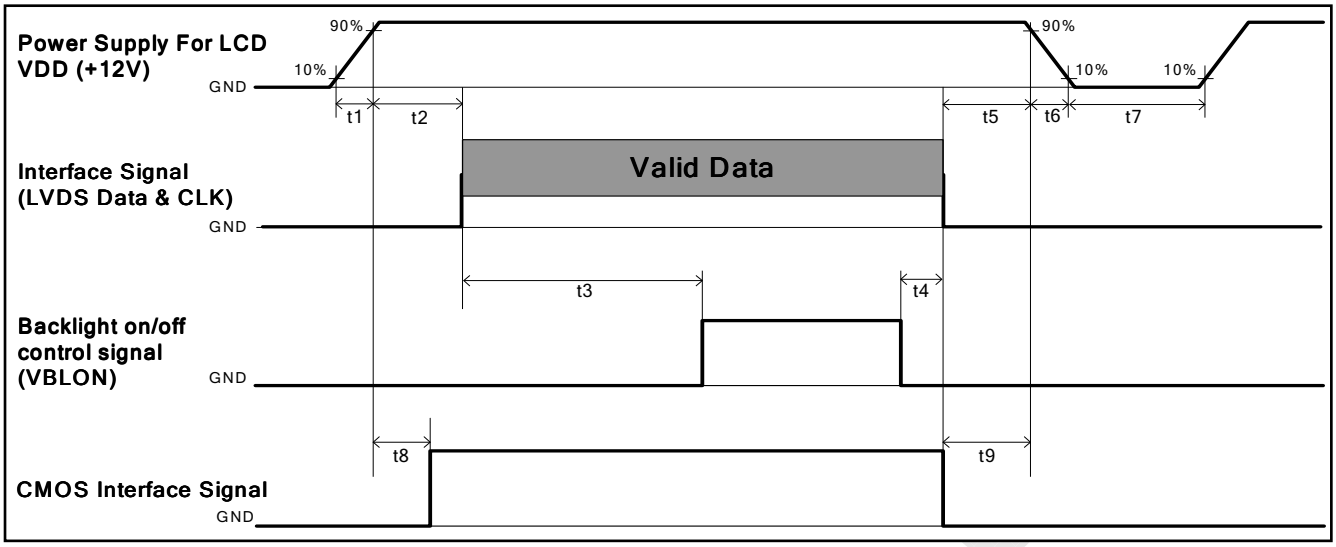
Color		Input Color Data																													
		RED										GREEN										BLUE									
		MSB									LSB	MSB									LSB	MSB									LSB
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue(1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R	RED(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(001)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	RED(1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
G	GREEN(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

	GREEN(1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	GREEN(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
B	BLUE(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

	BLUE(1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	BLUE(1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

3.7 Power Sequence for LCD

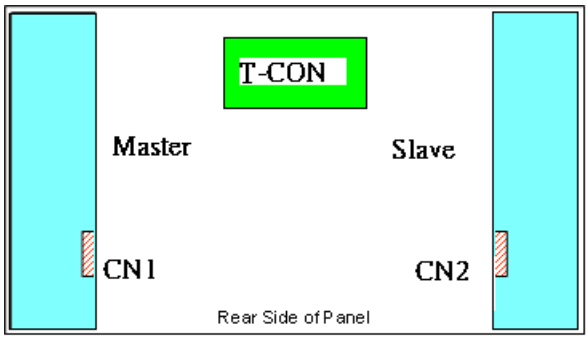


Parameter	Values			Unit
	Min.	Type.	Max.	
t1	0.4	---	30	ms
t2	0.1	---	50	ms
t3	450	---	---	ms
t4	0 *1	---	---	ms
t5	0	---	---	ms
t6	---	---	--- *2	ms
t7	500	---	---	ms
t8	10	---	50	ms
t9	0	---	---	ms

Note:
(1) T4=0 : concern for residual pattern before BLU turn off.
(2) T6 : voltage of VDD must decay smoothly after power-off. (customer system decide this value)

3.8 Backlight Specification

The backlight unit use Inverter type to control CCFL lamp.



3.8.1 Electrical specification

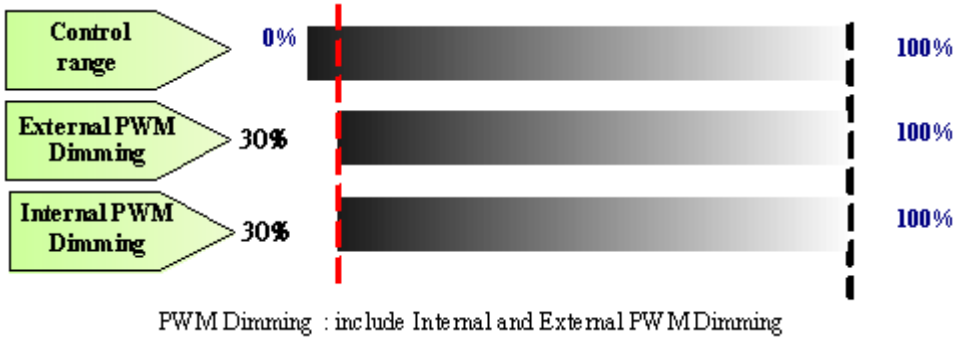
Item	Symbol		Condition	Spec			Unit	Note
				Min	Typ	Max		
Input Voltage	V_{DDB}		-	21.6	24	26.4	VDC	-
Input Current	I_{DDB}		VDDB=24V	13.64	15.84	18.51	ADC	1
Input Power	P_{DDB}		VDDB=24V	360	380	400	W	1
Inrush Current	I_{RUSH}		VDDB=24V	-	-	22.88	ADC	2
Operating Frequency	FBL		VDDB=24V	43	45	47	KHz	
On/Off control voltage	V_{BLON}	ON	VDDB=24V	2	3.3	5.0	VDC	-
		OFF		0	-	0.8		-
On/Off control current	I_{BLON}		VDDB=24V	-	-	1.5	mA	-
Internal PWM Dimming Control Voltage	V_IPWM	MAX	VDDB=24V	3.0	-	3.3	VDC	-
		MIN		-	0	-	VDC	-
Internal PWM Dimming Control Current	I_IPWM		VDDB=24V	-	-	2	mADC	-
Internal PWM Dimming Ratio	R_IPWM		VDDB=24V	30	-	100	%	
External PWM Control Voltage	V_EPWM	MAX	VDDB=24V	2	-	3.3	VDC	-
		MIN	VDDB=24V	0	-	0.8		-
External PWM Control Current	I_EPWM		VDDB=24V	-	-	2	mADC	-
External PWM Duty ratio	D_EPWM		VDDB=24V	30	-	100	%	3
External PWM Frequency	F_EPWM		VDDB=24V	140	180	240	Hz	-

Note 1 : Dimming ratio= 100% (MAX)（Ta=25±5℃, Turn on for 45minutes）
Note 2 : Measurement condition Rising time = 20ms (VDDB : 10%~90%);
Note 3: Less than 30% dimming control is functional well and no backlight shutdown happened

3.8.2 Input Pin Assignment

Inverter board CN1 connector : CI0114M1HRL-NH (Cvilux)

Pin	Symbol	Description
1	VDDB	Operating Voltage Supply, +24V DC regulated
2	VDDB	Operating Voltage Supply, +24V DC regulated
3	VDDB	Operating Voltage Supply, +24V DC regulated
4	VDDB	Operating Voltage Supply, +24V DC regulated
5	VDDB	Operating Voltage Supply, +24V DC regulated
6	BLGND	Ground and Current Return
7	BLGND	Ground and Current Return
8	BLGND	Ground and Current Return
9	BLGND	Ground and Current Return
10	BLGND	Ground and Current Return
11	DET (note 1)	BLU status detection: Normal : 0~0.8V ; Abnormal : Open collector
12	VBLON	BLU On-Off control: High (3.3V) : BL On ; Low /Open (0~0.8V/GND) : BL Off
13	VDIM (note 2)	Internal PWM (0~3.3V for 30~100% Duty, open for 100%) < NC ; at External PWM mode>
14	PDIM (note 2)	External PWM (30%~100% Duty, open for 100%) < NC ; at Internal PWM mode>



PWM Dimming : include Internal and External PWM Dimming

Note (1) Det is Output pin for detect power error. When backlight is normal operation, DET is GND(0V). When backlight is abnormal, DET is high(5V).

Note (2) PWM dimming function is included internal PWM and external PWM.

Internal PWM: input voltage 0 (GND) ~3.3V to pin 13th, and duty ratio of output voltage/current of inverter is from 30% to 100%. When use pin 13th to control backlight luminance, the pin 14th will be NC and can not be affect by noise!

External PWM: input duty ratio 30% ~100% to pin 14th, and duty ratio of output voltage/current of inverter is from 30% to 100%. When use pin 14th to control backlight luminance, the pin 13th will be NC and can not be affect by noise!

Pin 13th and pin 14th can not be used at the same time!

Inverter board CN2 connector : CI0114M1HRL-NH (Cvilux)

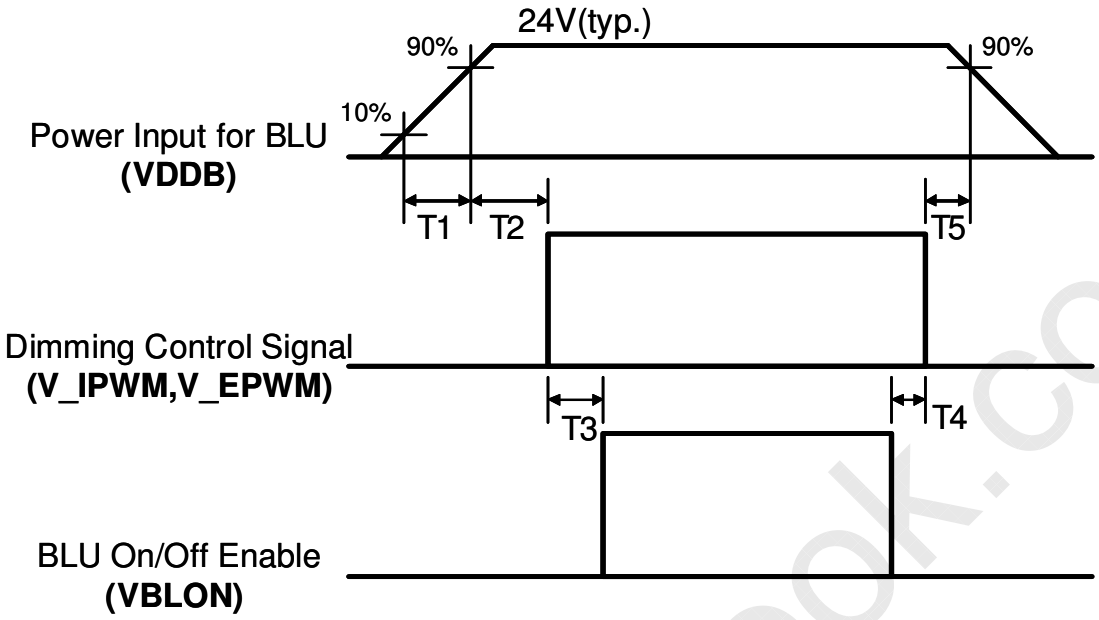
Pin	Symbol	Description
1	VDDB	Operating Voltage Supply, +24V DC regulated
2	VDDB	Operating Voltage Supply, +24V DC regulated
3	VDDB	Operating Voltage Supply, +24V DC regulated
4	VDDB	Operating Voltage Supply, +24V DC regulated
5	VDDB	Operating Voltage Supply, +24V DC regulated
6	BLGND	Ground and Current Return
7	BLGND	Ground and Current Return
8	BLGND	Ground and Current Return
9	BLGND	Ground and Current Return
10	BLGND	Ground and Current Return
11	NC (note 5)	No connect
12	NC (note 5)	No connect
13	NC (note 5)	No connect
14	NC (note 5)	No connect

Note [3]: All GND (ground) pins connectors should be connected together and should also be connected to the LCD's metal frame.

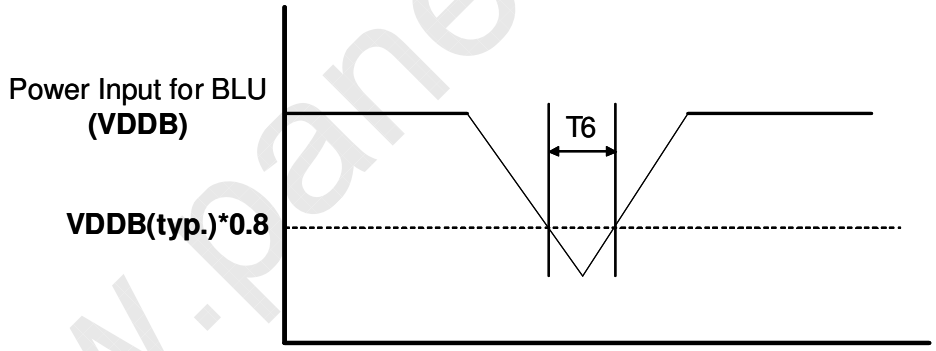
Note [4]: All V_{DDB} (power input) pins connectors should be connected together.

Note [5]: All NC (no connection) pins should be open without voltage input.

3.8.3 Power Sequence for Inverter



Dip condition for Inverter

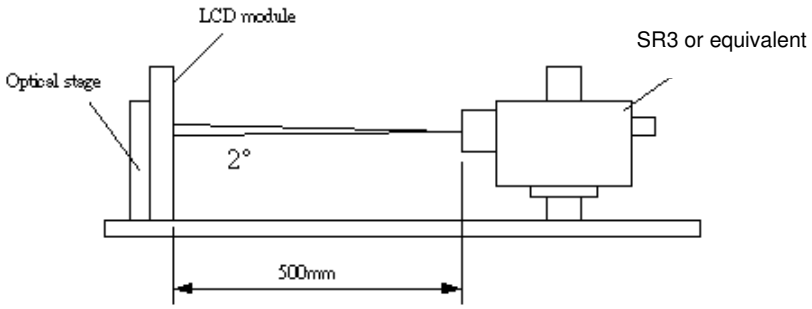


Parameter	Value			Units
	Min	Typ	Max	
T1	20	-	-	ms
T2	500	-	-	ms
T3	250	-	-	ms
T4	0	-	-	ms
T5	1	-	-	ms
T6	-	-	10	ms

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 45 minutes in a dark environment at 25℃. The values specified are at an approximate distance 50cm from the LCD surface at a viewing angle of φ and θ equal to 0°.

Fig.1 presents additional information concerning the measurement equipment and method.



Parameter		Symbol	Values			Unit	Notes
			Min.	Typ.	Max		
Contrast Ratio (2D)		CR	4,000	5,000	--		1
Contrast Ratio (3D)		CR	800	1,000	--		1
Surface Luminance (2D)		L_{WH}	360	450	--	cd/m^2	2
Surface Luminance (3D)/per eye		L_{WH}	100	125	--	cd/m^2	2
Luminance Variation		$\delta_{WHITE(9P)}$	--	--	1.3		3
Response Time (G to G)		Tγ	--	5.5	--	Ms	4
Color Gamut		NTSC		72		%	
3D cross talk (middle)			--	< 3%	--		mid axis
3D cross talk (+/- 15 degrees vert)				< 10%			6
Color Coordinates							
	Red	R_X	Typ.-0.03	0.645	Typ.+0.03		
		R_Y		0.330			
	Green	G_X		0.290			
		G_Y		0.615			
	Blue	B_X		0.145			
		B_Y		0.055			
	White (2D)	W_X		0.280			
		W_Y		0.290			
	White (3D)	W_X		0.290			
		W_Y		0.300			

Viewing Angle							5
	x axis, right(φ=0°)	θ_r	--	89	--	degree	
	x axis, left(φ=180°)	θ_l	--	89	--	degree	
	y axis, up(φ=90°)	θ_u	--	89	--	degree	
	y axis, down (φ=270°)	θ_d	--	89	--	degree	

Note:

1. Contrast Ratio (CR) is defined mathematically as:

$$\textbf{Contrast Ratio} = \frac{\textbf{Surface Luminance of } L_{on5}}{\textbf{Surface Luminance of } L_{off5}}$$

2. Surface luminance is luminance value at point 5 across the LCD surface 50cm from the surface with all pixels displaying white. From more information see FIG 2. When lamp current I_H = 13.5smA. L_{WH}=Lon5 where Lon5 is the luminance with all pixels displaying white at center 5 location.
3. The variation in surface luminance, δWHITE is defined (center of Screen) as:

   $\delta_{WHITE(9P)}$= Maximum(L_{on1}, L_{on2},…,L_{on9})/ Minimum(L_{on1}, L_{on2},…L_{on9})
4. Response time T_γ is the average time required for display transition by switching the input signal for five luminance ratio (0%,25%,50%,75%,100% brightness matrix) and is based on F_v=60Hz to optimize.

Measured Response Time		Target				
		0%	25%	50%	75%	100%
Start	0%		0% to 25%	0% to 50%	0% to 75%	0% to 100%
	25%	25% to 0%		25% to 50%	25% to 75%	25% to 100%
	50%	50% to 0%	50% to 25%		50% to 75%	50% to 100%
	75%	75% to 0%	75% to 25%	75% to 50%		75% to 100%
	100%	100% to 0%	100% to 25%	100% to 50%	100% to 75%	

5. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG4.
6. head in 0 degrees vertical angle from mid axis

FIG. 2 Luminance

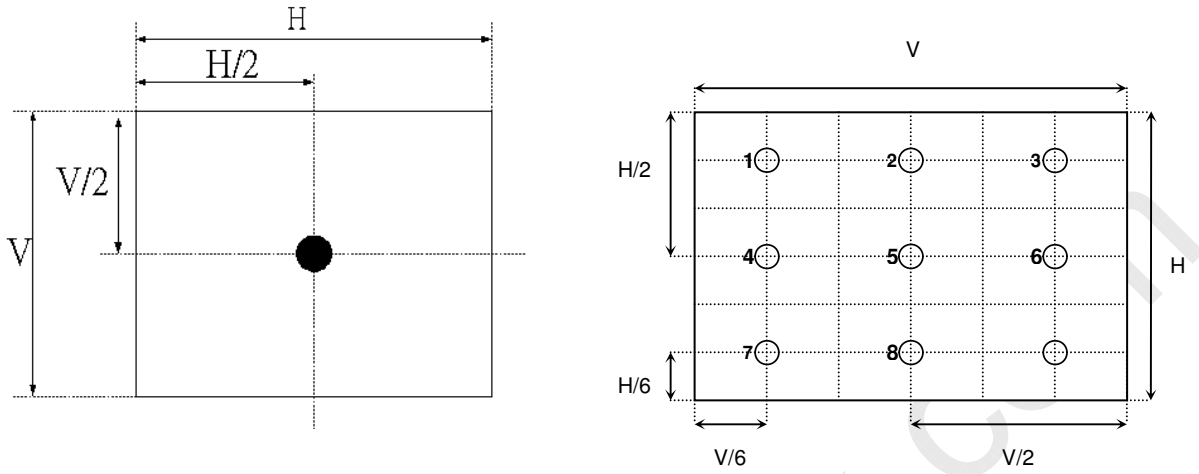


FIG.3 Response Time

The response time is defined as the following figure and shall be measured by switching the input signal for “any level of grey(bright) “ and “any level of gray(dark)”.

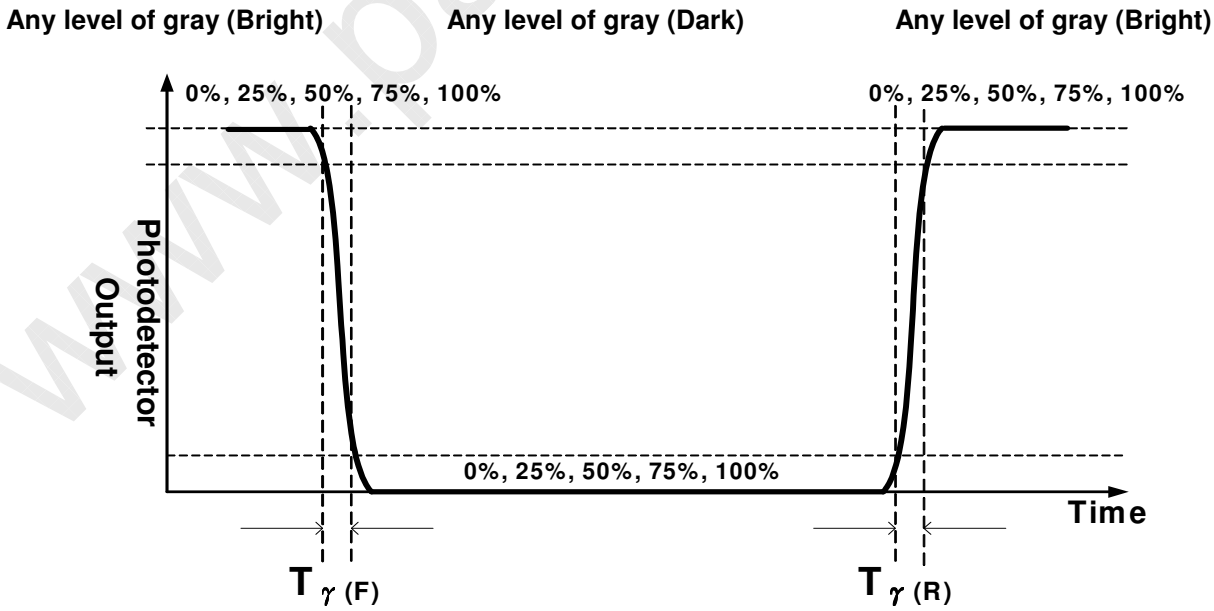
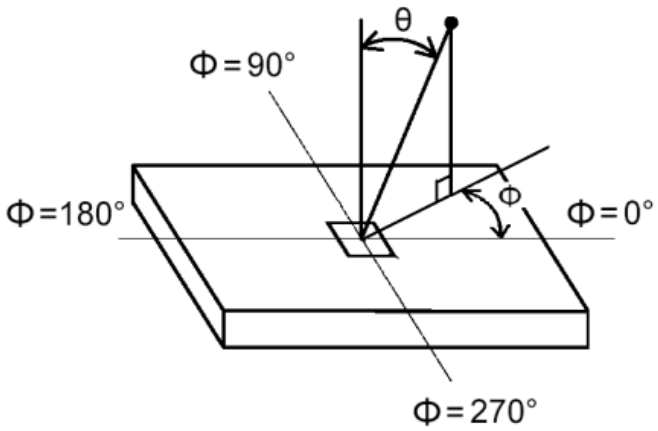


FIG.4 Viewing Angle

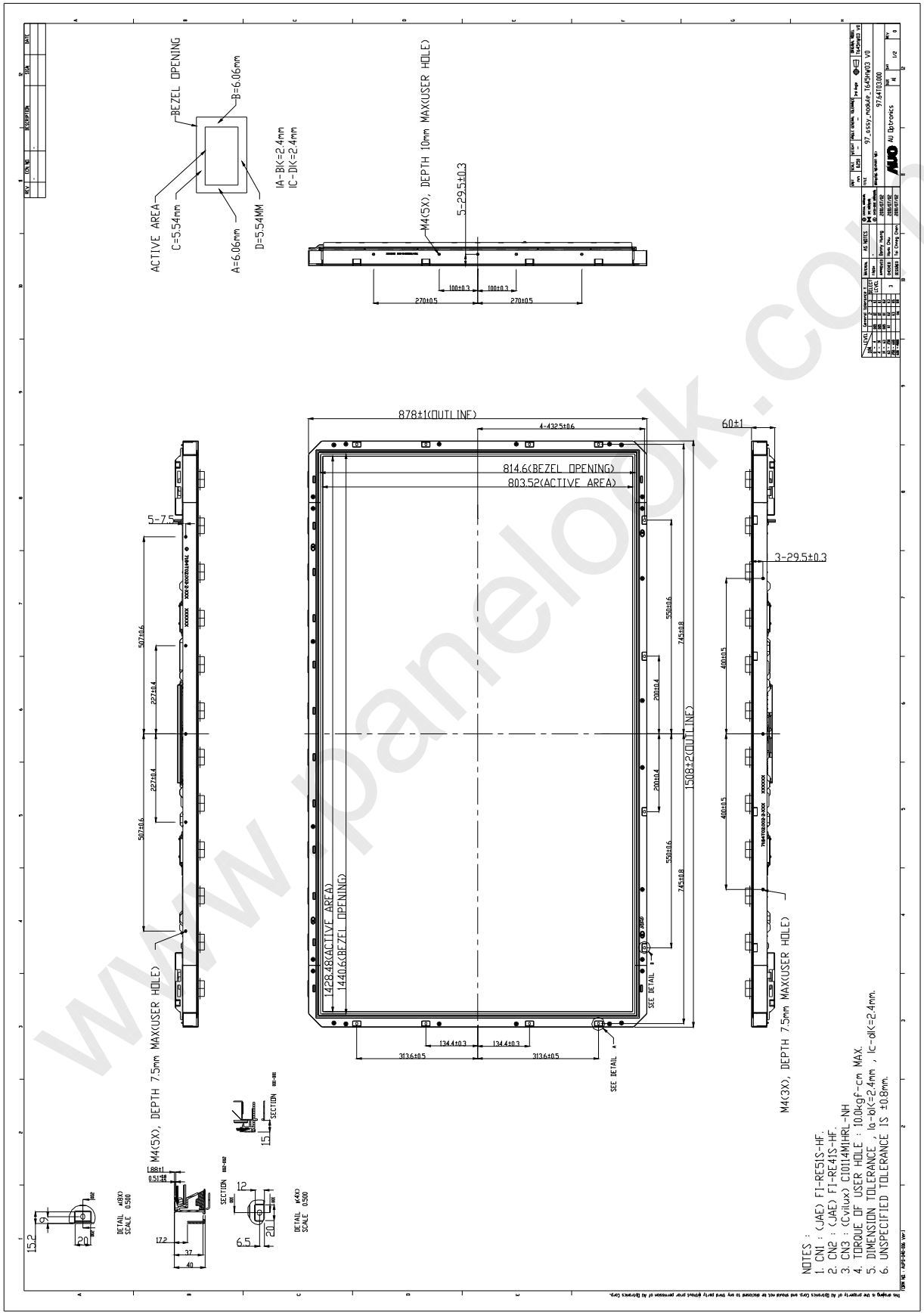


5. Mechanical Characteristics

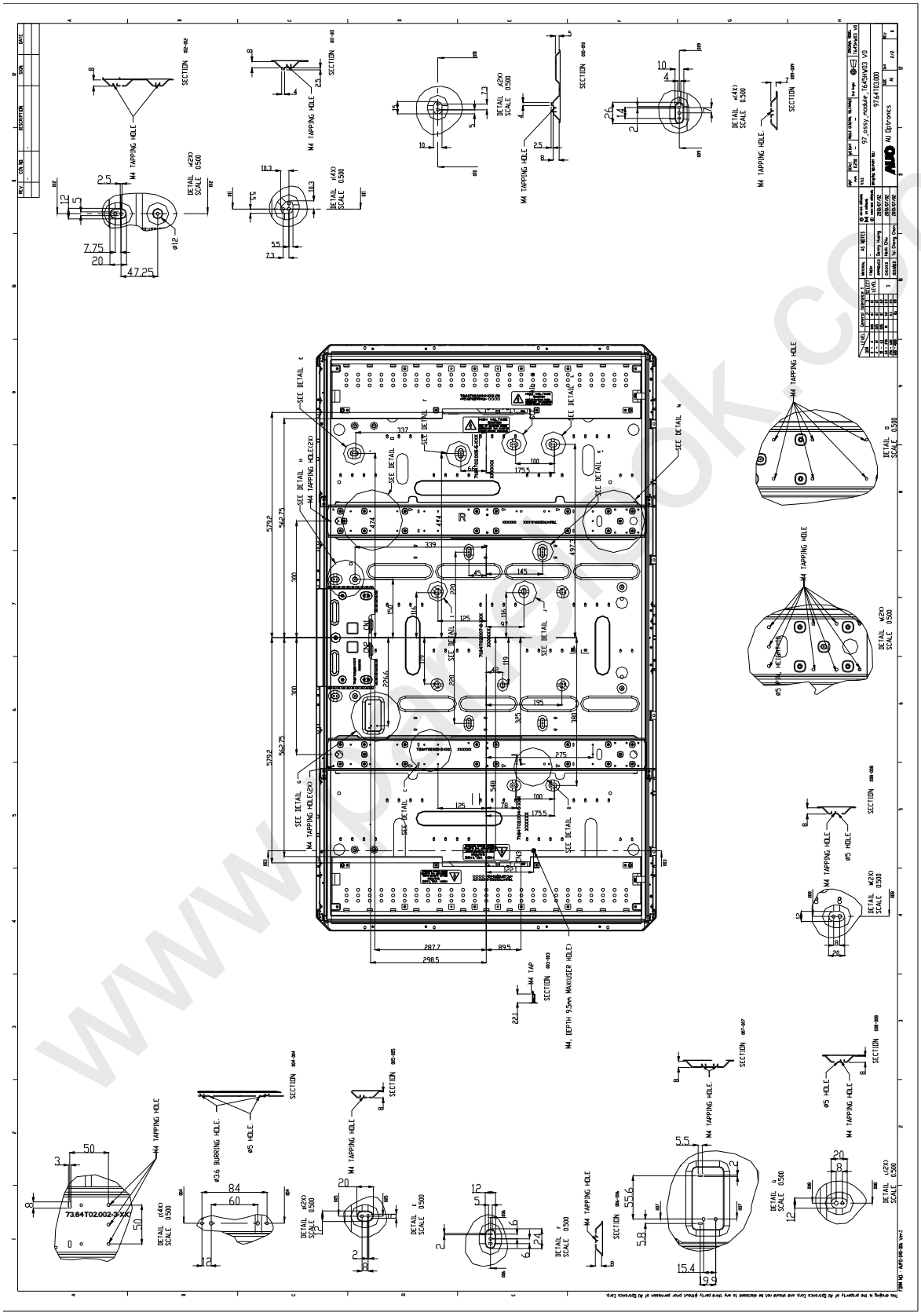
The contents provide general mechanical characteristics for the model T645HW03 V0. In addition the figures in the next page are detailed mechanical drawing of the LCD.

Outline Dimension	Horizontal	1508.0mm
	Vertical	878.0mm
	Depth	12.8mm (thinnest)
Bezel Opening	Horizontal	1440.6 mm
	Vertical	814.6 mm
Active Display Area	Horizontal	1428.48 mm
	Vertical	803.52 mm
Weight	36,000 g (Typ.)	
Surface Treatment	HC, 3H	

Front View



Back View



6. Reliability Test Items

	Test Item	Q'ty	Condition
1	High temperature storage test	3	60℃, 300hrs
2	Low temperature storage test	3	-20℃, 300hrs
3	High temperature operation test	3	50℃, 300hrs
4	Low temperature operation test	3	-5℃, 300hrs
5	Vibration test (non-operation)	3	Wave form : random Vibration level : 1.5G RMS Bandwidth: 10-300Hz Duration: X, Y, Z 30min One time for each direction
6	Shock test (non-operation)	3	Shock level: 50G Waveform: half since wave, 11ms Direction: ±X, ±Y, ±Z, One time each direction
7	Vibration test (With carton)	3	Random wave (1.5G RMS, 10-200Hz) 30mins/ Per each X,Y,Z axes
8	Drop test (With carton)	3	Height: 25.4 cm 6 surfaces (ASTMD4169-I)

7. International Standard

7.1 Safety

(1) UL 60950-1, UL 60065; Standard for Safety of Information Technology Equipment Including electrical Business Equipment.

(2) IEC 60950-1 : 2001, IEC 60065:2001 ; Standard for Safety of International Electrotechnical Commission

(3) EN 60950 : 2001+A11, EN 60065:2002+A1:2006; European Committee for Electrotechnical Standardization (CENELEC), EUROPEAN STANDARD for Safety of Information Technology Equipment Including Electrical Business Equipment.

7.2 EMC

(1) ANSI C63.4 “Methods of Measurement of Radio-Noise Emissions from Low-Voltage Electrical and Electrical Equipment in the Range of 9kHz to 40GHz. “American National standards Institute(ANSI), 1992

(2) C.I.S.P.R “Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment.” International Special committee on Radio Interference.

(3) EN 55022 “Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment.” European Committee for Electrotechnical Standardization. (CENELEC), 1998

8. Packing

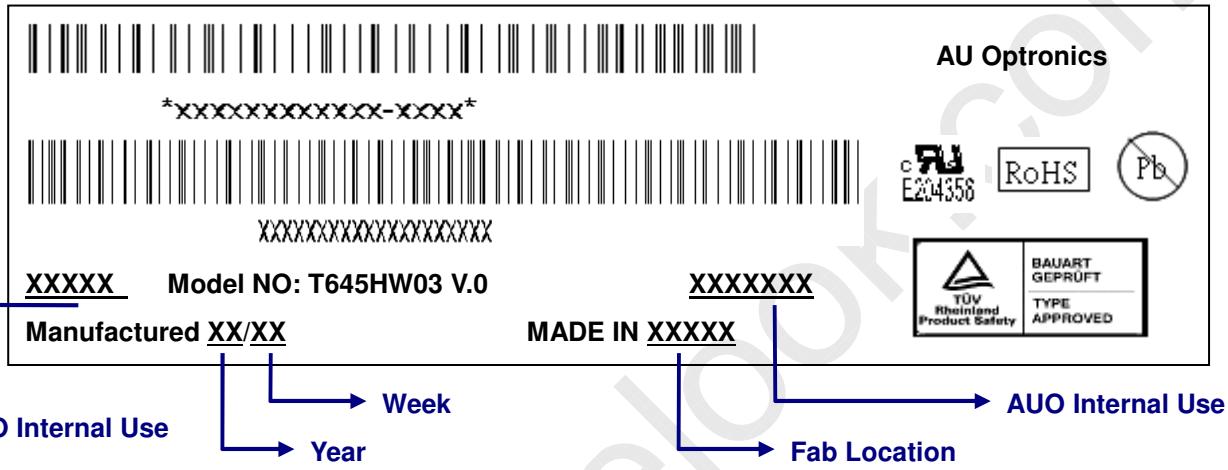
8-1 Definition of Label:

A. Panel Label:

xxxxxxxxxxxx-xxxx

Panel Unique ID

AUO Internal Use



AUO Internal Use

Week

Year

Fab Location

AUO Internal Use

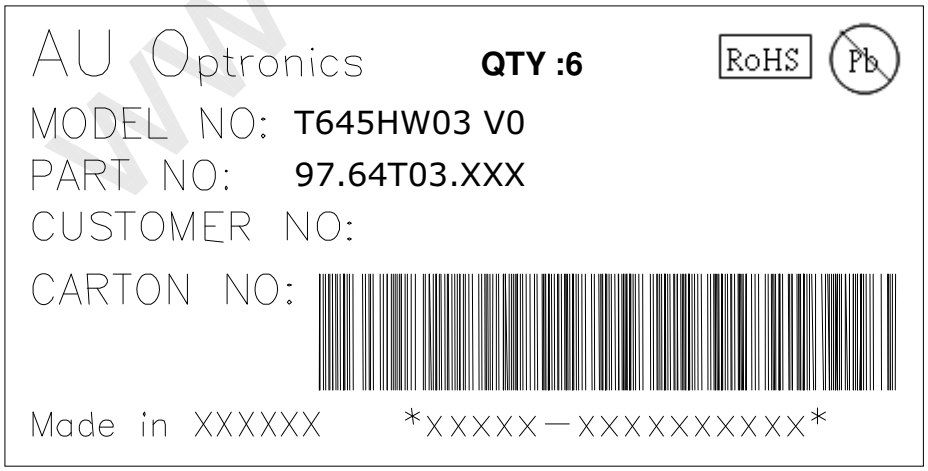
Green mark description

(1) For Pb Free Product, AUO will add Pb for identification.

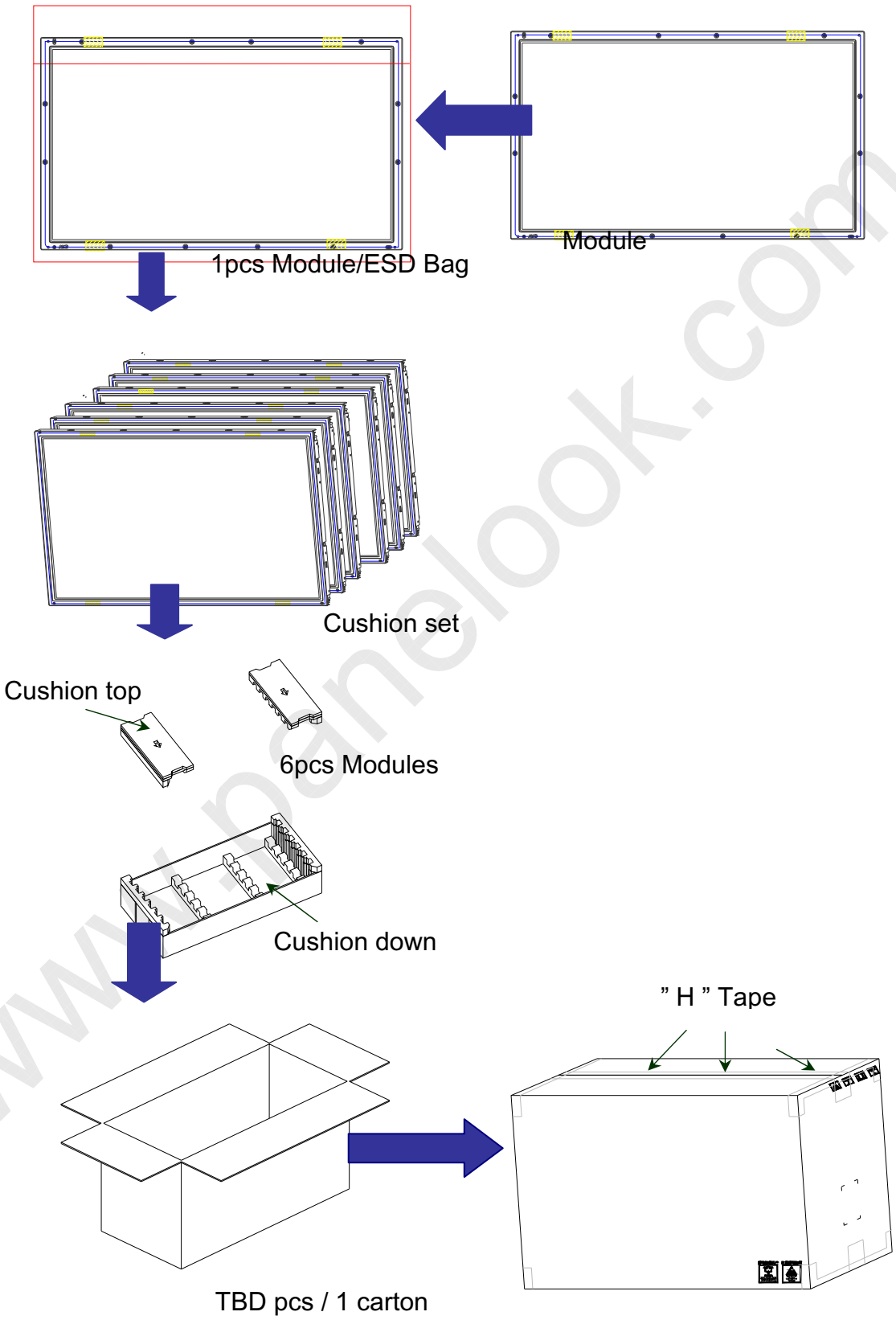
(2) For RoHs compatible products, AUO will add RoHS for identification.

Note: The green Mark will be present only when the green documents have been ready by AUO internal green team. (definition of green design follows the AUO green design checklist.)

B. Carton Label:

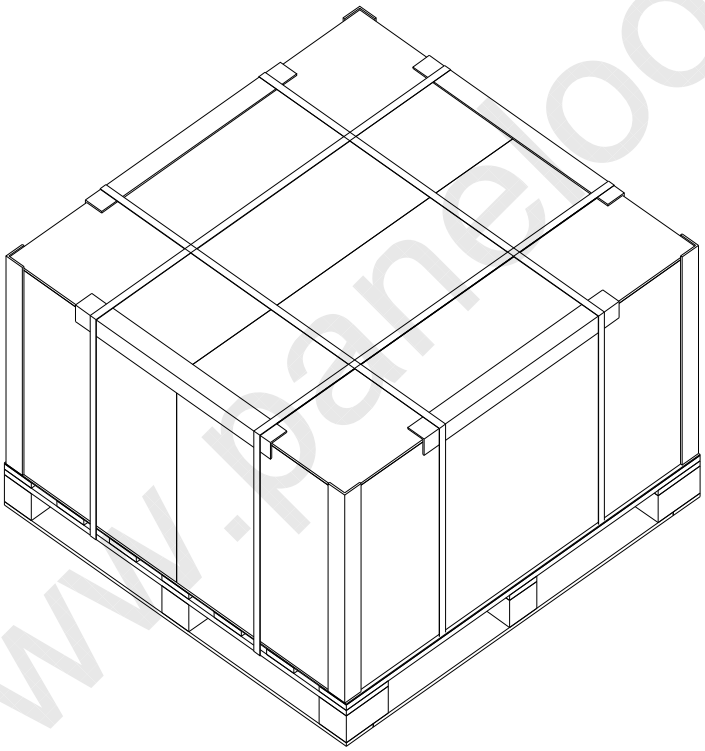


8-2 Packing Methods:



8-3 Pallet and Shipment Information

	Item	Specification			Packing Remark
		Qty.	Dimension	Weight (kg)	
1	Packing Box	6 pcs/box	1634(L)mm*555(W)mm*1035(H)mm	210	
2	Pallet	1	1660(L)mm*1150(W)mm*132(H)mm	20	
3	Boxes per Pallet	2 boxes/Pallet (By Air) ; 2 Boxes/Pallet (By Sea)			
4	Panels per Pallet	12 pcs/pallet(By Air) ; 12 pcs/Pallet (By Sea)			
5	Pallet after packing	12(by Air)	1660(L)mm*1150(W)mm*1167(H)mm	440(by Air)	
		24(by Sea)	1660(L)mm*1150(W)mm*2334(H)mm	880(by Sea)	40ft HQ



9. PRECAUTIONS

Please pay attention to the followings when you use this TFT LCD module.

9-1 MOUNTING PRECAUTIONS

(1) You must mount a module using holes arranged in four corners or four sides.

(2) You should consider the mounting structure so that uneven force (ex. twisted stress) is not applied to module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.

(3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.

(4) You should adopt radiation structure to satisfy the temperature specification.

(5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter cause circuit broken by electro-chemical reaction.

(6) Do not touch, push or rub the exposed polarizer with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of polarizer for bare hand or greasy cloth. (Some cosmetics are detrimental to the polarizer.)

(7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front/ rear polarizer. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.

(8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.

(9) Do not open the case because inside circuits do not have sufficient strength.

9-2 OPERATING PRECAUTIONS

(1) The device listed in the product specification sheets was designed and manufactured for TV application

(2) The spike noise causes the mis-operation of circuits. It should be lower than following voltage: V=±200mV(Over and under shoot voltage)

(3) Response time depends on the temperature. (In lower temperature, it becomes longer..)

(4) Brightness of CCFL depends on the temperature. (In lower temperature, it becomes lower.) And in lower temperature, response time (required time that brightness is stable after turned on) becomes longer.

(5) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.

(6) When fixed patterns are displayed for a long time, remnant image is likely to occur.

(7) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall

be done by system manufacturers. Grounding and shielding methods may be important to minimize the interface.

9-3 ELECTROSTATIC DISCHARGE CONTROL

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wristband etc. And don't touch interface pin directly.

9-4 PRECAUTIONS FOR STRONG LIGHT EXPOSURE

Strong light exposure causes degradation of polarizer and color filter.

9-5 STORAGE

When storing modules as spares for a long time, the following precautions are necessary.

(1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5℃ and 35℃ at normal humidity.

(2) The polarizer surface should not come in contact with any other object. It is recommended that they be stored in the container in which they were shipped.

9-6 HANDLING PRECAUTIONS FOR PROTECTION FILM

(1) The protection film is attached to the bezel with a small masking tape. When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.

(2) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the bezel after the protection film is peeled off.

(3) You can remove the glue easily. When the glue remains on the bezel or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.