T6497

Advance Data

Clock Generator Controller for Z80 CPU CMOS

- SGS CMOS Z80 Compatible
- 5 Volt Single Power Supply 5V ± 10%
- Selectable Three Modes
  RUN MODE
  IDLE MODE
  STOP MODE
- Low Power Consumption
  2 mA Typ. @5V @4 MHz (Run Mode)
  500 μA Typ. @5V @4 MHz (Idle Mode)
  10 μA Max. @5V (Stop Mode)
- Extended Operating Temperature Range
  −40°C to 85°C

General Description

The T6497 is a clock generator/controller for SGS CMOS Z80 microprocessor (Z84C00) and peripheral devices. The T6497 has two inputs for choosing one of three modes. When CPU executes HALT instruction, T6497 enters to one of three states described below.

Run Mode. The T6497 is always providing the clock (CLK) to Z80 CPU and peripheral devices. (CPU is actually in HALT state and execute NOP instruction until and interrupt signal or a reset signal is recognized).

Idle Mode. The T6497 stops providing the clock. However only the internal oscillator continues its operation.

Stop Mode. The T6497 stops its operation.

In the STOP MODE, CMOS Z80 microcomputer system may stop its operation, so that power consumption to maintain microcomputer system will be extremely reduced.

An interrupt signal ($\overline{NMI}$ or $\overline{INT}$) or a reset signal ($\overline{RESET}$) makes CPU terminate HALT states. The T6497 is molded in 16-pin standard dual-in-line plastic package.

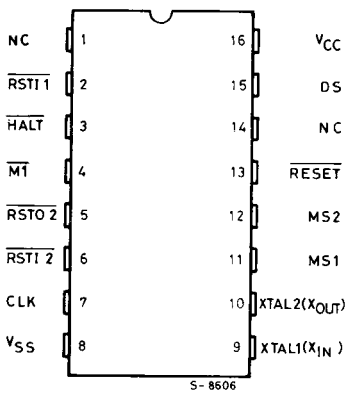


Figure 1. Pin Configuration

General Description (Continued)

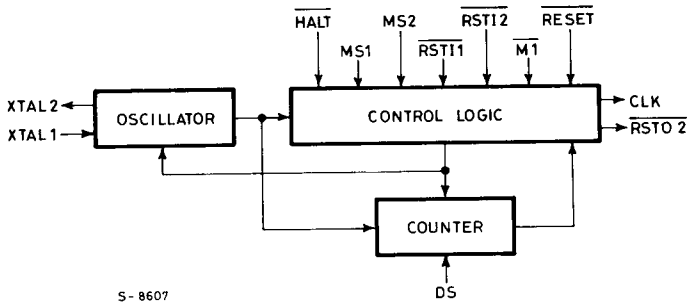


Figure 2. Block Diagram

Pin Names and Pin Description

Pin Name	No. of Pins	I/O, 3-State	
MS1, MS2	2	Input	Input for Mode select.
XTAL1, XTAL2	2	Input	Terminals for a crystal.
$\overline{RSTI1}$	1	Input	Input to resume the CLK. (Level trigger) Usually input for $\overline{INT}$ request.
$\overline{RSTI2}$	1	Input	Input with a latch to resume the CLK. (Edge trigger) Usually input for $\overline{NMI}$ request.
$\overline{RSTO2}$	1	Output	Output corresponding to $\overline{RSTI2}$. Usually output for $\overline{NMI}$ terminal of CPU.
$\overline{M1}$	1	Input	Input for $\overline{M1}$ signal from CPU.
$\overline{HALT}$	1	Input	Input for $\overline{HALT}$ signal from CPU.
$\overline{RESET}$	1	Input	Input signal to resume the CLK. Usually input for $\overline{RESET}$ signal.
CLK	1	Output	Clock output. When HALT instruction is executed by Z80 CPU in either IDLE MODE or STOP MODE, CLK is kept a low level.
DS	1	Input	Input for selecting the number of counter stage. It is used to determine warming-up time when T6497 restarts from STOP MODE.
NC	2	—	No connection.
V_{CC}	1	Power	Single 5V power supply.
V_{SS}	1	Power	Ground reference.

Functional Description

Table 1 illustrates mode select and those functions.
There are two modes (IDLE and STOP) effective when HALT instruction is executed by Z80 CPU. The T6497 continuously provides the system clock (CLK) to Z80 CPU and peripherals unless HALT instruction is executed. In Idle Mode or Stop Mode, $\overline{RSTI1}$, $\overline{RSTI2}$ or $\overline{RESET}$ makes the T6497 resume the CLK.

MS1	MS2	Mode	Functions
1	1	RUN	Always provides the system clock (CLK)
0	(Note) X	IDLE	Stops the system clock (CLK), but keeps the oscillator operation. The CLK is kept low in this mode
1	0	STOP	Stop all the internal operation and the CLK is kept low.

(Note) X = Don't care

Table 1. Operation Modes

Halt Operation in Each Mode

Run Mode (MS1=1, MS2=1). Figure 3 shows a basic timing when HALT instruction is executed. When Z80 CPU fetches the OPcode of HALT instruction (76H) from program memory, $\overline{HALT}$ signal goes active ("0" level) at the timing synchronized with the falling edge of T4 clock cycle and it shows that Z80 CPU is in the HALT state. In this mode, T6497 always provides the CLK.

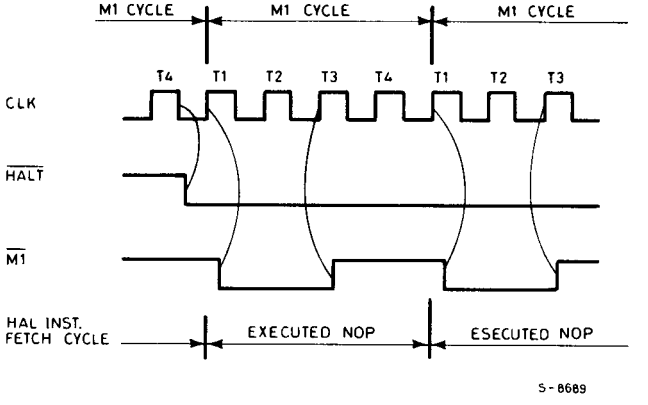


Figure 3. Run Mode

Halt Operation In Each Mode (Continued)

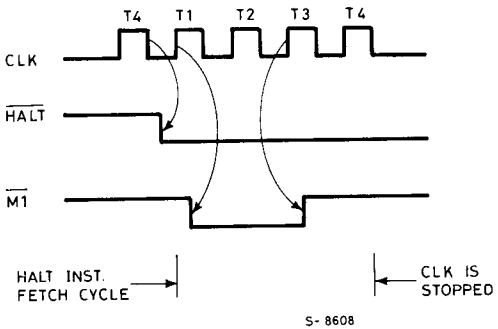
Idle Mode (MS1=0, MS2=don't care). Figure 4 shows a basic timing when HALT instruction is executed in Idle Mode. When Z80 CPU fetches the OPcode of HALT instruction (76H) from program memory, $\overline{HALT}$ signal goes active at the timing sychronized with the falling edge of T4 clock cycle and it shows that Z80 CPU is in the HALT state.

T6497 stops providing the CLK at low level state during the T4 clock cycle of the following machine cycle next to OPcode fetch cycle of HALT instruction.

A rising edge of $\overline{M1}$ signal during active $\overline{HALT}$ signal makes the T6497 stop the CLK.

However the internal oscillator continuously works.

Stop Mode (MS1=1, MS2=0). The same function as IDLE MODE is implemented when $\overline{HALT}$ instruction is executed. (See Figure 4).
Only difference from IDLE MODE is that the T6497 completely stops its operation.



CLK Restart Sequence

There are three inputs to resume the CLK. $\overline{RSTI1}$ (level trigger), $\overline{RSTI2}$ (edge trigger) or $\overline{RESET}$ (level trigger) can be used.

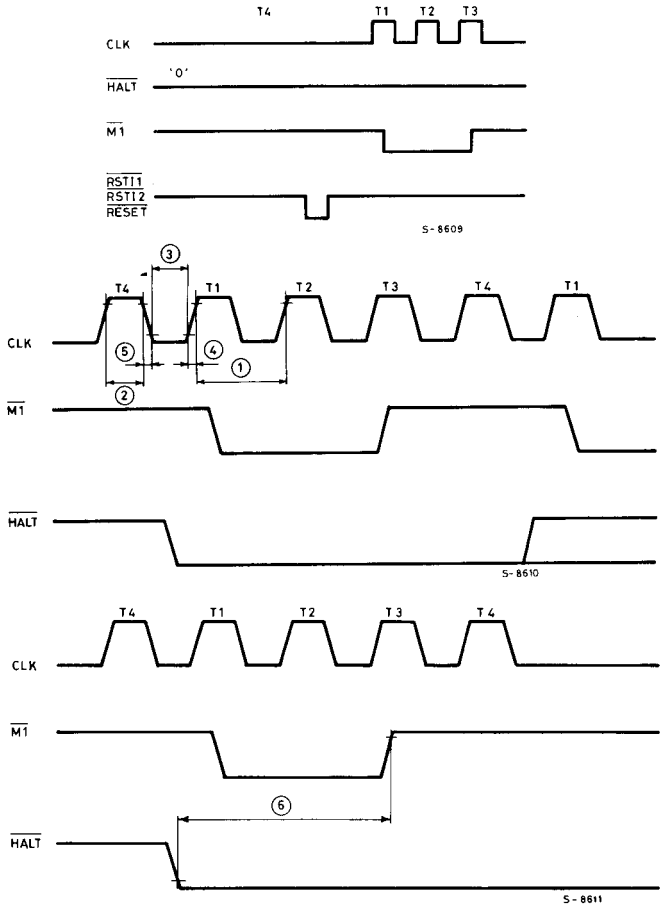
Idle mode. Figure 5 shows the sequence to resume the CLK in IDLE MODE.
In IDLE MODE, the CLK will resume in small delay when a signal to terminate is generated as the internal oscillator is working.

Stop Mode. Figure 6 shows the sequence to resume the CLK in STOP MODE.
As the T6497 needs warming-up time to stabilize the frequency it uses the counter when a restart signal is generated.

DS (Divider Select) input must be used to determine warming-up time. External crystal frequency is divided by either 2^{17} or 2^{14}.

Figure 7 shows the block diagram regarding counter and Table 2 illustrates the warming-up time.

CLK Restart Sequence (Continued)



DS	Counter Output	Warming-up Time		
		f_{XTAL}=4 MHz	f_{XTAL}=2.5 MHz	f_{XTAL}=400 KHz
0	2^{18}	32.8 ms	52.4 ms	328 ms
1	2^{15}	4 ms	6.6 ms	40 ms

Table 2. Warming-up Time in Stop Mode

CLK Restart Sequence (Continued)

Note (1)

Note that either interrupt input or $\overline{\text{RESET}}$ input must be generated to terminate the HALT state of Z80 CPU, where CLK is stopped at a low level during T4 state, in either IDLE MODE or STOP MODE.

(1) In case of $\overline{\text{RESET}}$ input signal is connected with both Z80 CPU $\overline{\text{RESET}}$ terminal and T6497 $\overline{\text{RESET}}$ terminal.

$\overline{\text{RESET}}$ input signal to Z80 CPU must be kept active (Low) during at least three clock cycles. When $\overline{\text{RESET}}$ input signal goes inactive, CPU fetches the first OPcode from address 0000H after at least two dummy clock cycles.
Thus CPU will terminate HALT state.
Note that if $\overline{\text{RESET}}$ input is connected with both Z80 CPU $\overline{\text{RESET}}$ terminal and T6497 $\overline{\text{RESET}}$ terminal, the $\overline{\text{RESET}}$ signal should be active for enough period to reset the Z80 CPU surely at power on reset. (See Figure 8.)

(2) In case of using an interrupt signal

Figure 9 shows the timing to resume the CLK and to terminate HALT state by an interrupt signal.
$\overline{\text{RSTI1}}$ or $\overline{\text{RSTI2}}$ input makes T6497 resume the CLK, And then an interrupt signal ($\overline{\text{INT}}$ or $\overline{\text{NMI}}$) must be generated to terminate HALT state.
Note that Z80 CPU in HALT state executes NOP instruction unless an interrupt is recognized.

a) In case of using $\overline{\text{NMI}}$

$\overline{\text{NMI}}$ of Z80 CPU is an input (edge trigger) with a latch. If active (low) $\overline{\text{NMI}}$ signal is accepted prior to sampling timing for an interrupt request signal, Z80 CPU recognizes $\overline{\text{NMI}}$. $\overline{\text{RSTI2}}$ of T6497 may be used as $\overline{\text{NMI}}$ input, since $\overline{\text{RSTI2}}$ has a latch and $\overline{\text{RSTO2}}$ may be connected with $\overline{\text{NMI}}$ input of Z80 CPU.

b) In case of using $\overline{\text{INT}}$

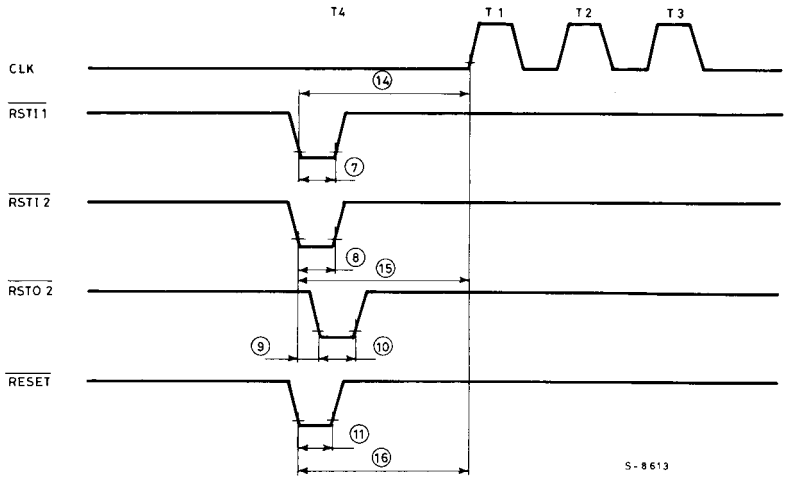
In maskable interrupt ($\overline{\text{INT}}$), interrupt enable flip flop (IFF) must be set by software before receiving an interrupt signal.

Figure 9 shows the timing when an interrupt signal is connected with both $\overline{\text{RSTI1}}$ terminal of T6497 and $\overline{\text{INT}}$ terminal of Z80 CPU.

Note 2)

The internal counter of T6497 to determine warming-up time is not used in Stop Mode when $\overline{\text{RESET}}$ input is activated to resume the clock, so Z80 CPU may not restart properly due to unstable clok when the oscillator restarts.
Therefore connect $\overline{\text{RESET}}$ input of T6497 with that of Z80 CPU when $\overline{\text{RESET}}$ input of T6497 is used to restart the clock in Stop Mode.
Also it is suggested that $\overline{\text{RESET}}$ input be kept low for enough period to initialize Z80 CPU.

CLK Restart Sequence (Continued)

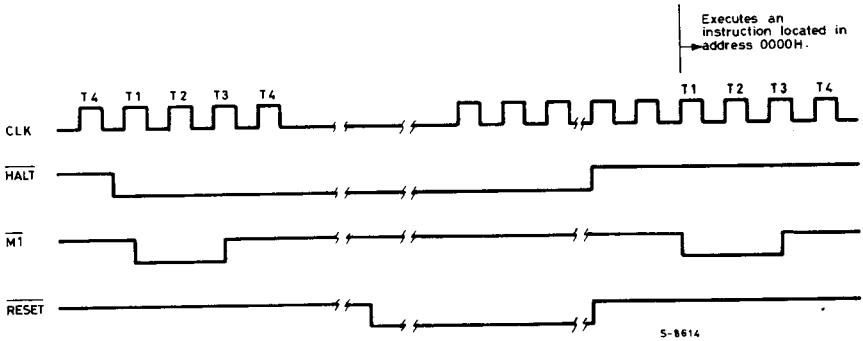


Note the followings when release from power down state.

(1) When external oscillator has been stopped to enter power down state, some warming-up time may be required to obtain precious and stable system clock for release from power down state.

(2) When HALT instruction is executed to enter power down state, Z80 CPU will enter HALT state. An interrupt signal ($\overline{NMI}$ or $\overline{INT}$) or $\overline{RESET}$ signal must be generated to Z80 CPU after the system clock is supplied to release power down state. Otherwise Z80 CPU is still in HALT state even if the system clock is supplied.

CLK Restart Sequence (Continued)



Release from Power Down State for CMOS Z80

The system clock must be supplied to Z80 CPU to release power down state. When the system clock is supplied to CLK terminal of Z80 CPU, CPU restarts operation continuously from the state when power down function has been implemented.

Absolute Maximum Ratings

Symbol	Item	Rating
V_{CC}	V_{CC} Supply Voltage with respect to V_{SS}	−0.5V to 7.0V
V_{IN}	Input Voltage	−0.5V to V_{CC} + 0.5V
I_{IN}	Input Current	±10mA
P_D	Power Dissipation (TA-85°C)	250mW
T_{SOLDER}	Soldering Temperature (Soldering Time 10 sec.)	260°C
T_{STG}	Storage Temperature	−65°C to 150°C
T_{OPR}	Operating Temperature	−40°C to 85°C

DC Characteristics (TA = −40°C to 85°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

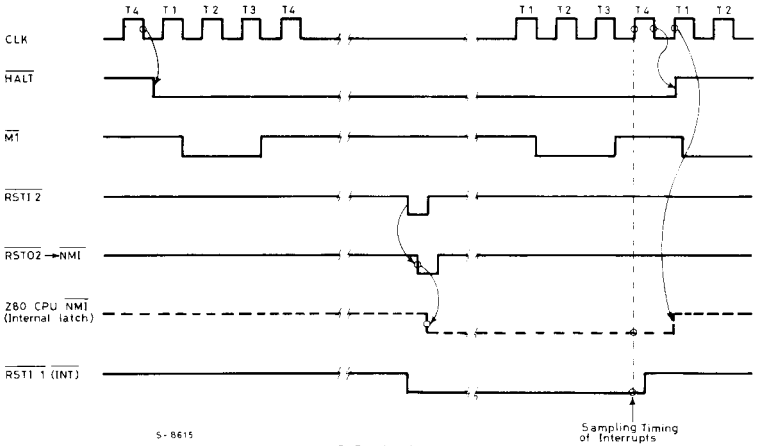
Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{IL}	Input Low Voltage (except XTAL1,2)	−0.5	—	0.8	V	
V_{IH}	Input High Voltage (except XTAL1,2)	2.2	—	V_{CC}	V	
V_{OLC}	Output Low Voltage (CLK)	—	—	0.4	V	I_{OL} = 2.0mA
V_{OL}	Output Low Voltage (except CLK)	—	—	0.4	V	I_{OL} = 2.0mA
V_{OHC}	Output High Voltage (CLK)	V_{CC} − 0.6	—	—	V	I_{OH} = 250μA
V_{OH1}	Ouput High Voltage (except CLK)	2.4	—	—	V	I_{OH} = −1.6mA
V_{OH2}	Output High Voltage (except CLK)	V_{CC} − 0.8	—	—	V	I_{OH} = −250μA
I_{IL}	Input Leakage	—	—	±1	μA	$V_{SS} \le V_{IN} \le V_{CC}$
I_{OL}	Output Leakage	—	—	±1	μA	V_{SS} + 0.4V ≤ $V_{IN} \le V_{CC}$
I_{CC1}	V_{CC} Supply Current (NORMAL/RUN MODE)	—	2	4	mA	V_{CC} = 5V f_{XTAL} = 4 MHz $V_{IH} = V_{CC} - 0.2V$ V_{IL} = 0.2V
I_{CC2}	V_{CC} Supply Current (STOP MODE)	—	0.3	10	μA	V_{CC} = 5V $V_{IH} = V_{CC} - 0.2V$ V_{IL} = 0.2V
I_{CC3}	V_{CC} Supply Current (IDLE MODE)	—	0.5	1	mA	V_{CC} = 5V f_{XTAL} = 4 MHz $V_{IH} = V_{CC} - 0.2V$ V_{IL} = 0.2V

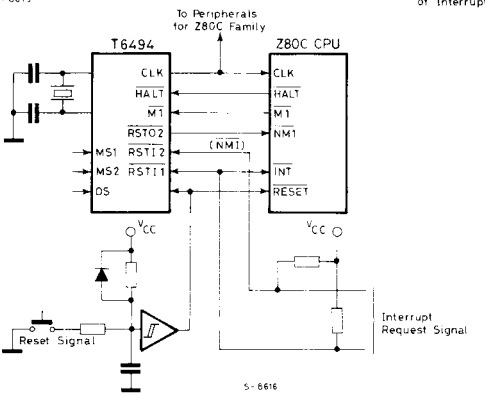
AC Characteristics (TA = −40°C to 85°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

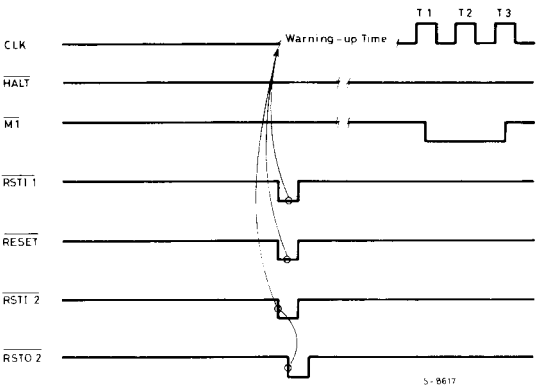
Number	Symbol	Parameter		Min	Typ	Max	Unit	Test Conditions
1	TcC	CLK Cycle Time		250	—	—	ns	
2	TwCh	CLK Pulse Width (High)		110	—	—	ns	
3	TwCl	CLK Pulse Width (Low)		110	—	—	ns	
4	TrC	CLK Rise Time		—	—	15	ns	
5	TfC	CLK Fall Time		—	—	15	ns	
6	TsHALT(M1r)	$\overline{HALT}$ Setup Time to M1↑		10	—	—	ns	
7	TwRSTI1	$\overline{RSTI1}$ Pulse Width (Low)		80	—	—	ns	
8	TwRSTI2	$\overline{RSTI2}$ Pulse Width (Low)		200	—	—	ns	
9	TdRSTO2 (RSTI2f)	$\overline{RSTI2}$ to $\overline{RSTO2}$↓ Delay		—	—	100	ns	
10	TwRSTO2	$\overline{RSTO2}$ Pulse Width (Low)		80	—	—	ns	C_L = 100pF
11	TwRESET	$\overline{RESET}$ Pulse Width (Low)		80	—	—	ns	
12	TRST1S	CLK Restart Delay by $\overline{RSTI1}$ (Stop Mode)	DS = 0	—	$(2^{17}+2.5)$TcC	—	ns	
			DS = 1	—	$(2^{14}+2.5)$TcC	—	ns	
13	TRST2S	CLK Restart Delay by $\overline{RSTI2}$ (Stop Mode)	DS = 0	—	$(2^{17}+2.5)$TcC	—	ns	
			DS = 1	—	$(2^{14}+2.5)$TcC	—	ns	
14	TRST1I	CLK Restart Delay by $\overline{RSTI1}$ (Idle Mode)		—	2.5 TcC	—	ns	
15	TRST2I	CLK Restart Delay by $\overline{RSTI2}$ (Idle Mode)		—	2.5 TcC	—	ns	
16	TRESETI	CLK Restart Delay by $\overline{RESET}$ (Idle Mode)		—	1 TcC	—	ns	

Note) A.C. Testing: Inputs are driven at 2.4V for a logic "1" and 0.4V for a logic "0". Timing measurements are made at 2.2V for a logic "1" and 0.8V for a logic "0" except CLK output. CLK is made at V_{CC} − 0.6V for a logic "1" and 0.4V for a logic "0".

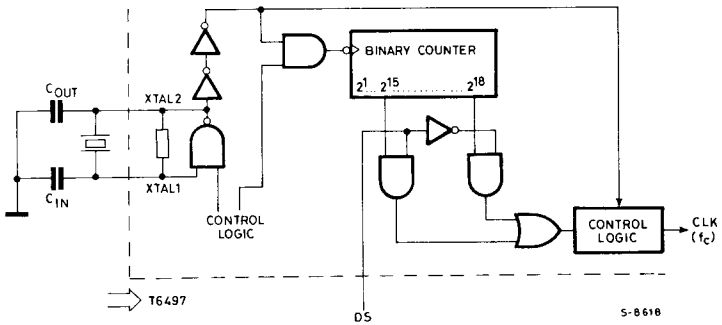
Timing Waveforms







Timing Waveforms (Continued)



Ordering Information

Type	Package	Temp.	Clock	Description
T6497 B6	Plastic	−40°/+85°C	4 MHz	Clock Generator Controller for Z80 CMOS