Model Name: T650QVJ02.0

Issue Date : 2013/04/23

( )Preliminary Specifications
(*)Final Specifications

Customer Signature	Date	AUO	Date
Approved By		Approval By PM Director CP Wang	
Note		Reviewed By RD Director Eugene CC Chen Reviewed By Project Leader Stanley Lo	
		Prepared By PM Mick Chen	

Contents

Record of Revision

Version	Date	Page	Description
0.1	2013/01/14		First release
0.2	2013/01/29	7	Update Part 3 electrical spec
0.3	2013/01/29	20	Update LCD power connector
0.4	2013/01/30	31	Update mechanical drawing
0.5	2013/01/31	7	Update I2C spec
0.6	2013/01/31	7,11	Update DC characteristics & LVDS 51pin assignment
0.7	2013/02/07	11	Change 51pin; pin 7 function decription
0.8	2013/03/26	7	DC/AC characteristics
		14	Timing spec
		15,16	Timing waveform
		18	Update Power sequence
		23	Revise Color coordination spec
		11	51pin, pin1 change
0.9	2013/04/12	11	51pin, pin3 change
1.0	2013/04/23	34	Revise safety information: E204358→E204356

1. General Description

This specification applies to the 65 inch Color TFT-LCD Module T650QVJ02.0. This LCD module has a TFT active matrix type liquid crystal panel 3,840x2,160 pixels, and diagonal size of 65 inch. This module supports 3,840x2,160 mode. Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 10-bit gray scale signal for each dot.

The T650QVJ02.0 has been designed to apply the 10-bit LVDS interface method. It is intended to support displays where high brightness, wide viewing angle, high color saturation, and high color depth are very important. Also, 3D function is also embedded into front glass as pattern retarder.

*** General Information**

Items	Specification	Unit	Note
Active Screen Size	65	inch	
Display Area	1428.48(H) x 803.52(V)	mm	
Outline Dimension	1454.3(H) x 831.5 (V) x 18(D)	mm	D: front bezel to back bezel
Driver Element	a-Si TFT active matrix		
Bezel Opening	**1434.5 (H) x 809.6 (V)**	mm	
Display Colors	10 bit, 16.7M	Colors	
Number of Pixels	3840x2160	Pixel	
Pixel Pitch	0.372 (H) x 0.372(W)	mm	
Pixel Arrangement	RGB vertical stripe		
Display Operation Mode	Normally Black		
Rotate Function	Unachievable		Note 1
Display Orientation	Signal input with “ABC”		Note 2

Note 1: Rotate Function refers to LCD display could be able to rotate.

Note 2: LCD display as below illustrated when signal input with “ABC”.

2. Absolute Maximum Ratings

The followings are maximum values which, if exceeded, may cause faulty operation or damage to the unit

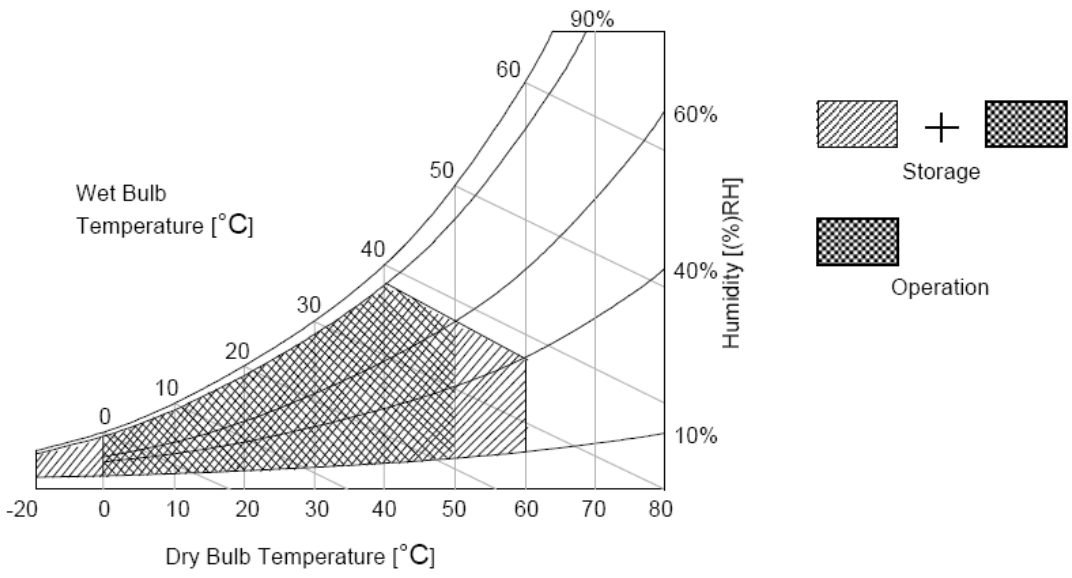
Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	V_{DD}	-0.3	14	[Volt]	Note 1
Input Voltage of Signal	Vin	-0.3	4	[Volt]	Note 1
Operating Temperature	TOP	0	+50	[°C]	Note 2
Operating Humidity	HOP	10	90	[%RH]	Note 2
Storage Temperature	TST	-20	+60	[°C]	Note 2
Storage Humidity	HST	10	90	[%RH]	Note 2
Panel Surface Temperature	PST		65	[°C]	Note 3

Note 1: Duration:50 msec.

Note 2 : Maximum Wet-Bulb should be 39℃ and No condensation.

The relative humidity must not exceed 90% non-condensing at temperatures of 40℃ or less. At temperatures greater than 40℃, the wet bulb temperature must not exceed 39℃.

Note 3: Surface temperature is measured at 50℃ Dry condition



3. Electrical Specification

The T650QVJ02.0 requires two power inputs. One is employed to power the LCD electronics and to drive the TFT array and liquid crystal. The other is to power Back Light Unit.

3.0 ASIC feature

- Input resolution FHD120Hz / UHD 30Hz/ 4k1k 30Hz switchable
- MEMC Function with High/Middle/Low level
- 2D / 3D switchable
- Video Mute Function
- OSD protection function

3.1 Electrical Characteristics

3.1.1: DC Characteristics

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max		
LCD							
Power Supply Input Voltage (for input power=12V)		V_{DD}	10.8	12	13.2	V_{DC}	
Power Supply Input Current (Define to section:1.1)		I_{DD}	--	1.8	3.7	A	1
Inrush Current (Define to section:1.1)		I_{RUSH}	--	--	5	A	2
Permissible Ripple of Power Supply Input Voltage (for input power=12V)		V_{RP}	--	--	V_{DD} * 5%	mV_{pk-pk}	3
LVDS Interface	Input Differential Voltage	$\|V_{ID}\|$	200	400	600	mV_{DC}	4
	Differential Input High Threshold Voltage	V_{TH}	+100	--	+300	mV_{DC}	4
	Differential Input Low Threshold Voltage	V_{TL}	-300	--	-100	mV_{DC}	4
	Input Common Mode Voltage	V_{ICM}	1.1	1.25	1.4	V_{DC}	4
CMOS Interface	Input High Threshold Voltage	V_{IH} (High)	2.0	--	3.3	V_{DC}	5
	Input Low Threshold Voltage	V_{IL} (Low)	0	--	0.8	V_{DC}	5

3.1.2: AC Characteristics

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max		
LVDS Interface	Receiver Clock : Spread Spectrum Modulation range	Fclk_ss	Fclk -3%	--	Fclk +3%	MHz	6
	Receiver Clock : Spread Spectrum Modulation frequency	Fss	50	--	200	KHz	6
	Receiver Data Input Margin Fclk = 150 MHz Fclk = 85 MHz	tRMG	 -0.15 -0.4	 -- --	 0.15 0.4	ns	7
I2C Interface	SCL clock frequency	F_{SCL}	--	--	400	KHZ	
	I2C clock high level	T_{SCHi}	0.6	--	--	us	
	I2C clock low level	T_{SCLo}	1.3	--	--	us	
	I2C data setup time	T_{SDS}	0.1	--	--	us	
	I2C data hold time	T_{SDH}	0	--	900	us	
	SDA and SCL rise time	T_R	--	--	0.3	us	
	SDA and SCL fall time	T_F	--	--	0.3	us	

3.1.3: Driver Characteristics

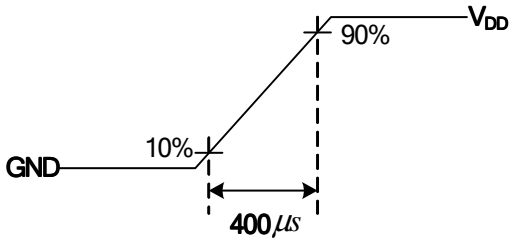
Item	Symbol	Min	Max	Unit	condition
Driver Surface Temperature	DST		100	[℃]	Note

Any point on the driver surface must be less than 100℃ under any condition

Note:

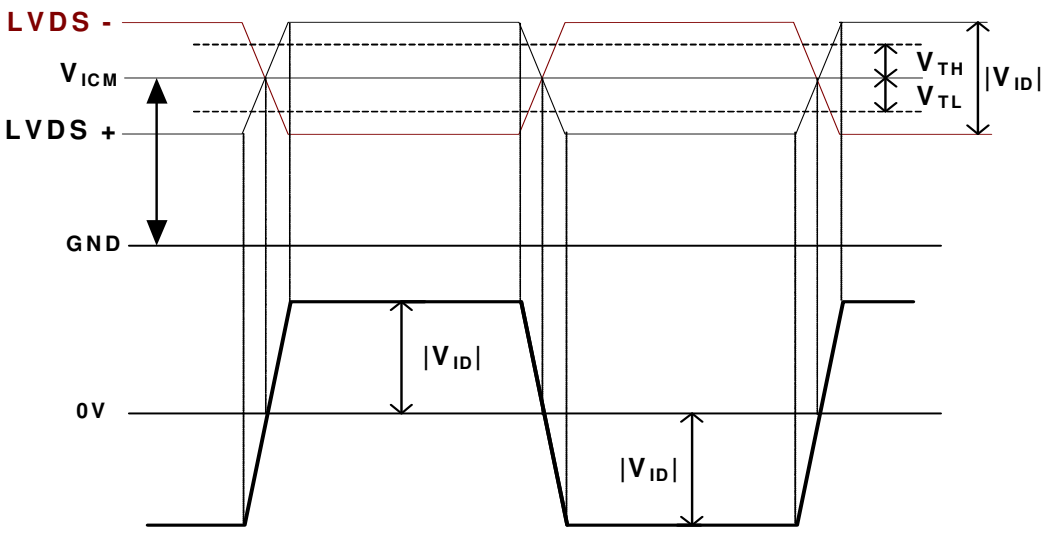
1. Test Condition:
(1) V_{DD} = 12.0V
(2) Fv = Type Timing 120Hz
(3) Fclk= Max freq.
(4) Temperature = 25 ℃
(5) Typ. Input current : White Pattern
Max. Input current: Heavy loading pattern defined by AUO
>> refer to "Section:3.3 Signal Timing Specification, Typical timing"

2. Measurement condition : Rising time = 400us

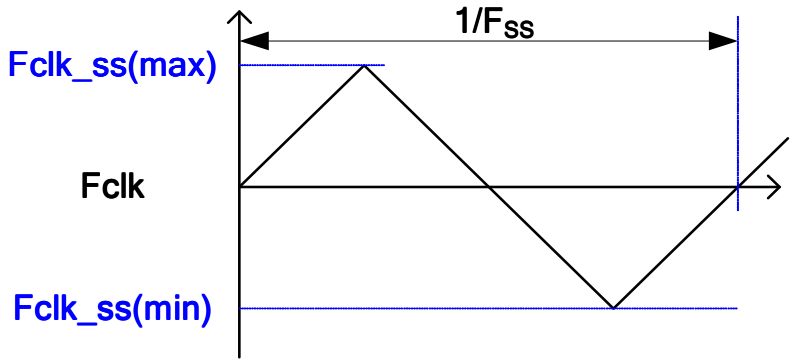


3. Test Condition:
(1) The measure point of V_{RP} is in LCM side after connecting the System Board and LCM.
(2) Under Max. Input current spec. condition.

4. V_{ICM} = 1.25V

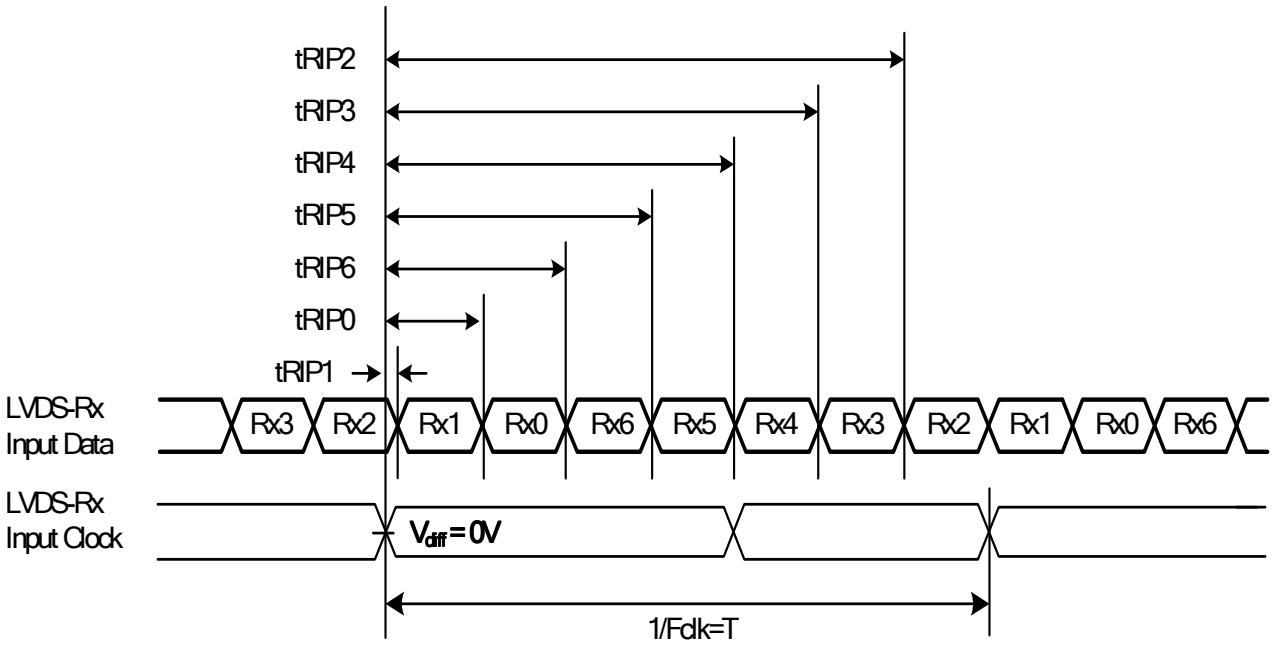


5. The measure points of V_{IH} and V_{IL} are in LCM side after connecting the System Board and LCM.
6. LVDS Receiver Clock SSCG (Spread spectrum clock generator) is defined as below figures.



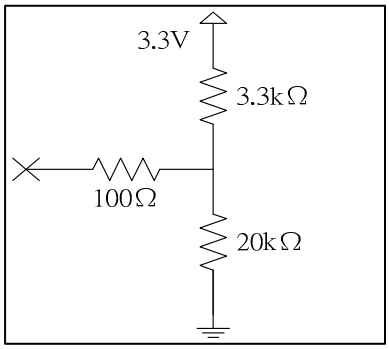
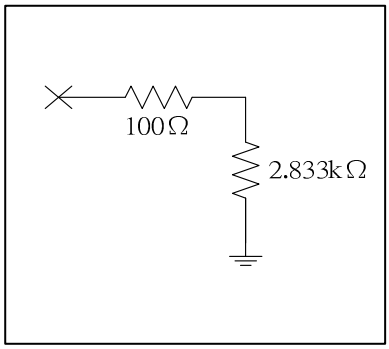
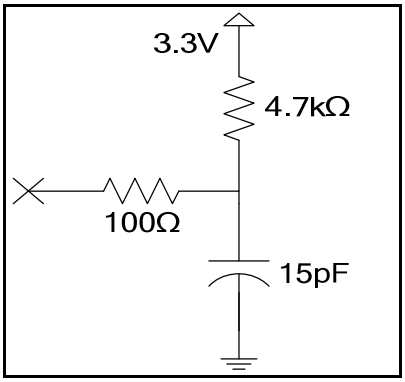
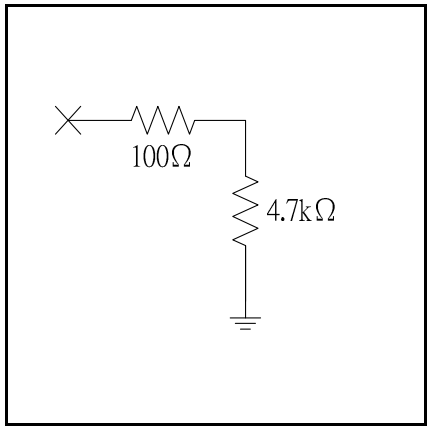
7. Receiver Data Input Margin

Parameter	Symbol	Rating			Unit	Note
		Min	Type	Max		
Input Clock Frequency	Fclk	Fclk (min)	--	Fclk (max)	MHz	**T=1/Fclk**
Input Data Position0	tRIP1	-|tRMG|	0	|tRMG|	ns	
Input Data Position1	tRIP0	T/7-|tRMG|	T/7	T/7+|tRMG|	ns	
Input Data Position2	tRIP6	2T/7-|tRMG|	2T/7	2T/7+|tRMG|	ns	
Input Data Position3	tRIP5	3T/7-|tRMG|	3T/7	3T/7+|tRMG|	ns	
Input Data Position4	tRIP4	4T/7-|tRMG|	4T/7	4T/7+|tRMG|	ns	
Input Data Position5	tRIP3	5T/7-|tRMG|	5T/7	5T/7+|tRMG|	ns	
Input Data Position6	tRIP2	6T/7-|tRMG|	6T/7	6T/7+|tRMG|	ns	



3.2 Interface Connections

3.2.1: LVDS connector control and I2C pin description

Note * : Open/High(3.3V) 	**Note ** : Open/Low(GND)** 
Note ** : SCL/SDA** 	**Note ***** : WP** 

3.2.2: LVDS Pin-Assignment

- LCD connector: 187059-51221-1 (JAE, LVDS connector)
  187060-41221-1 (JAE, LVDS connector)
- Mating connector:

PIN	Symbol	Description	PIN	Symbol	Description
1	N.C	AUO Internal Use Only	26	GND	Ground
2	SCL	I2C Serial Clock	27	GND	Ground
3	N.C	AUO Internal Use Only	28	CH2_0-	LVDS Channel 2, Signal 0-
4	SDA	I2C Serial Data	29	CH2_0+	LVDS Channel 2, Signal 0+
5	N.C	AUO Internal Use Only	30	CH2_1-	LVDS Channel 2, Signal 1-
6	N.C	AUO Internal Use Only	31	CH2_1+	LVDS Channel 2, Signal 1+
7	SELLVDS	LVDS Format Select Open/High(3.3V) for JEIDA, Low(GND) for NS	32	CH2_2-	LVDS Channel 2, Signal 2-
8	N.C	AUO Internal Use Only	33	CH2_2+	LVDS Channel 2, Signal 2+
9	N.C	AUO Internal Use Only	34	GND	Ground
10	N.C	AUO Internal Use Only	35	CH2_CLK-	LVDS Channel 2, Clock -
11	GND	Ground	36	CH2_CLK+	LVDS Channel 2, Clock +
12	CH1_0-	LVDS Channel 1, Signal 0-	37	GND	Ground
13	CH1_0+	LVDS Channel 1, Signal 0+	38	CH2_3-	LVDS Channel 2, Signal 3-
14	CH1_1-	LVDS Channel 1, Signal 1-	39	CH2_3+	LVDS Channel 2, Signal 3+
15	CH1_1+	LVDS Channel 1, Signal 1+	40	CH2_4-	LVDS Channel 2, Signal 4-
16	CH1_2-	LVDS Channel 1, Signal 2-	41	CH2_4+	LVDS Channel 2, Signal 4+
17	CH1_2+	LVDS Channel 1, Signal 2+	42	GND	Ground
18	GND	Ground	43	N.C	AUO Internal Use Only
19	CH1_CLK-	LVDS Channel 1, Clock -	44	GND	Ground
20	CH1_CLK+	LVDS Channel 1, Clock +	45	GND	Ground
21	GND	Ground	46	GND	Ground
22	CH1_3-	LVDS Channel 1, Signal 3-	47	N.C.	No connection (for AUO test only. Do not connect)
23	CH1_3+	LVDS Channel 1, Signal 3+	48	N.C.	No connection (for AUO test only. Do not connect)
24	CH1_4-	LVDS Channel 1, Signal 4-	49	N.C.	No connection (for AUO test only. Do not connect)
25	CH1_4+	LVDS Channel 1, Signal 4+	50	N.C.	No connection (for AUO test only. Do not connect)
			51	N.C.	No connection (for AUO test only. Do not connect)

Note: N.C. : please leave this pin unoccupied. It can not be connected by any signal (Low/GND/High).

PIN	Symbol	Description	PIN	Symbol	Description
1	N.C.	No connection (for AUO test only. Do not connect)	21	CH3_3+	LVDS Channel 3, Signal 3+
2	N.C.	No connection (for AUO test only. Do not connect)	22	CH3_4-	LVDS Channel 3,Signal 4-
3	N.C.	No connection (for AUO test only. Do not connect)	23	CH3_4+	LVDS Channel 3,Signal 4+
4	N.C.	No connection (for AUO test only. Do not connect)	24	GND	Ground
5	N.C.	No connection (for AUO test only. Do not connect)	25	GND	Ground
6	N.C.	No connection (for AUO test only. Do not connect)	26	CH4_0-	LVDS Channel 4, Signal 0-
7	N.C.	No connection (for AUO test only. Do not connect)	27	CH4_0+	LVDS Channel 4, Signal 0+
8	N.C.	No connection (for AUO test only. Do not connect)	28	CH4_1-	LVDS Channel 4, Signal 1-
9	GND	Ground	29	CH4_1+	LVDS Channel 4, Signal 1+
10	CH3_0-	LVDS Channel 3, Signal 0-	30	CH4_2-	LVDS Channel 4, Signal 2-
11	CH3_0+	LVDS Channel 3, Signal 0+	31	CH4_2+	LVDS Channel 4, Signal 2+
12	CH3_1-	LVDS Channel 3, Signal 1-	32	GND	Ground
13	CH3_1+	LVDS Channel 3, Signal 1+	33	CH4_CLK-	LVDS Channel 4, Clock -
14	CH3_2-	LVDS Channel 3, Signal 2-	34	CH4_CLK+	LVDS Channel 4, Clock +
15	CH3_2+	LVDS Channel 3, Signal 2+	35	GND	Ground
16	GND	Ground	36	CH4_3-	LVDS Channel 4, Signal 3-
17	CH3_CLK-	LVDS Channel 3, Clock -	37	CH4_3+	LVDS Channel 4, Signal 3+
18	CH3_CLK+	LVDS Channel 3, Clock +	38	CH4_4-	LVDS Channel 4,Signal 4-
19	GND	Ground	39	CH4_4+	LVDS Channel 4,Signal 4+
20	CH3_3-	LVDS Channel 3, Signal 3-	40	GND	Ground
			41	GND	Ground

Note: N.C. : please leave this pin unoccupied. It can not be connected by any signal (Low/GND/High).

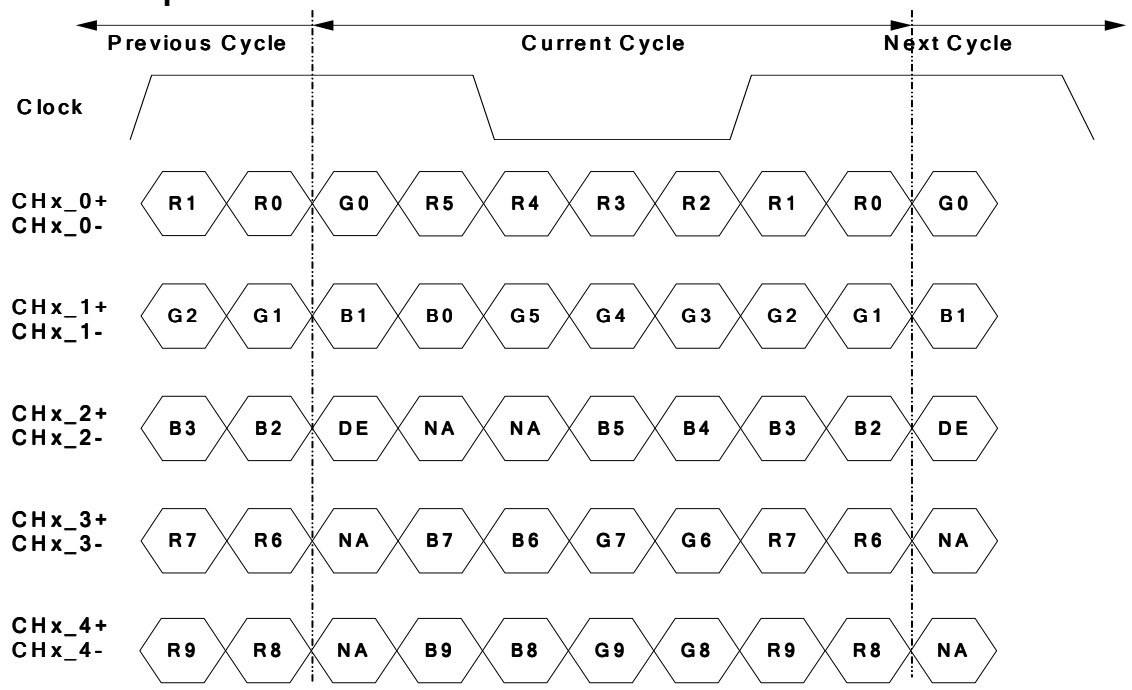
- LCD Power connector:

  Power CN(12pin)：MSAK242151P12R (STM)

PIN	Symbol	Description
1	PWR Power 12V IN	PWR Power 12V IN
2	PWR Power 12V IN	PWR Power 12V IN
3	PWR Power 12V IN	PWR Power 12V IN
4	PWR Power 12V IN	PWR Power 12V IN
5	PWR Power 12V IN	PWR Power 12V IN
6	NC	NC Pin
7	NC	NC Pin
8	GND	Ground
9	GND	Ground
10	GND	Ground
11	GND	Ground
12	GND	Ground

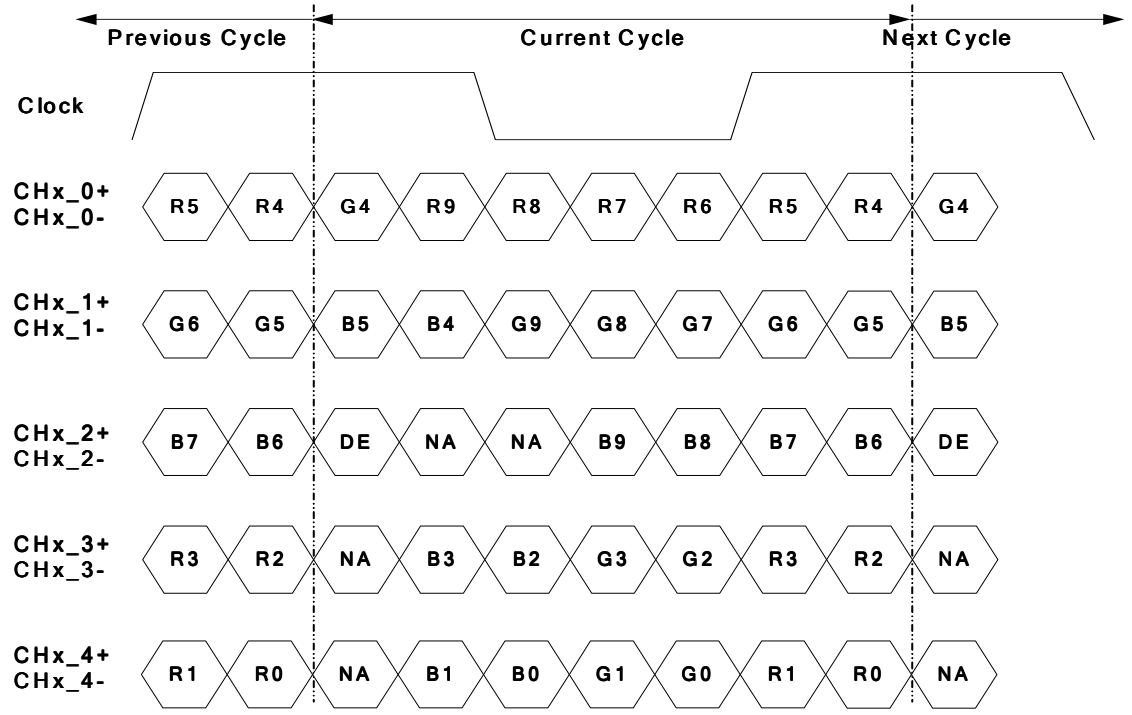
3.2.3: LVDS Option

■ **LVDS Option = Low➔NS**



Note: x = 1, 2, 3, 4…

■ **LVDS Option = High/Open➔JEIDA**



Note: x = 1, 2, 3, 4

3.3 Signal Timing Specification

UHD (4K2K) 3840x2160 LVDS 4ch Timing Table (960x2160 @30Hz)

Input Timing	Vertical Section					Horizontal Section					Frequency			
	Active	Period Tv	Blanking Tblk(v)			Active	Period Th	Blanking Tblk(h)			Pixel Clock (MHz)			Frame
	Tdisp(v)	Typ.	Min.	Typ.	Max.	Tdisp(h)	Typ.	Min.	Typ.	Max.	Min.	Typ.	Max.	Rate (Hz)
4K2K30Hz	2160	2250	76	90	104	3840	4400	516	560	604	233.8	-	237.6	24
											243.7	-	247.5	25
											292.2	-	297.2	30

FHD 1920x1080 LVDS 4ch Timing Table (480x1080 @120Hz)

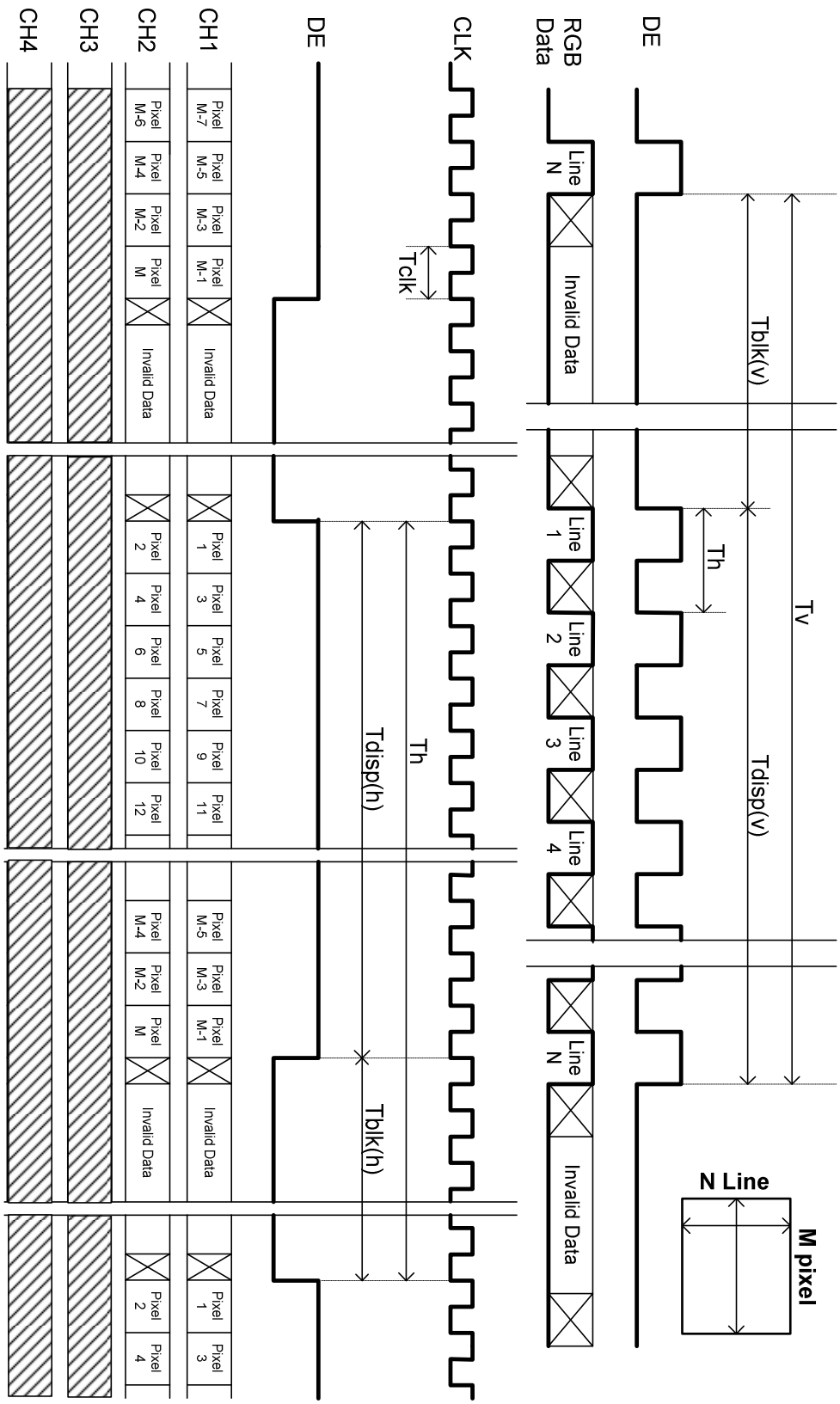
Input Timing	Vertical Section					Horizontal Section					Frequency			
	Active	Period Tv	Blanking Tblk(v)			Active	Period Th	Blanking Tblk(h)			Pixel Clock (MHz)			Frame
	Tdisp(v)	Typ.	Min.	Typ.	Max.	Tdisp(h)	Typ.	Min.	Typ.	Max.	Min.	Typ.	Max.	Rate (Hz)
FHD120Hz	1080	1125	38	45	52	1920	2200	252	280	304	234	-	237.6	96
											243.9	-	247.5	100
											293.5	-	297.2	120

4K1K 3840x1080 LVDS 2ch Timing Table (1920x1080 @30Hz)

Input Timing	Vertical Section					Horizontal Section					Frequency			
	Active	Period Tv	Blanking Tblk(v)			Active	Period Th	Blanking Tblk(h)			Pixel Clock (MHz)			Frame
	Tdisp(v)	Typ.	Min.	Typ.	Max.	Tdisp(h)	Typ.	Min.	Typ.	Max.	Min.	Typ.	Max.	Rate (Hz)
4K1K30Hz	1080	1125	38	45	52	3840	4400	516	560	604	116.9	-	118.8	24
											121.8	-	123.8	25
											146.1	-	148.5	30

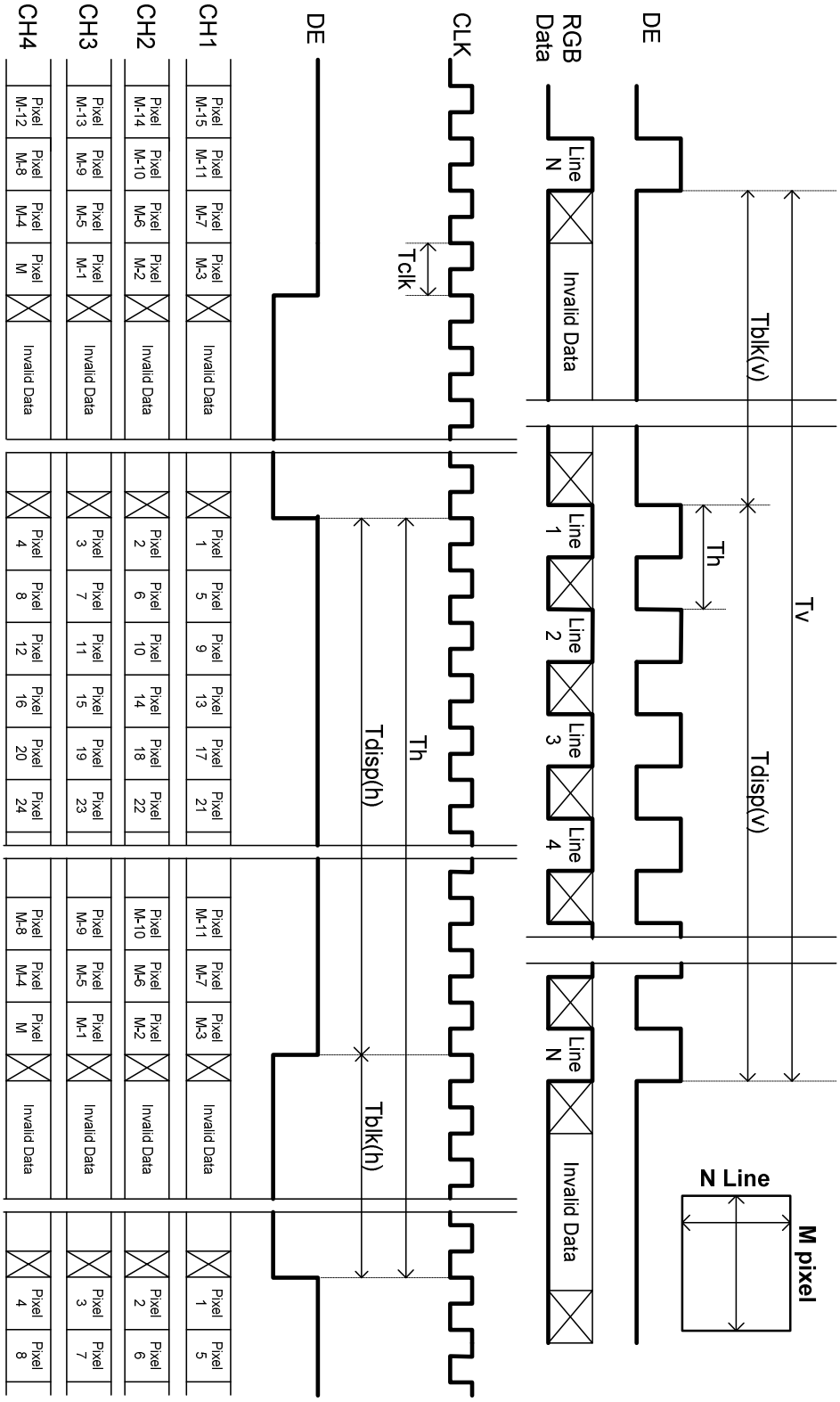
3.4 Signal Timing Waveforms

- 4K1K 3840x1080 LVDS 2ch Timing Table (1920x1080 @30Hz)



- FHD 1920x1080 LVDS 4ch Timing Table (480x1080 @120Hz)

- QFHD 3840x2160 LVDS 4ch Timing Table (960x2160 @30Hz)



3.5 Color Input Data Reference

The brightness of each primary color (red, green and blue) is based on the 10 bit gray scale data input for the color; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

COLOR DATA REFERENCE

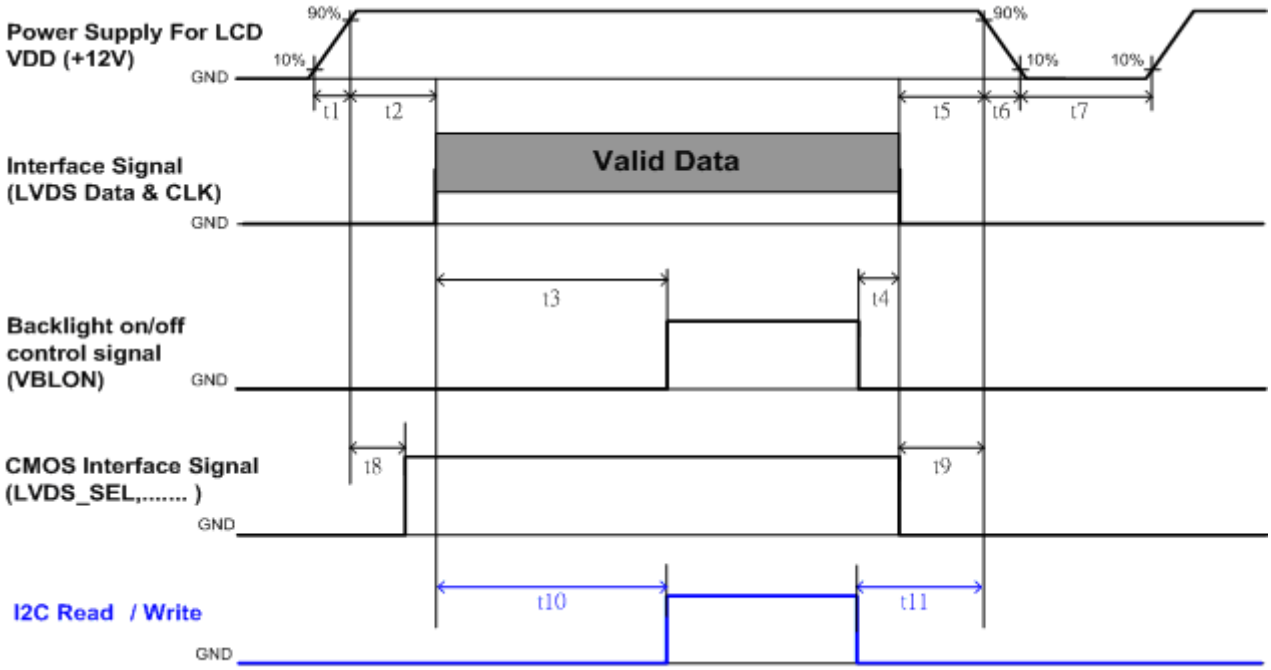
Color		Input Color Data																													
		RED										GREEN										BLUE									
		MSB									LSB	MSB									LSB	MSB									LSB
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue(1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R	RED(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(001)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	RED(1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
G	GREEN(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

	GREEN(1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	GREEN(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
B	BLUE(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

	BLUE(1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	BLUE(1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

3.6 Power Sequence for LCD



Parameter	Values			Unit
	Min.	Type.	Max.	
t1	0.4	---	30	ms
t2	0.1	---	50	ms
t3	2000	---	---	ms
t4	0 *1	---	---	ms
t5	0	---	---	ms
t6	---	---	--- *2	ms
t7	500	---	---	ms
t8	10 *3	---	50	ms
t9	0	---	---	ms
t10	2000	---	---	ms
t11	150	---	---	ms

Note:
(1) t4=0 : concern for residual pattern before BLU turn off.
(2) t6 : voltage of VDD must decay smoothly after power-off. (customer system decide this value)
(3) When CMOS Interface signal is N.C. (no connection), opened in Transmitted end, t8 timing spec can be negligible.

3.7 Backlight Specification

The backlight unit contains 8pcs light bar.

3.7.1 Light bar Driven Condition

	Item	Symbol		Condition	Spec			Unit	Note
					Min	Typ	Max		
1	Input Voltage	VDDB		-	22.8	24	25.2	VDC	-
2	Input Current	I_{DDB}		VDDB=24V		**7.23**	**7.77**	ADC	1
3	Input Power	P_{DDB}		VDDB=24V		**173.6**	**186.5**	W	1
4	Inrush Current	I_{RUSH}		VDDB=24V			**16.3**	Apeak	2
5	Control signal voltage	V_{Signal}	Hi	VDDB=24V	2	-	5.5	VDC	-
			Low		0	-	0.8		3
6	Control signal current	I_{Signal}		VDDB=24V	-	-	1.5	mA	-
7	External PWM Duty ratio (input duty ratio)	D_EPWM		VDDB=24V	0	-	100	%	4,5
8	External PWM Frequency	F_EPWM		VDDB=24V	140	180	240	Hz	4,5
9	DET status signal	DET	HI	VDDB=24V	Open Collector			VDC	6
			Lo		0	-	0.8	VDC	6
10	Input Impedance	Rin		VDDB=24V	300			Kohm	-

Note 1: Dimming ratio= 100%,（Ta=25±5℃, Turn on for 45minutes）

Note 2: MAX input current at all operating mode, measurement condition Rising time = 20ms (VDDB: 10%~90%)

Note 3: When BLU off (VDDB = 24V , VBLON = 0V) , IDDB (max) = 0.1A

Note 4: Less than 5% dimming control is functional well and no backlight shutdown happened

Note 5: D_EPWM and F_EPWM are available only at 2D mode

Note 6: Normal: 0~0.8V ; Abnormal : Open collector

3.7.2 Input Pin Assignment

■ LED DB connector: CI0114M1HR0-NH(CviLux) or equivalent
CI0112M1HR0-NH(CviLux) or equivalent

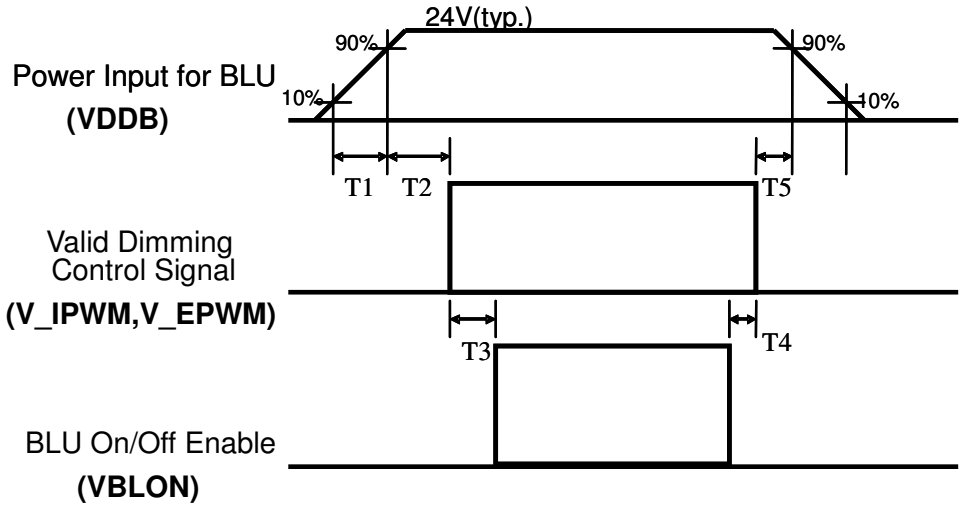
Pin	Symbol	Description
1	VDDB	Operating Voltage Supply, +24V DC regulated
2	VDDB	Operating Voltage Supply, +24V DC regulated
3	VDDB	Operating Voltage Supply, +24V DC regulated
4	VDDB	Operating Voltage Supply, +24V DC regulated
5	VDDB	Operating Voltage Supply, +24V DC regulated
6	BLGND	Ground and Current Return
7	BLGND	Ground and Current Return
8	BLGND	Ground and Current Return
9	BLGND	Ground and Current Return
10	BLGND	Ground and Current Return
11	DET	BLU status detection: Normal : 0~0.8V ; Abnormal : Open collector (Recommend Pull high R > 10K, VDD = 3.3V)
12	VBLON	BLU On-Off control: High/Open (2~5.5V) : BL On ; Low (0~0.8V/GND) : BL Off
13	NC	NC
14	PDIM(*)	External PWM (0%~100% Duty, open for 100%)

Pin	Symbol	Description
1	VDDB	Operating Voltage Supply, +24V DC regulated
2	VDDB	Operating Voltage Supply, +24V DC regulated
3	VDDB	Operating Voltage Supply, +24V DC regulated
4	VDDB	Operating Voltage Supply, +24V DC regulated
5	VDDB	Operating Voltage Supply, +24V DC regulated
6	BLGND	Ground and Current Return
7	BLGND	Ground and Current Return
8	BLGND	Ground and Current Return
9	BLGND	Ground and Current Return
10	BLGND	Ground and Current Return
11	NC	NC
12	NC	NC

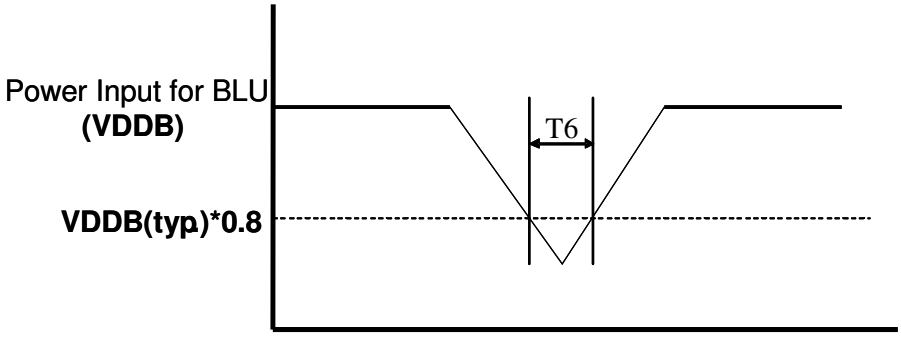
(Note*)
PWM Dimming range:

IF External PWM function less than 5% dimming ratio, Judge condition as below:
(1)Backlight module must be lighted ON normally.
(2)All protection function must work normally.
(3)Uniformity and flicker could not be guaranteed

3.7.3 Power Sequence for Backlight



Dip condition

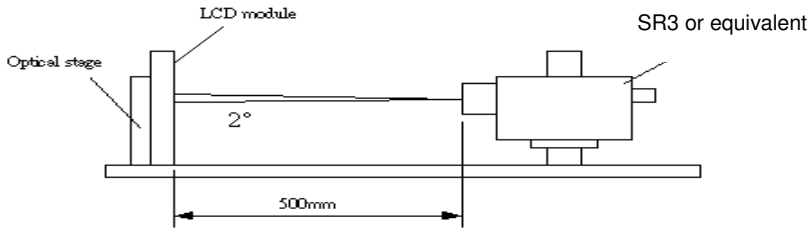


Parameter	Value			Units
	Min	Typ	Max	
T1	20	-	-	ms *1
T2	250	-	-	ms
T3	200			ms
T4	0	-	-	ms
T5	0	-	-	ms
T6		-	1000	ms *2

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 45 minutes in a dark environment at 25℃. The values specified are at an approximate distance 50cm from the LCD surface at a viewing angle of φ and θ equal to 0°.

Fig.1 presents additional information concerning the measurement equipment and method.



Parameter		Symbol	Values			Unit	Notes
			Min.	Typ.	Max		
Contrast Ratio		CR	3200	4000	--		1
Surface Luminance (White)		L_{WH} (2D)	360	450	--	cd/m^2	2
		L_{WH} (3D)		180			6
Luminance Variation		$\delta_{WHITE(9P)}$	--	--	1.3		3
Response Time (G to G)		Tγ	--	5.5	--	ms	4
Color Gamut		NTSC		72		%	
Color Coordinates							
	Red	R_X	Typ.-0.03	0.640	Typ.+0.03		
		R_Y		0.330			
	Green	G_X		0.300			
		G_Y		0.600			
	Blue	B_X		0.150			
		B_Y		0.050			
	White	W_X		0.280			
		W_Y		0.290			
Viewing Angle							5
2D	x axis, right(φ=0°)	θ_r	--	89	--	degree	
	x axis, left(φ=180°)	θ_l	--	89	--	degree	
	y axis, up(φ=90°)	θ_u	--	89	--	degree	
	y axis, down (φ=270°)	θ_d	--	89	--	degree	
3D	y axis, up + down	$\theta_u + \theta_d$	12	16		degree	6
3D cross talk (middle)			--	1	3	%	6

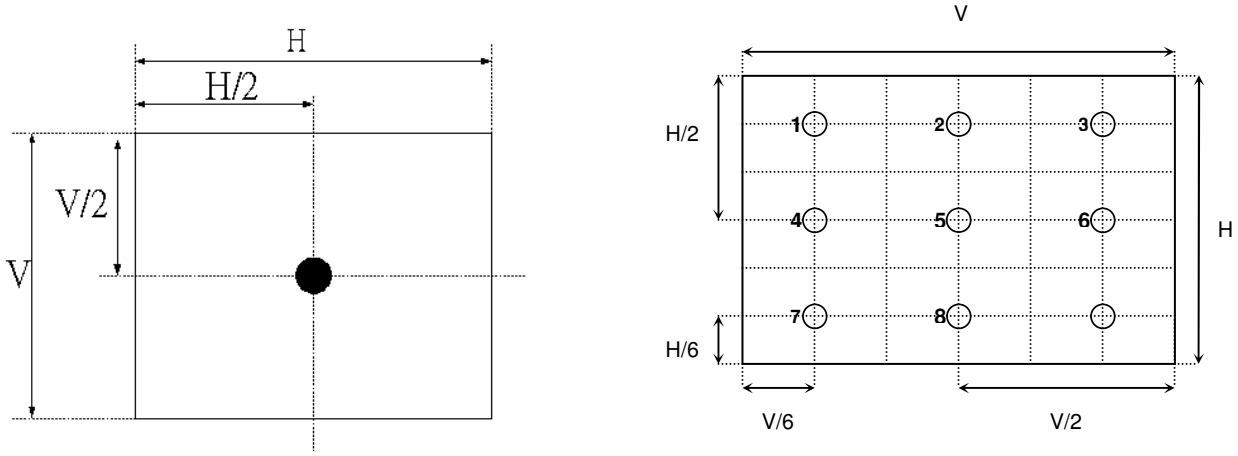
Note:

1. Contrast Ratio (CR) is defined mathematically as:

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance of } L_{on5}}{\text{Surface Luminance of } L_{off5}}$$

2. Surface luminance is luminance value at point 5 across the LCD surface 50cm from the surface with all pixels displaying white. From more information see FIG 2. When LED current I_F = typical value (without driver board), LED input VDDB =24V, I_{DDB}. = Typical value (with driver board), L_{WH}=Lon5 where Lon5 is the luminance with all pixels displaying white at center 5 location.

FIG. 2 Luminance



3. The variation in surface luminance, δWHITE is defined (center of Screen) as:

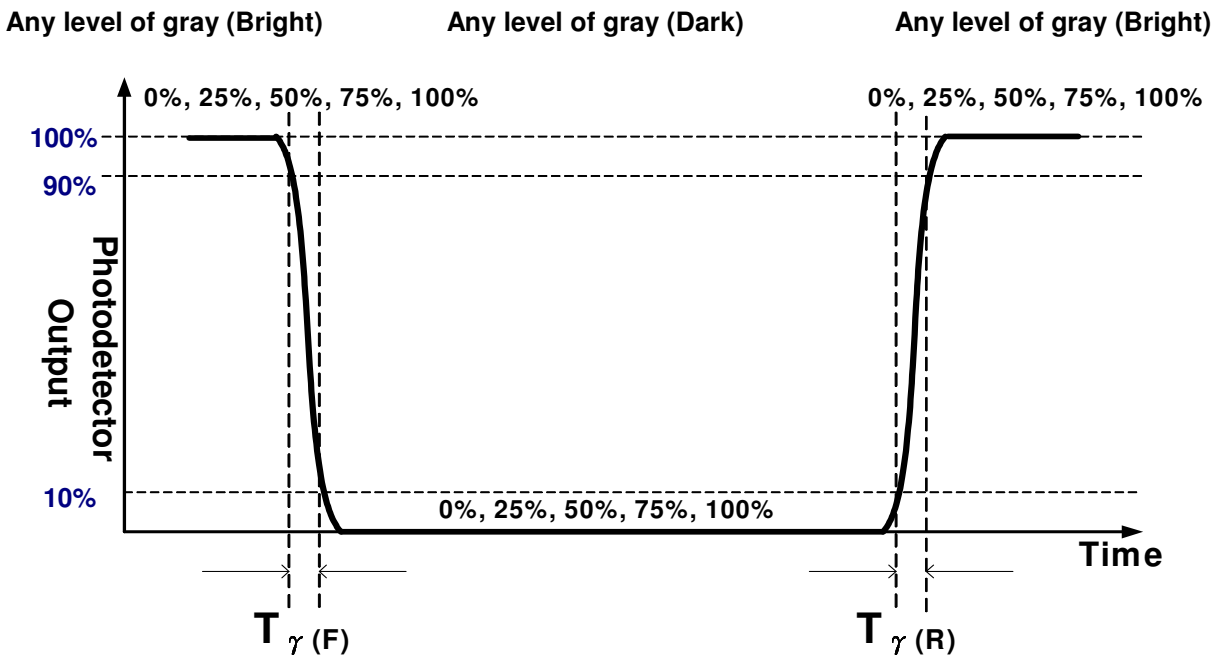
   $\delta_{WHITE(9P)}$= Maximum(L_{on1}, L_{on2},…,L_{on9})/ Minimum(L_{on1}, L_{on2},…L_{on9})

4. Response time T_γ is the average time required for display transition by switching the input signal for five luminance ratio (0%,25%,50%,75%,100% brightness matrix) and is based on F_v=120Hz to optimize.

Measured Response Time		Target				
		0%	25%	50%	75%	100%
Start	0%		0% to 25%	0% to 50%	0% to 75%	0% to 100%
	25%	25% to 0%		25% to 50%	25% to 75%	25% to 100%
	50%	50% to 0%	50% to 25%		50% to 75%	50% to 100%
	75%	75% to 0%	75% to 25%	75% to 50%		75% to 100%
	100%	100% to 0%	100% to 25%	100% to 50%	100% to 75%	

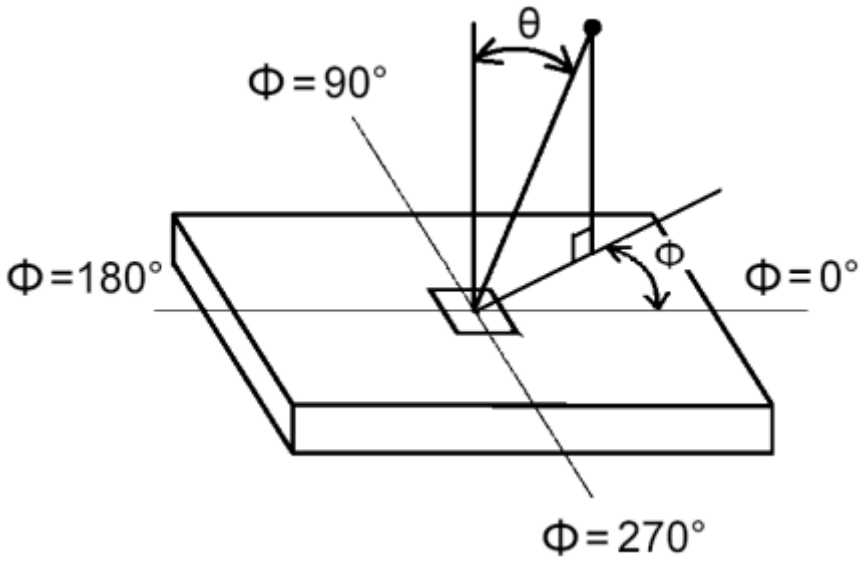
T_γ is determined by 10% to 90% brightness difference of rising or falling period. (As illustrated)

The response time is defined as the following figure and shall be measured by switching the input signal for "any level of gray(bright) " and "any level of gray(dark)".



5. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG3.

FIG.3 Viewing Angle

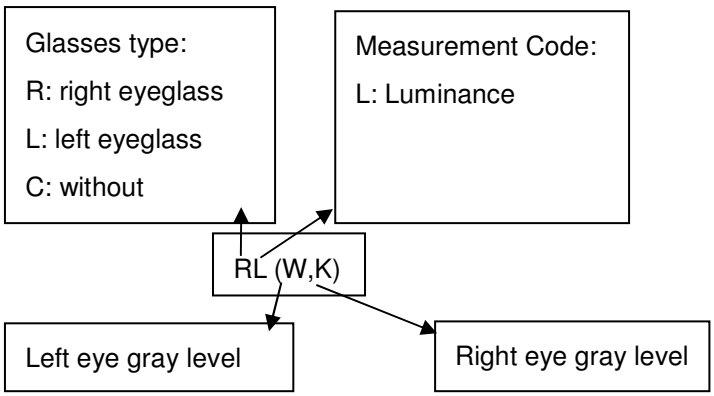


6. 3D performance specification is expressed by 3D luminance, 3D Crosstalk and 3D viewing angle. 3D luminance which is defined by **average of left and right eye brightness** under wearing glasses condition is measured at panel center point. Also, 3D crosstalk is measured at panel center point.
   a. Cross talk (middle) is defined by observation position which is 2.4m distance from panel center point and human head in 0 degree steady vertical angle from panel mid axis level.
   b. Cross talk (in vertical viewing angle) is defined by observation position which is 2.4m distance from panel

center point and observation range within specified degrees of vertical angle from panel mid axis level, and the value is limited by 10%.

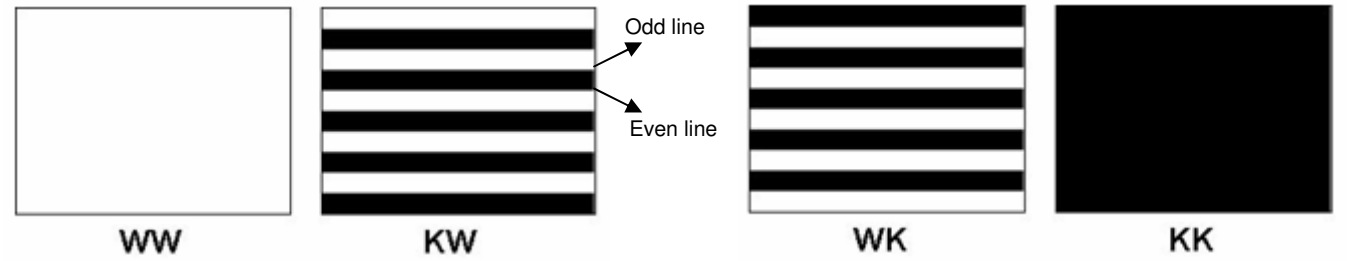
For more information, refer to 6-5 3D Measurement of 3D view angle.

6-1 Notation of measurement.



6-2 Measurement Configuration

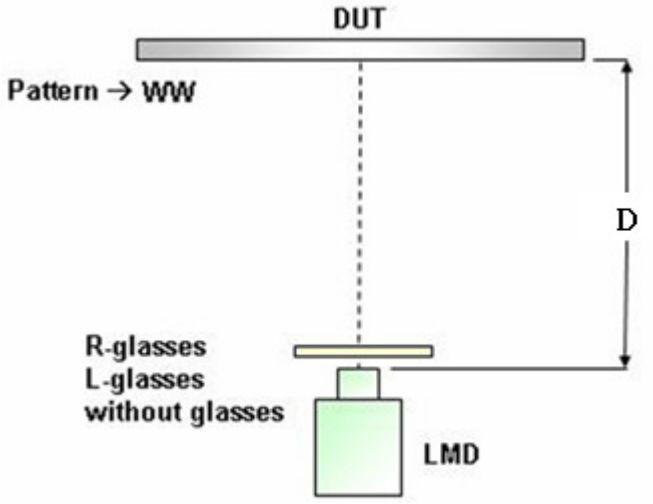
4-test patterns (first character refers to Left eye gray level; second one refers to Right eye gray level). W is defined as brightness gray level; K is defined as dark state where black and white lines are displayed on even or odd lines.



6-3 Measurement of 3D luminance

a. Test pattern WW is displayed, measuring distance is 50cm.

b. Left or right eyeglass are placed in front of SR3 or equivalent equipment (as FIG1 showed) successively and luminance is measured at panel center point where the notation for luminance measurement is RL(W,W) and LL(W,W).

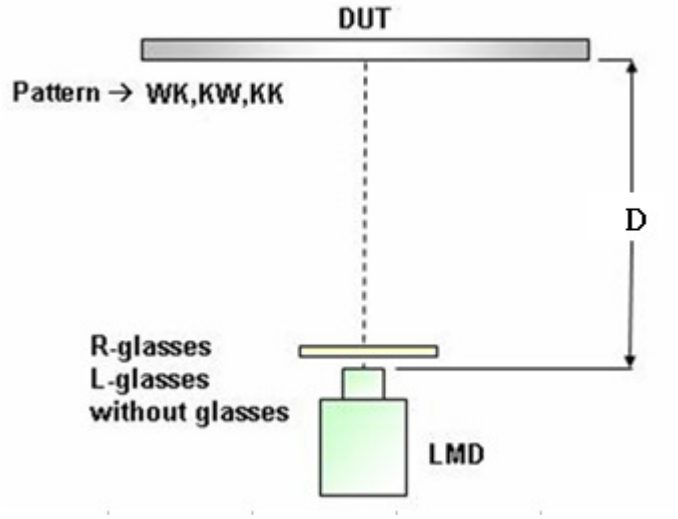


$$3D\ \ Lum = \frac{R_L(W,W) + L_L(W,W)}{2}$$

6-4 Measurement of 3D Crosstalk

a. Test patterns KW, WK and KK are displayed, measuring distance is 1.2m.

b. Right or left eyeglass is placed in front of SR3 or equivalent equipment (as FIG1 showed) successively and luminance is measured at panel center point



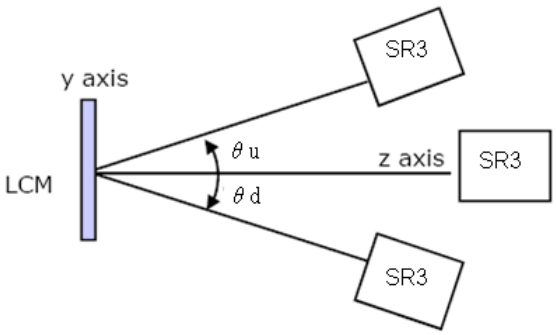
$$Crosstalk_R = \frac{R_L(W,K) - R_L(K,K)}{R_L(K,W) - R_L(K,K)} \times 100\%$$

$$Crosstalk_L = \frac{L_L(K,W) - L_L(K,K)}{L_L(W,K) - L_L(K,K)} \times 100\%$$

$$Crosstalk = \frac{Crosstalk_R + Crosstalk_L}{2}$$

6-5 Measurement of 3D view angle

The angles are determined for the vertical or y axis with respect to the z axis which is normal to the LCD module surface and measured at panel center position.

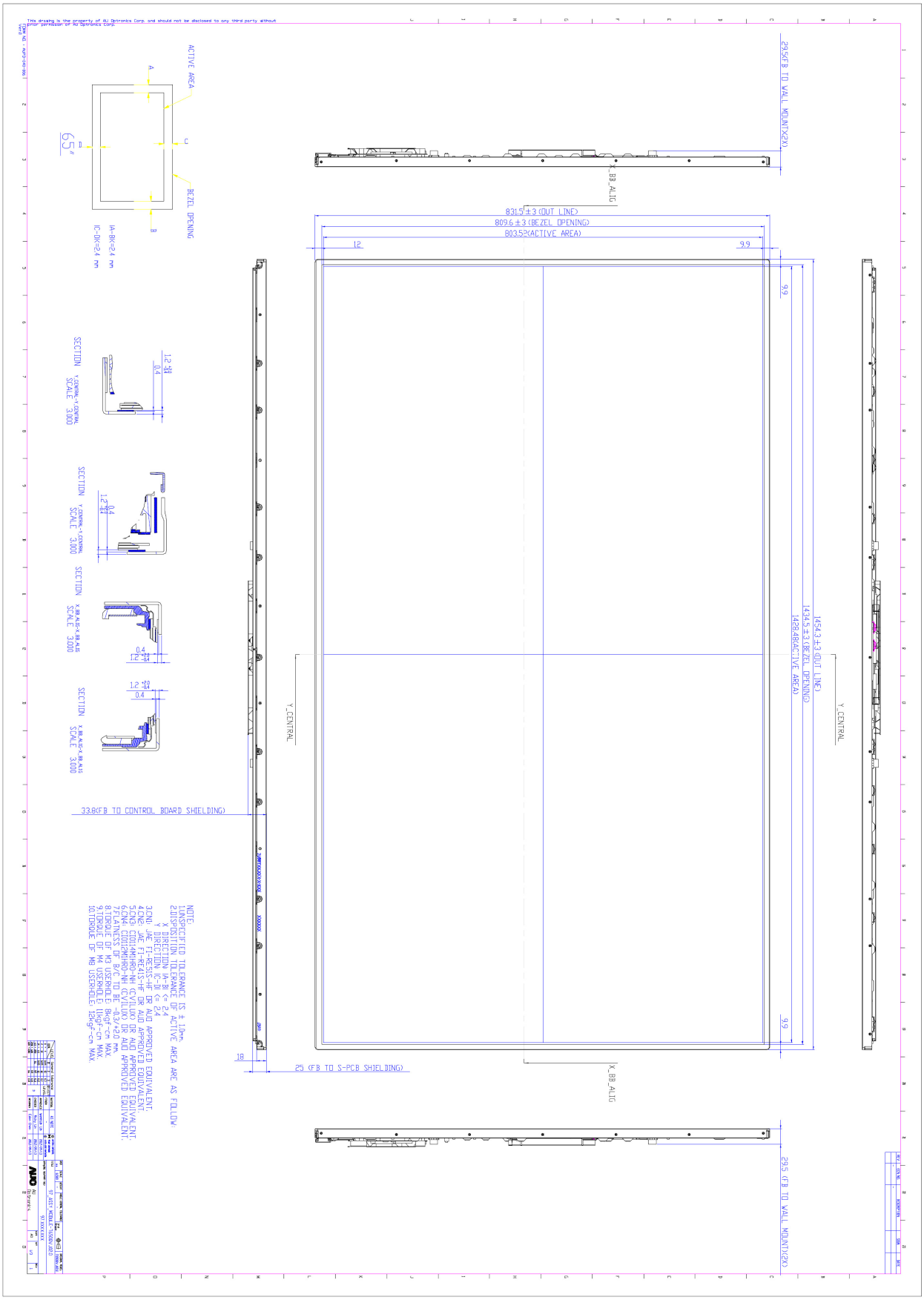


5. Mechanical Characteristics

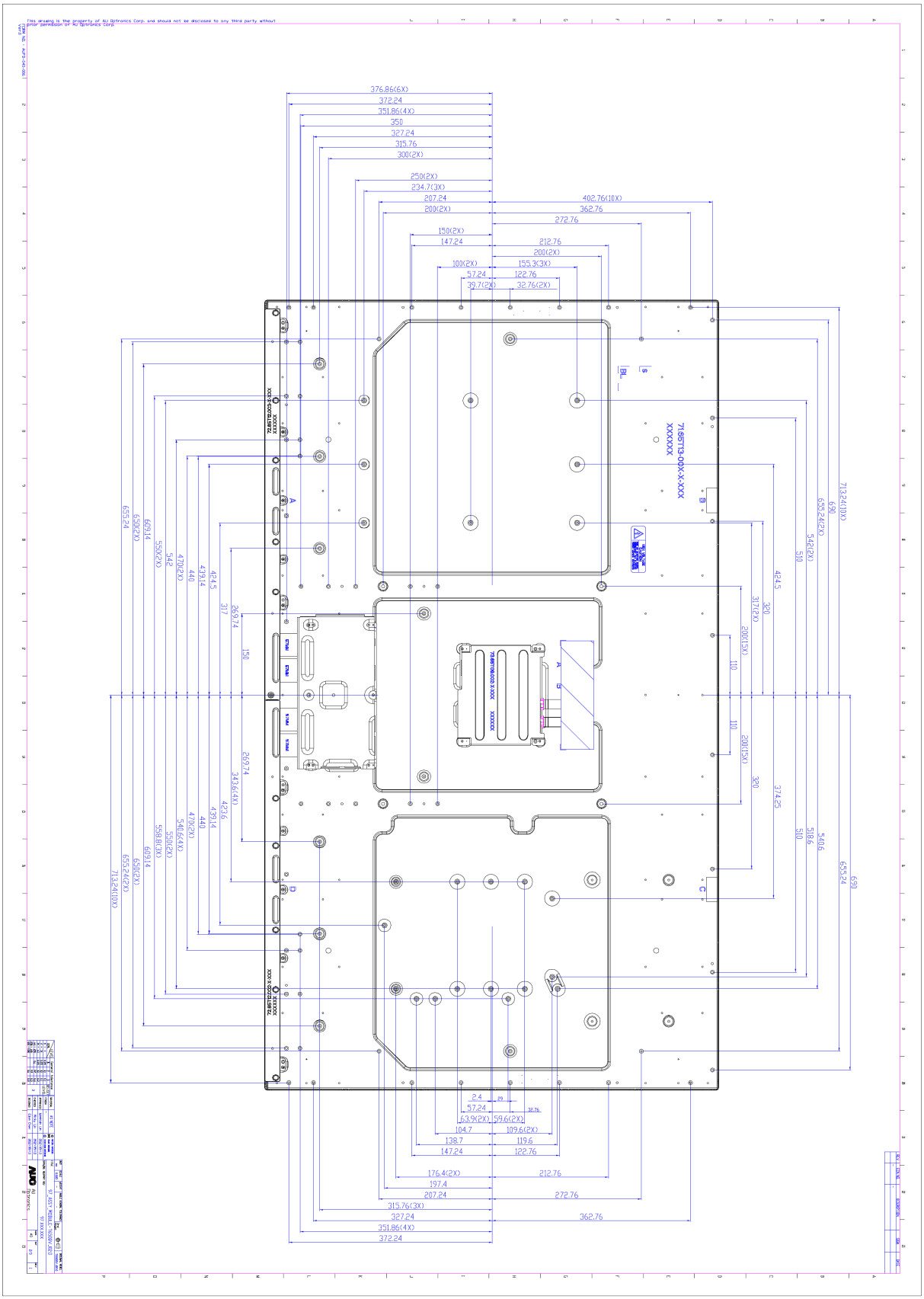
The contents provide general mechanical characteristics for the model T650QVD01.1. In addition the figures in the next page are detailed mechanical drawing of the LCD.

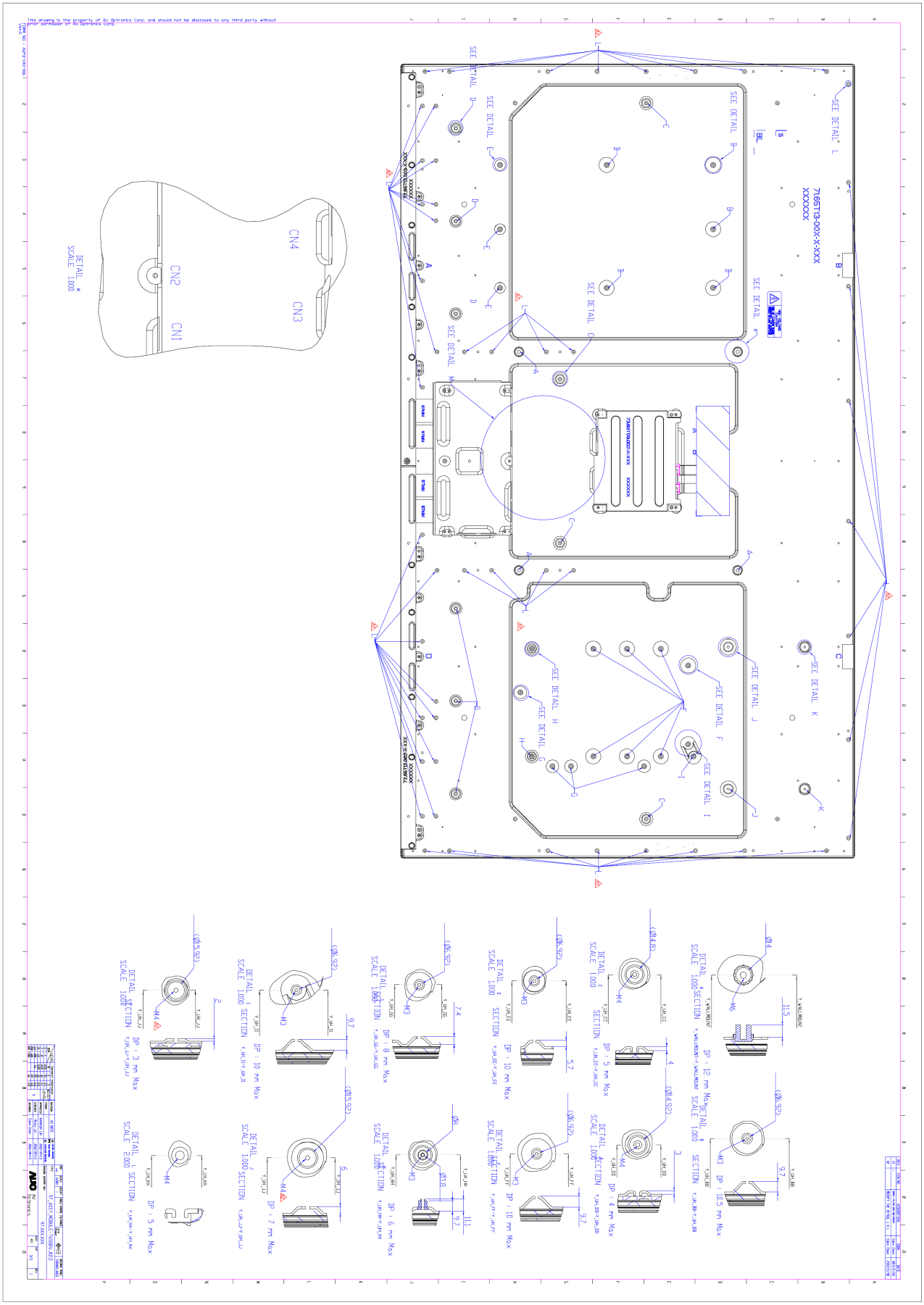
Item		Dimension	Unit	Note
Outline Dimension	Horizontal	1455.3	mm	
	Vertical	832.5	mm	
	Depth (Dmin)	18	mm	front bezel to back bezel
	Depth (Dmax)	29.3	mm	to T-con cover
Weight	27100		g	w/o DB

Front View



Back View





Reliability Test Items

	Test Item	Q'ty	Condition
1	Wet and High Temperature Storage test	3	60℃, Humidity 75% 300hrs
2	Low temperature storage test	3	-20℃, 300hrs
3	High temperature operation test	3	50℃, 300hrs
4	Low temperature operation test	3	-10℃, 300hrs
5	Vibration test (With carton)	5/carton	*Wave form, Random *Overall average energy level : 1.04Grms *Bandwidth & Level, 2~200Hz *Duration, X,Y,Z 20min per axes
6	Drop test (With carton)	5/carton	Height: 25.4 cm Direction: Only bottom flat twice (ASTMD4169-I)

7. International Standard

7.1 Safety

(1) UL 60950-1, UL 60065; Standard for Safety of Information Technology Equipment Including electrical Business Equipment.

(2) IEC 60950-1 : 2001, IEC 60065:2001 ; Standard for Safety of International Electrotechnical Commission

(3) EN 60950 : 2001+A11, EN 60065:2002+A1:2006; European Committee for Electrotechnical Standardization (CENELEC), EUROPEAN STANDARD for Safety of Information Technology Equipment Including Electrical Business Equipment.

7.2 EMC

(1) ANSI C63.4 “Methods of Measurement of Radio-Noise Emissions from Low-Voltage Electrical and Electrical Equipment in the Range of 9kHz to 40GHz. “American National standards Institute(ANSI), 1992

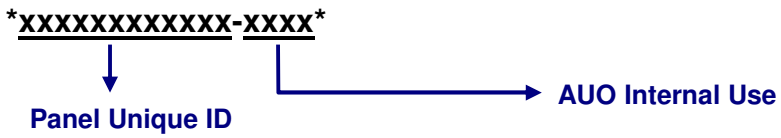
(2) C.I.S.P.R “Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment.” International Special committee on Radio Interference.

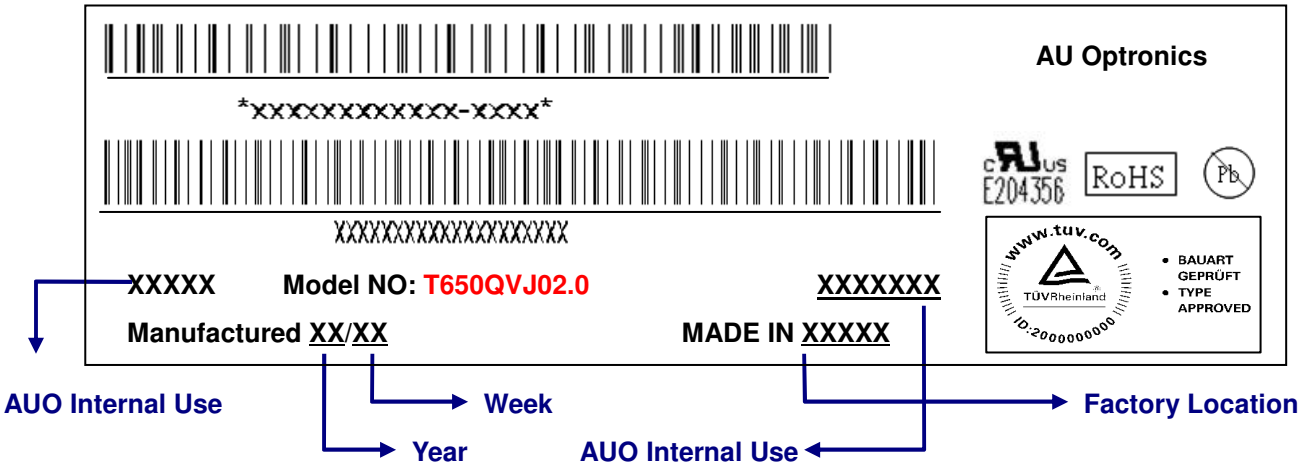
(3) EN 55022 “Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment.” European Committee for Electrotechnical Standardization. (CENELEC), 1998

8. Packing

8-1 DEFINITION OF LABEL:

A. Panel Label:





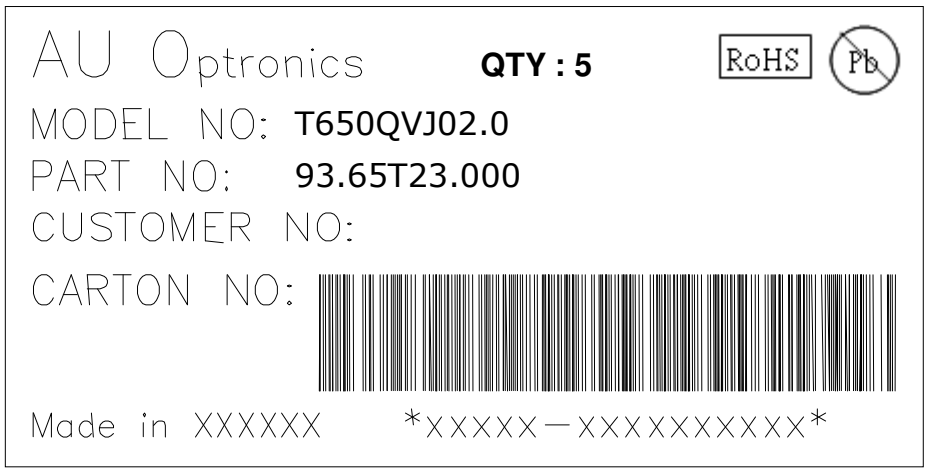
Green mark description

(1) For Pb Free Product, AUO will add Pb for identification.

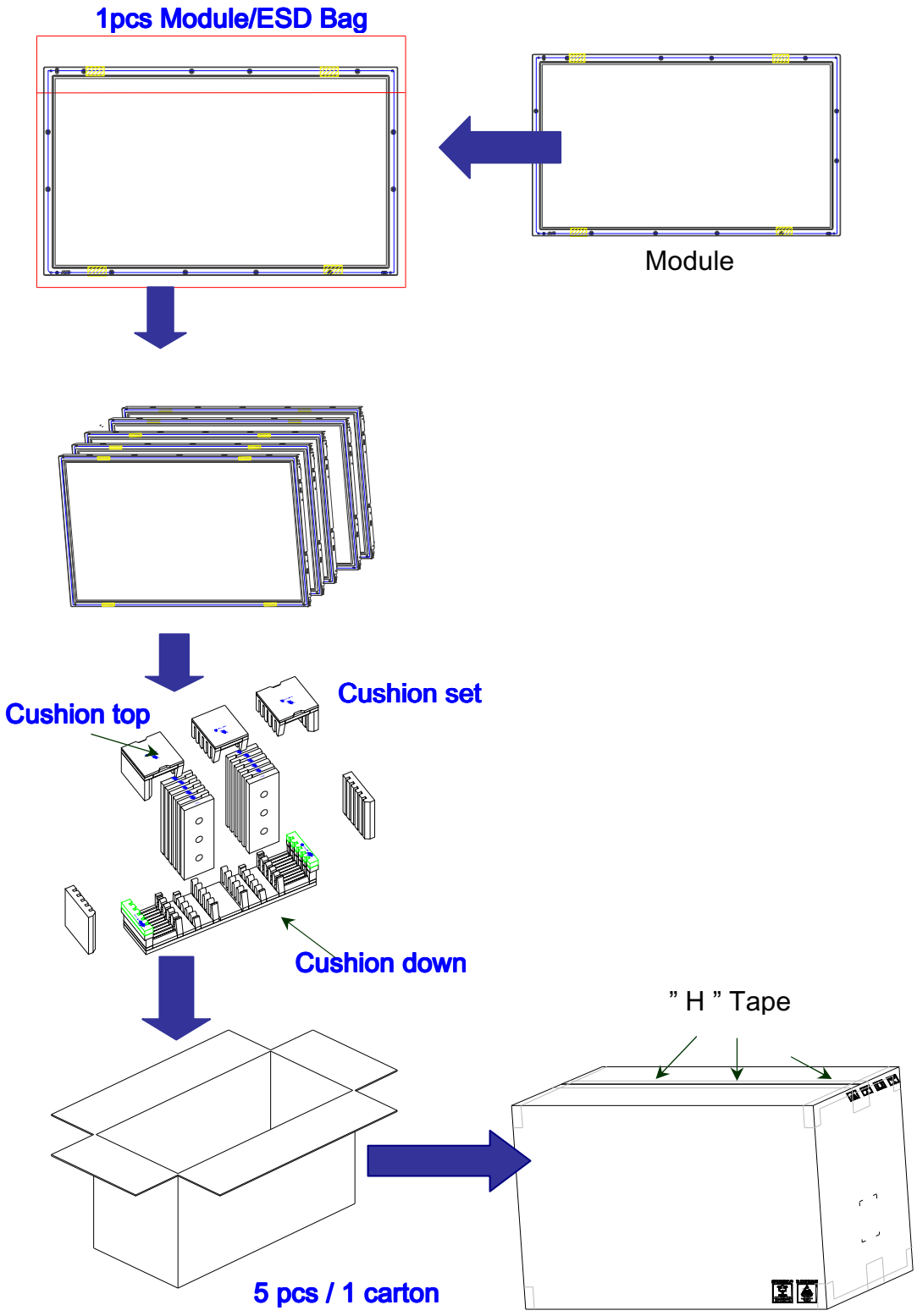
(2) For RoHs compatible products, AUO will add RoHS for identification.

Note: The green Mark will be present only when the green documents have been ready by AUO internal green team. (definition of green design follows the AUO green design checklist.)

B. Carton Label:

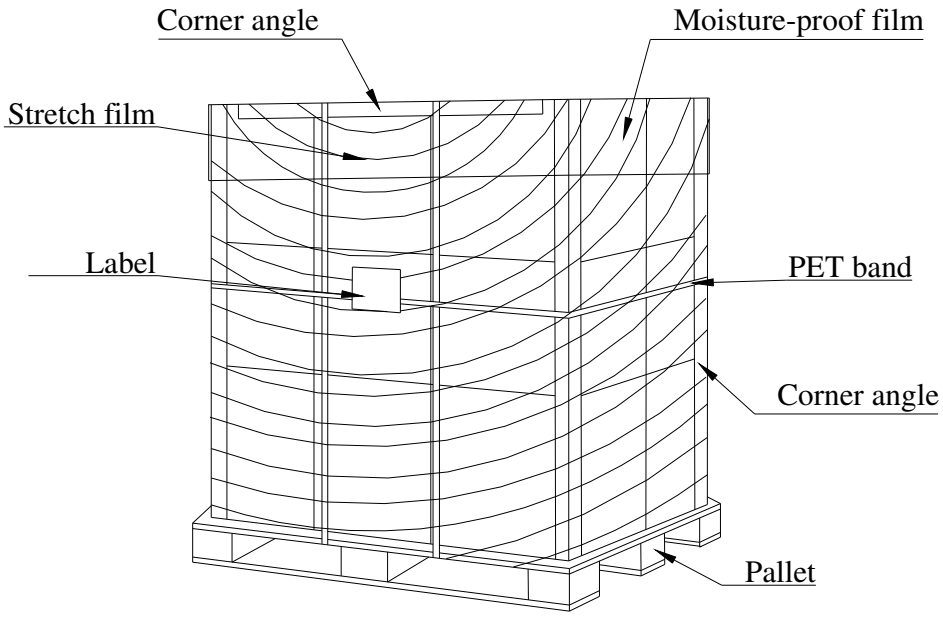


8-2 PACKING METHODS:



8-3 Pallet and Shipment Information

	Item	Specification			Packing Remark
		Qty.	Dimension	Weight (kg)	
1	Packing Box	5 pcs/box	1565(L)mm*380(W)mm*978(H)mm	165	
2	Pallet	1	1660(L)mm*1150(W)mm*144(H)mm	20	
3	Boxes per Pallet	5 boxes/Pallet (By Air) ; 3 Boxes/Pallet (By Sea)			
4	Panels per Pallet	25 pcs/pallet(By Air) ; 15 pcs/Pallet (By Sea)			
5	Pallet after packing	15 (by Air)	1660(L)mm*1150(W)mm*1122(H)mm	465(by Air)	
		30 (by Sea)	1660(L)mm*1150(W)mm*2244(H)mm	930(by Sea)	40ft HQ



9. PRECAUTIONS

Please pay attention to the followings when you use this TFT LCD module.

9-1 MOUNTING PRECAUTIONS

(1) You must mount a module using holes arranged in four corners or four sides.

(2) You should consider the mounting structure so that uneven force (ex. twisted stress) is not applied to module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.

(3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.

(4) You should adopt radiation structure to satisfy the temperature specification.

(5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter cause circuit broken by electro-chemical reaction.

(6) Do not touch, push or rub the exposed polarizer with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of polarizer for bare hand or greasy cloth. (Some cosmetics are detrimental to the polarizer.)

(7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front/ rear polarizer. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.

(8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.

(9) Do not open the case because inside circuits do not have sufficient strength.

9-2 OPERATING PRECAUTIONS

(1) The device listed in the product specification sheets was designed and manufactured for TV application

(2) The spike noise causes the mis-operation of circuits. It should be lower than following voltage: V=±200mV(Over and under shoot voltage)

(3) Response time depends on the temperature. (In lower temperature, it becomes longer..)

(4) Brightness of CCFL depends on the temperature. (In lower temperature, it becomes lower.) And in lower temperature, response time (required time that brightness is stable after turned on) becomes longer.

(5) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.

(6) When fixed patterns are displayed for a long time, remnant image is likely to occur.

(7) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interface.

9-3 ELECTROSTATIC DISCHARGE CONTROL

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wristband etc. And don't touch interface pin directly.

9-4 PRECAUTIONS FOR STRONG LIGHT EXPOSURE

Strong light exposure causes degradation of polarizer and color filter.

9-5 STORAGE

When storing modules as spares for a long time, the following precautions are necessary.

(1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5℃ and 35℃ at normal humidity.

(2) The polarizer surface should not come in contact with any other object. It is recommended that they be stored in the container in which they were shipped.

9-6 HANDLING PRECAUTIONS FOR PROTECTION FILM

(1) The protection film is attached to the bezel with a small masking tape. When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.

(2) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the bezel after the protection film is peeled off.

(3) You can remove the glue easily. When the glue remains on the bezel or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

