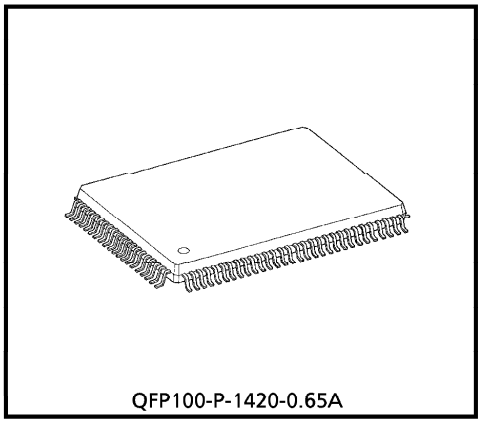
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

T6B36

ROW DRIVER FOR A DOT MATRIX LCD

The T6B36 is an 80-channel-output row driver for an STN dot matrix LCD. The T6B36 features an −38V-LCD drive voltage. The T6B36 is able to drive LCD panels with a duty ratio of up to 1/480. It is recommended for use with the T6A39.



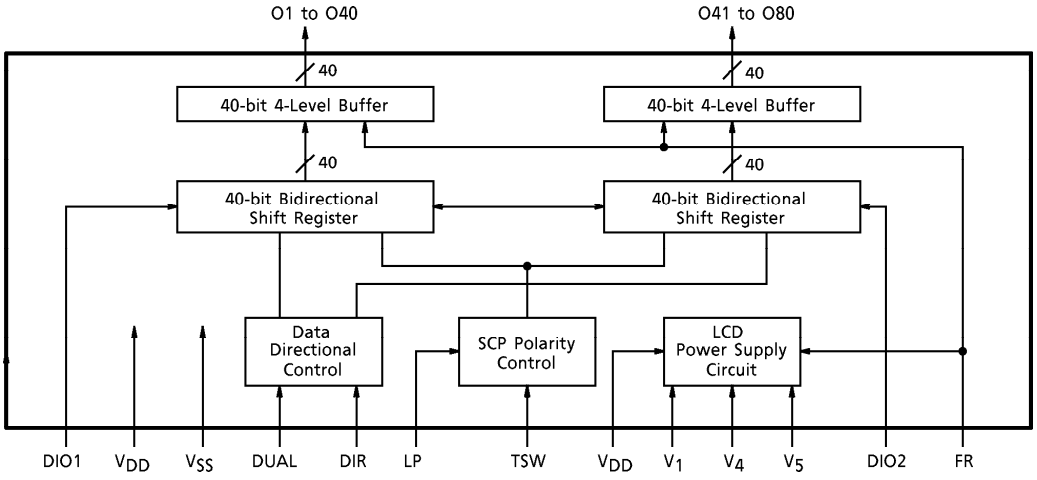
QFP100-P-1420-0.65A

Weight : 1.6g (typ.)

FEATURES

- Display duty application : to 1/480
- LCD drive signal : 80
- Data transfer : 1-bit bidirectional
  ① O80←O1
  ② O80→O1
  ③ O1→O40, O41←O80
- LCD drive voltage : −10 to −38V (max −40V)
- Operating voltage : 4.5 to 5.5V
- Operating temperature : −20 to 75°C
- LCD drive output resistance : 2.2kΩ (max) (20V, 1/13 bias)
- Display-off function : When /DSPOF is L, all LCD drive outputs (O1 to O80) remain at the V_{DD} level.
- LCD drive output timing : Change on falling edge or rising edge of LP (selected by TSW)

BLOCK DIAGRAM



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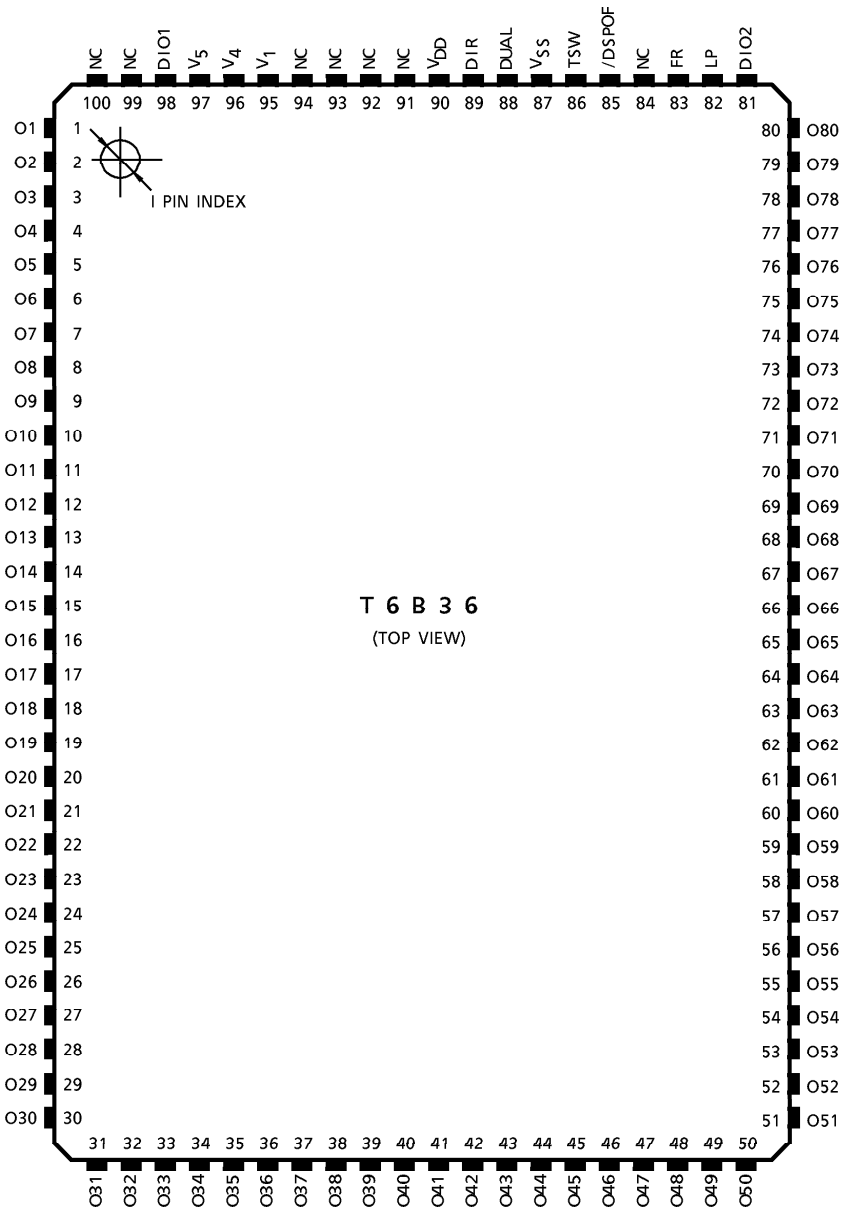
PIN ASSIGNMENT



PIN FUNCTIONS

PIN NAME	I/O	FUNCTIONS	LEVEL
O1 to O80	Output	Output for LCD drive signal	V_{DD} to V_5
DIO1, DIO2	I/O	Input/output for shift data U_{SE} to FP signal	V_{DD} to V_{SS}
LP	Input	(Shift Clock Pulse) Input for shift clock pulse	
FR	Input	(Frame) Input for frame signal	
DUAL	Input	(Dual Mode) Terminal for dual input mode or single input mode select	
DIR	Input	(Direction) Input for data flow direction select	
TSW	Input	(Terminal Switch) When fied to V_{SS} : (O1 to O80) output on the rising edge of LP When fied to V_{DD} : (O1 to O80) output on the falling edge of LP	
/DSPOF	Input	(Display Off) /DSPOF = L : Display-off mode, (O1 to O80) remain at the V_{DD} level. /DSPOF = H : Display-on mode, (O1 to O80) are operational.	
V_{DD}	—	Power supply for internal logic (5V)	—
V_{SS}	—	Power supply for internal logic (0V)	
V_1	—	Power supply for LCD drive circuit	
V_4	—	Power supply for LCD drive circuit	
V_5	—	Power supply for LCD drive circuit	

RELATION BETWEEN FR, DATA INPUT AND OUTPUT LEVEL

FR	DATA INPUT (DIO1, DIO2)	/DSPOF	OUTPUT LEVEL
L	L	H	V_1
L	H	H	V_5
H	L	H	V_4
H	H	H	V_{DD}
*	*	L	V_{DD}

* Don't Care

DATA INPUT FORMAT

DUAL	DIR	DATA FLOW	DATA INPUT	
			DIO1	DIO2
H	H	O1→O40 O80→O41	IN	IN
L	H	O1→O80	IN	OUT
H	L	O80→O1	OUT	IN
L	L			

TIMING DIAGRAM

DIR = H, DUAL = L, TSW = H

ABSOLUTE MAXIMUM RATINGS

(Ensure that the following conditions are maintained, $V_{DD} \geqq V_1 \geqq V_4 \geqq V_5$, $V_{SS} = 0V$)

ITEM	SYMBOL	PIN NAME	RATING	UNIT
Supply Voltage 1	V_{DD}	V_{DD}	− 0.3 to 7.0	V
Supply Voltage 2	V_1 V_4 V_5	V_1 V_4 V_5	V_{DD} − 40.0 to V_{DD} + 0.3	V
Input Voltage	V_{in}	(*1)	− 0.3 to V_{DD} + 0.3	V
Operating Temperature	T_{opr}	—	− 20 to 75	°C
Storage Temperature	T_{stg}	—	− 55 to 125	°C

(*1) SCP, FR, /DSPOF, TSW, DUAL, DIR, DIO1, DIO2

ELECTRICAL CHARACTERISTICS

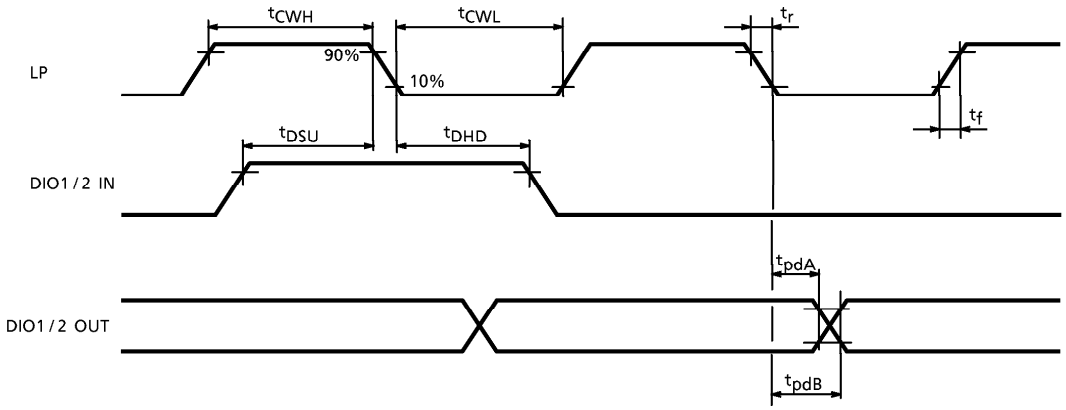
DC CHARACTERISTICS

TEST CONDITIONS (Unless otherwise noted, $V_{SS} = 0V$, $V_{DD} = 4.5$ to $5.5V$, $V_5 = (V_{DD} - 38)$ to $(V_{DD} - 10)$ V, Ta = − 20 to 75°C)

ITEM		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT	PIN NAME
Supply Voltage 1		—	—	—	4.5	5.0	5.5	V	V_{DD}
Supply Voltage 2		—	—	—	V_{DD} − 38	—	V_{DD} − 10	V	V_5
Input Voltage	H Level	V_{IH}	—	—	V_{DD} − 0.8	—	V_{DD}	V	LP, FR, /DSPOF, TSW, DUAL, DIR, DIO1, DIO2
	L Level	V_{IL}		—	0	—	0.8		
Output Voltage	H Level	V_{OH}	—	I_{OH} = − 0.5mA	V_{DD} − 0.5	—	V_{DD}	V	DIO1, DIO2
	L Level	V_{OL}		I_{OL} = 0.5mA	0	—	0.5		
Output Resistance	H Level	R_{OH}	—	$V_{OUT} = V_{DD} - 0.5V$ (*2)	—	—	2.2	kΩ	O1 to O80
	M Level	R_{OM}		$V_{OUT} = V_1 \pm 0.5V$ (*2)	—	—	2.2		
		R_{OM}		$V_{OUT} = V_4 \pm 0.5V$ (*2)	—	—	2.2		
	L Level	R_{OL}		$V_{OUT} = V_5 + 0.5V$ (*2)	—	—	2.2		
Current Consumption		I_{SS}	—	f_{FR} = 35.5Hz, f_{SCP} = 7.1kHz (Duty : 1 / 704) O1 to O80 No load; Input data f_{DIO} = 71Hz (Duty : 1 / 100) Input voltage "H" = V_{DD} "L" = V_{SS}	—	2.0	10.0	μA	V_{SS}

(*2) $V_{DD} = 5.0V$, $V_5 = -15.0V$, $V_1 = V_{DD}\text{-}1 / 13 (V_{DD}\text{-}V_5)$, $V_4 = V_{DD}\text{-}12 / 13 (V_{DD}\text{-}V_5)$

AC CHARACTERISTICS



TEST CONDITIONS (V_{SS} = 0V, V_{DD} = 4.5 to 5.5V, V_5 = (V_{DD}-38) to (V_{DD}-10) V, Ta = – 20 to 75°C)

ITEM	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
SCP Pulse Width H	t_{CWH}	LP	30	—	ns
SCP Pulse Width L	t_{CWL}	LP	1	—	μs
Input Rise / Fall Time	t_r, t_f	LP, FR, DIO1, DIO2	—	(*4)	ns
Data Set-up Time	t_{DSU}	DIO1, DIO2	30	—	ns
Data Hold Time	t_{DHD}	DIO1, DIO2	50	—	ns
Output Data Delay Time A (*3)	tpdA	DIO1, DIO2	80	—	ns
Output Data Delay Time B (*3)	tpdB	DIO1, DIO2	—	1	μs

(*3) C_L = 10pF

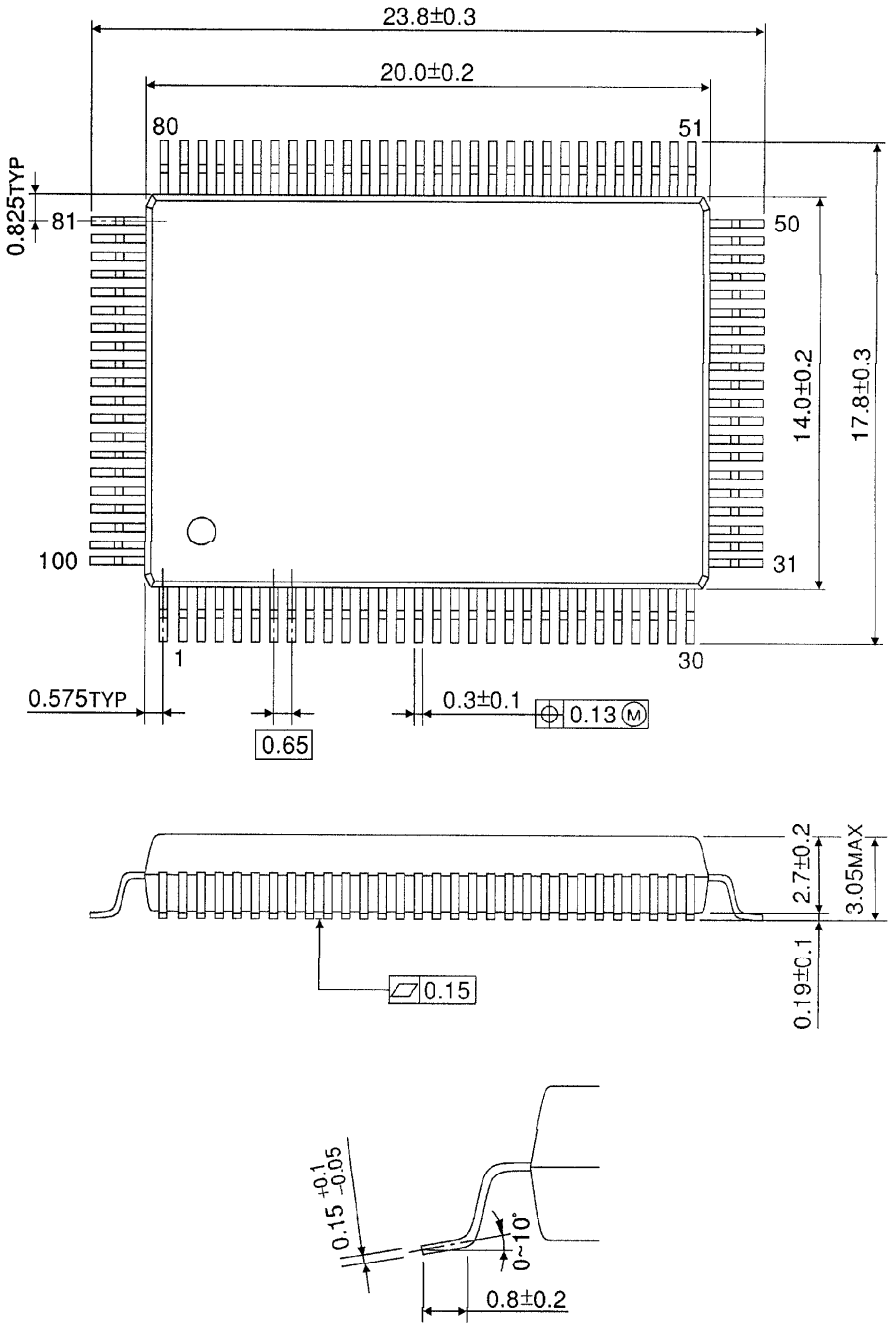
(*4) t_r, $t_f \leqq (t_C - t_{CWH} - t_{CWL}) / 2$ or t_r, $t_f \leqq$ 50ns

NOTE

Insert the bypass capacitor (0.1μF) between V_{DD} and V_{SS} to decrease power supply noise. Place the bypass capacitor as close to the LSI as possible.

OUTLINE DRAWING

QFP100-P-1420-0.65A Unit : mm



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