



Features

- Single 3-V Supply Voltage
- High Power-added Efficient Power Amplifier (P_{out} Typically 23 dBm)
- Ramp-controlled Output Power
- Low-noise Preamplifier (NF Typically 2.1 dB)
- Biasing for External PIN Diode T/R Switch
- Current-saving Standby Mode
- Few External Components
- Packages:
 - PSSO20
 - QFN20 with Extended Performance

Electrostatic sensitive device.
Observe precautions for handling.



Bluetooth™/ISM 2.4-GHz Front- End IC

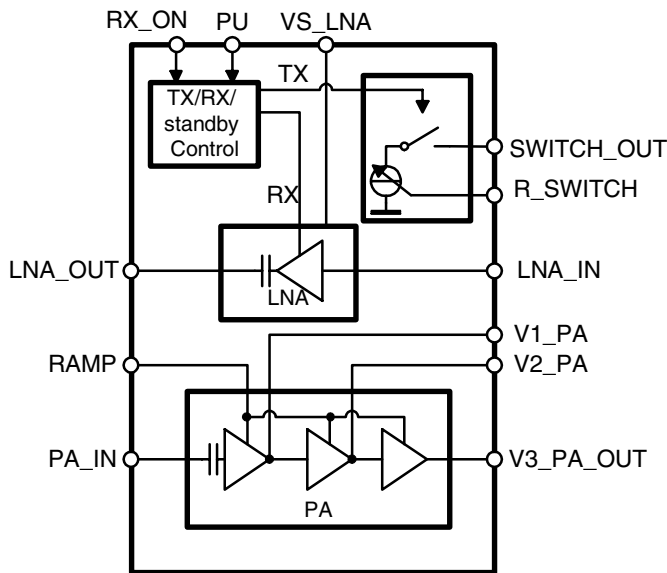
T7024

Description

The T7024 is a monolithic SiGe transmit/receive front-end IC with power amplifier, low-noise amplifier and T/R switch driver. It is especially designed for operation in TDMA systems like Bluetooth™ and WDC T.

Due to the ramp-control feature and a very low quiescent current, an external switch transistor for V_S is not required.

Figure 1. Block Diagram



Pin Configuration

Figure 2. Pinning PSSO20

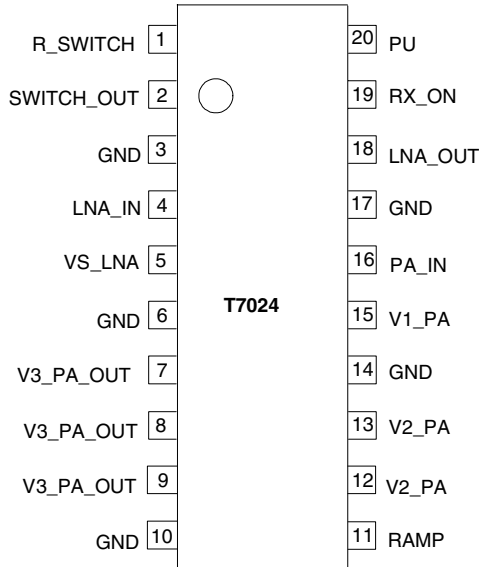
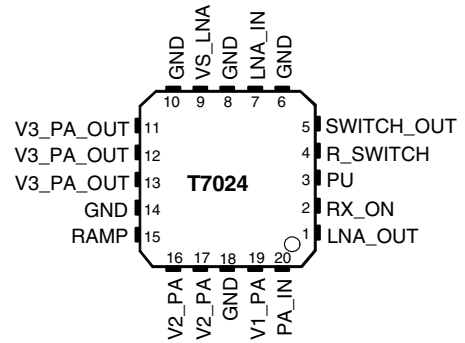


Figure 3. Pinning QFN20



Pin Description

| Pins PSSO20 | Pins QFN20 | Symbol | Function |
|-------------|------------|------------|--|
| 1 | 4 | R_SWITCH | Resistor to GND sets the PIN diode current |
| 2 | 5 | SWITCH_OUT | Switched current output for PIN diode |
| 3 | 6 | GND | Ground |
| 4 | 7 | LNA_IN | Low-noise amplifier input |
| 5 | 9 | VS_LNA | Supply voltage input for low-noise amplifier |
| 6 | 8 | GND | Ground |
| 7 | 11 | V3_PA_OUT | Inductor to power supply and matching network for power amplifier output |
| 8 | 12 | V3_PA_OUT | Inductor to power supply and matching network for power amplifier output |
| 9 | 13 | V3_PA_OUT | Inductor to power supply and matching network for power amplifier output |
| 10 | 10 | GND | Ground |
| 11 | 15 | RAMP | Power ramping control input |
| 12 | 16 | V2_PA | Inductor to power supply for power amplifier |
| 13 | 17 | V2_PA | Inductor to power supply for power amplifier |
| 14 | 14 | GND | Ground |
| 15 | 19 | V1_PA | Supply voltage for power amplifier |
| 16 | 20 | PA_IN | Power amplifier input |
| 17 | 18 | GND | Ground |
| 18 | 1 | LNA_OUT | Low-noise amplifier output |
| 19 | 2 | RX_ON | RX active high |
| 20 | 3 | PU | Power-up active high |
| Slug | Slug | GND | Ground |

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| Parameters | Symbol | Value | Unit |
|--|-------------|-------------|------|
| Supply voltage Pins VS_LNA, V1_PA, V2_PA, V3_PA_OUT | V_S | 6 | V |
| Junction temperature | T_j | 150 | °C |
| Storage temperature | T_{stg} | -40 to +125 | °C |
| RF input power LNA | P_{inLNA} | 5 | dBm |
| RF input power PA | P_{inPA} | 10 | dBm |

Thermal Resistance

| Parameters | Symbol | Value | Unit |
|--|------------|-------|------|
| Junction ambient PSSOP20, slug soldered on PCB | R_{thJA} | 19 | K/W |
| Junction ambient QFN20, slug soldered on PCB | R_{thJA} | 27 | K/W |

Handling

Do not operate this part near strong electrostatic fields. This IC meets class 1 ESD test requirement (HBM in accordance to EIA/JESD22-A114-A (October 97) and class A ESD test requirement (MM) in accordance to EIA/JESD22-A115A.

Operating Range

All voltages are referred to ground (pins GND and slug). Power supply points are VS_LNA, V1_PA, V2_PA, V3_PA_OUT. The table represents the sum of all supply currents depending on the TX/RX mode.

| Parameters | Symbol | Min. | Typ. | Max. | Unit |
|---|------------------|------|------|------|------|
| Supply voltage Pins V1_PA, V2_PA and V3_PA_OUT | V_S | 2.7 | 3.0 | 4.6 | V |
| Supply voltage Pin VS_LNA | V_S | 2.7 | 3.0 | 5.5 | V |
| Supply current TX PSSO20 | I_S | | 190 | | mA |
| Supply current TX QFN20 | I_S | | 165 | | mA |
| Supply current RX | I_S | | 8 | | mA |
| Standby current PU = 0 | $I_{S_standby}$ | | 10 | | μA |
| Ambient temperature | T_{amb} | -25 | +25 | +85 | °C |

Electrical Characteristics

Test conditions (unless otherwise specified): $V_S = 3.0\text{ V}$, $T_{amb} = 25^\circ\text{C}$

| Parameters | Test Conditions | Symbol | Min. | Typ. | Max. | Unit |
|--|---|---------------------|------|--------|------|---------------|
| Power Amplifier⁽¹⁾ | | | | | | |
| Supply voltage | Pins V1_PA, V2_PA, V3_PA_OUT | V_S | 2.7 | 3.0 | 4.6 | V |
| Supply current | TX PSSO20 | I_{S_TX} | | 190 | | mA |
| | TX QFN20 | I_{S_TX} | | 165 | | mA |
| | RX (PA off), $V_{RAMP} \leq 0.1\text{ V}$ | I_{S_RX} | | | 10 | μA |
| Standby current | Standby | $I_{S_standby}$ | | | 10 | μA |
| Frequency range | TX | f | 2.4 | | 2.5 | GHz |
| Gain-control range | TX | ΔGp | 60 | 42 | | dB |
| Power gain maximum | TX, Pin PA_IN to V3_PA_OUT | Gp | 28 | 30 | 33 | dB |
| Power gain minimum | TX, Pin PA_IN to V3_PA_OUT | Gp | -40 | | -17 | dB |
| Ramping voltage maximum | TX, power gain (maximum) Pin RAMP | $V_{RAMP\ max}$ | 1.7 | 1.75 | 1.83 | V |
| Ramping voltage minimum | TX, power gain (minimum) Pin RAMP | $V_{RAMP\ min}$ | | 0.1 | | V |
| Ramping current maximum | TX, $V_{RAMP} = 1.75\text{ V}$, Pin RAMP | $I_{RAMP\ max}$ | | | 0.5 | mA |
| Power-added efficiency | TX PSSO20 | PAE | 30 | 35 | | % |
| | TX QFN20 | PAE | 35 | 40 | | % |
| Saturated output power | TX, input power = 0 dBm referred to Pins V3_PA_OUT | P_{sat} | 22 | 23 | 24 | dBm |
| Input matching ⁽²⁾ | TX, Pin PA_IN | Load VSWR | | <1.5:1 | | |
| Output matching ⁽²⁾ | TX, Pins V3_PA_OUT | Load VSWR | | <1.5:1 | | |
| Harmonics at $P_{sat} = 23\text{ dBm}$ | TX, Pins V3_PA_OUT | 2 fo | | | -30 | dBc |
| | TX, Pins V3_PA_OUT | 3 fo | | | -30 | dBc |
| T/R Switch Driver (Current Programming by External Resistor from R_SWITCH to GND) | | | | | | |
| Switch-out current output | Standby, Pin SWITCH_OUT | $I_{S_O_standby}$ | | | 1 | μA |
| | RX | $I_{S_O_RX}$ | | | 1 | μA |
| | TX at 100 Ω | $I_{S_O_100}$ | | 1.7 | | mA |
| | TX at 1.2 k Ω | $I_{S_O_1k2}$ | | 7 | | mA |
| | TX at 33 k Ω | $I_{S_O_33k}$ | | 17 | | mA |
| | TX at ∞ | $I_{S_O_R}$ | | 19 | | mA |
| Low-noise Amplifier⁽³⁾ | | | | | | |
| Supply voltage | All, Pin VS_LNA | V_S | 2.7 | 3.0 | 5.5 | V |
| Supply current | RX | I_S | | 8 | 9 | mA |

- Notes:
- Power amplifier shall be unconditionally stable, maximum duty cycle 100%, true CW operation, maximum load mismatch and duration: load VSWR = 10:1 (all phases) 10 s, $Z_G = 50\ \Omega$
 - With external matching network, load impedance 50 Ω
 - Low-noise amplifier shall be unconditionally stable.
 - With external matching components.
 - LNA gain can be adjusted with RX_ON voltage according to Figure 19 on page 11. Please note, that for RX_ON below 1.4 V the T/R switch driver switches to TX mode.

Electrical Characteristics (Continued)

Test conditions (unless otherwise specified): $V_S = 3.0\text{ V}$, $T_{\text{amb}} = 25^\circ\text{C}$

| Parameters | Test Conditions | Symbol | Min. | Typ. | Max. | Unit |
|---|---|------------------|------|------|--------------|---------------|
| Supply current (LNA and control logic) | TX (control logic active) Pin VS_LNA | I_S | | | 0.5 | mA |
| Standby current | Standby, Pin VS_LNA | $I_{S_standby}$ | | 1 | 10 | μA |
| Frequency range | RX | f | 2.4 | | 2.5 | GHz |
| Power gain ⁽⁵⁾ | RX, Pin LNA_IN to LNA_OUT | Gp | 15 | 16 | 19 | dB |
| Noise figure | RX, PSSO20 | NF | | 2.5 | 2.8 | dB |
| | RX, QFN20 | NF | | 2.1 | 2.3 | dB |
| Gain compression | RX, referred to Pin LNA_OUT | O1dB | -9 | -7 | -6 | dBm |
| 3 rd -order input interception point | RX | IIP3 | -16 | -14 | -13 | dBm |
| Input matching ⁽⁴⁾ | RX, Pin LNA_IN | VSWRin | | | 2:1 | |
| Output matching ⁽⁴⁾ | RX Pin LNA_OUT | VSWRout | | | 2:1 | |
| Logic Input Levels (RX_ON, PU)⁽⁵⁾ | | | | | | |
| High input level | = '1' Pins RX_ON and PU | V_{iH} | 2.4 | | V_{S_LNA} | V |
| Low input level | = '0' | V_{iL} | 0 | | 0.5 | V |
| High input current | = '1' $V_{iH} = 2.4\text{ V}$ | I_{iH} | | 40 | 60 | μA |
| Low input current | = '0' | I_{iL} | | | 0.2 | μA |

- Notes:
- Power amplifier shall be unconditionally stable, maximum duty cycle 100%, true CW operation, maximum load mismatch and duration: load VSWR = 10:1 (all phases) 10 s, $Z_G = 50\ \Omega$
 - With external matching network, load impedance $50\ \Omega$
 - Low-noise amplifier shall be unconditionally stable.
 - With external matching components.
 - LNA gain can be adjusted with RX_ON voltage according to Figure 19 on page 11. Please note, that for RX_ON below 1.4 V the T/R switch driver switches to TX mode.

Control Logic for LNA and T/R Switch Driver

| Operation Mode | PU | RX_ON |
|----------------|----|-------|
| Standby | 0 | 0 |
| TX | 1 | 0 |
| RX | 1 | 1 |

Typical Operating Characteristics

Figure 4. LNA (PSSO20): Gain and Noise Figure versus Frequency

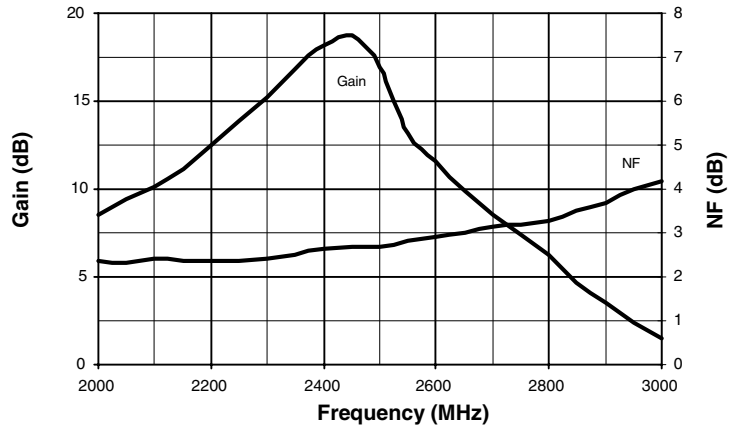


Figure 5. LNA (N20): Gain and Noise Figure versus Frequency

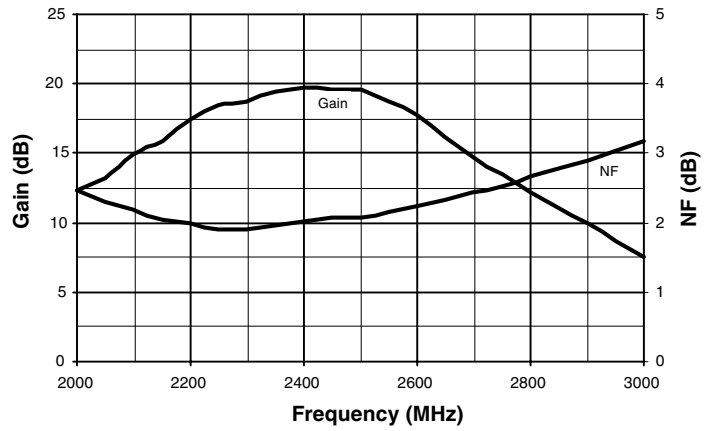


Figure 6. LNA: NF and Gain versus Temperature

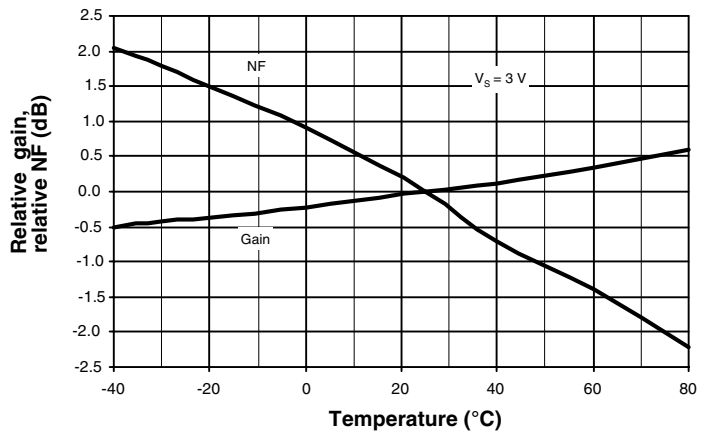


Figure 7. LNA: Typical Switch-out Current versus R_{switch}

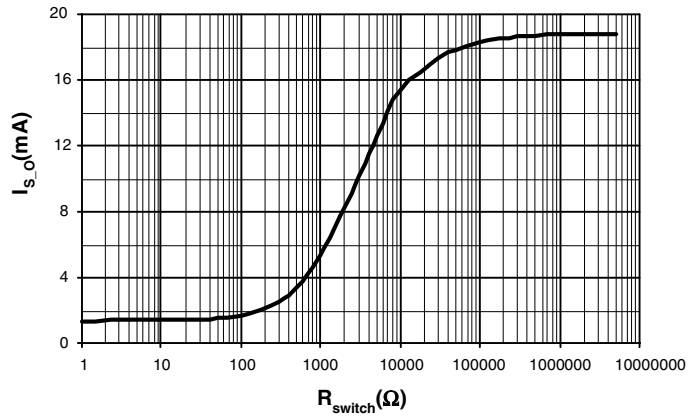


Figure 8. PA (PSSO20): Output Power and PAE versus Supply

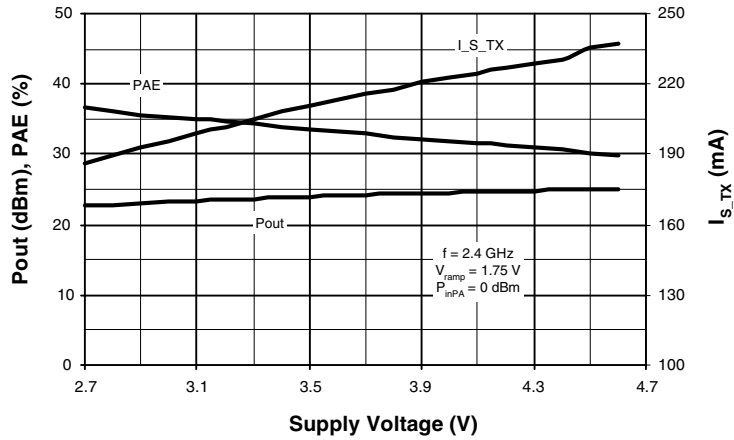


Figure 9. PA (PSSO20): Output Power and PAE versus Ramp Voltage

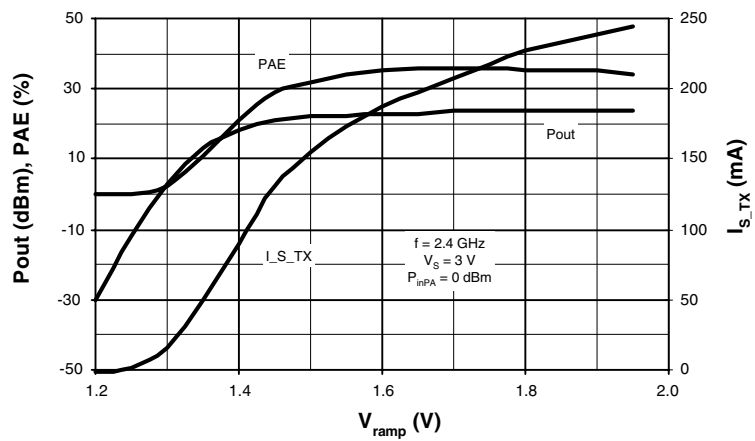


Figure 10. PA (PSSO20): Output Power and PAE versus Input Power

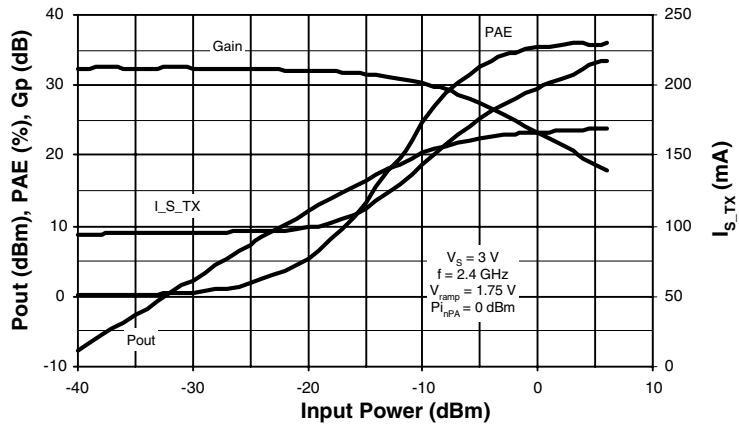


Figure 11. PA (PSSO20): Output Power and PAE versus Frequency

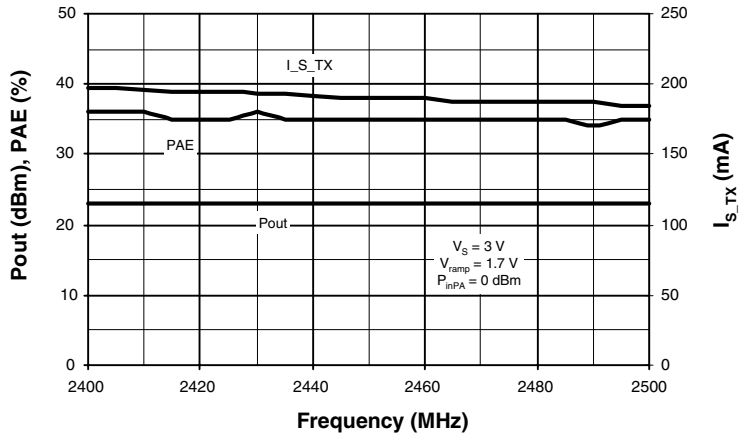


Figure 12. PA (QFN20): Output Power and PAE versus Supply Voltage

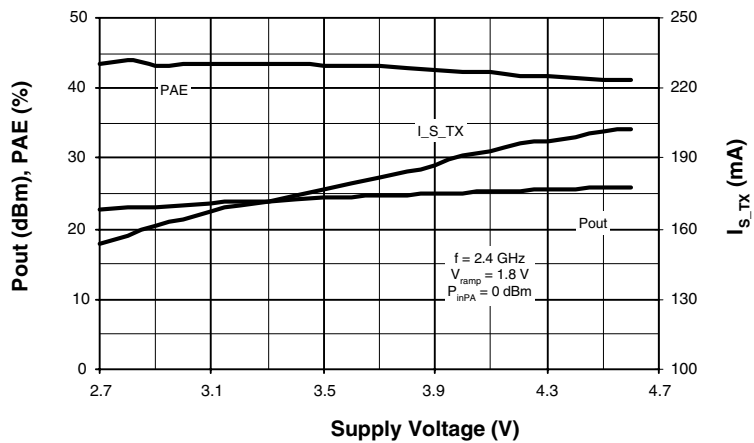


Figure 13. PA (QFN20) Output Power and PAE versus Ramp Voltage

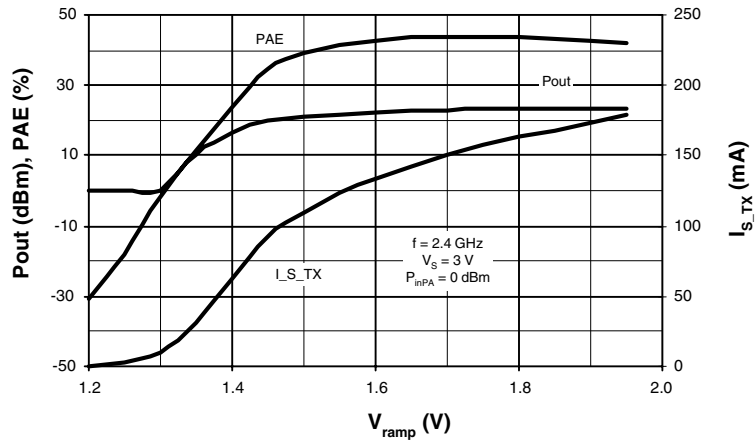


Figure 14. PA (QFN20): Output Power and PAE versus Input Power

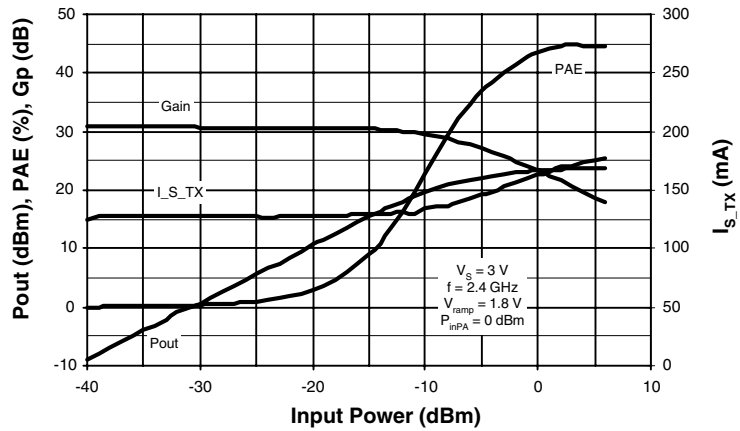


Figure 15. PA (QFN20): Output Power and PAE versus Frequency

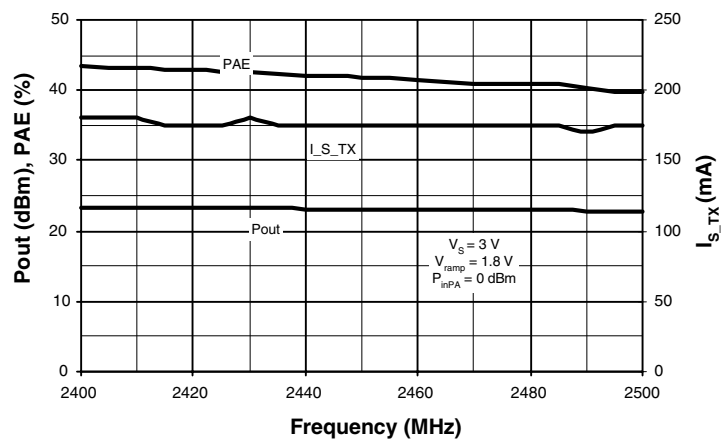


Figure 16. LNA: Supply Current versus Temperature

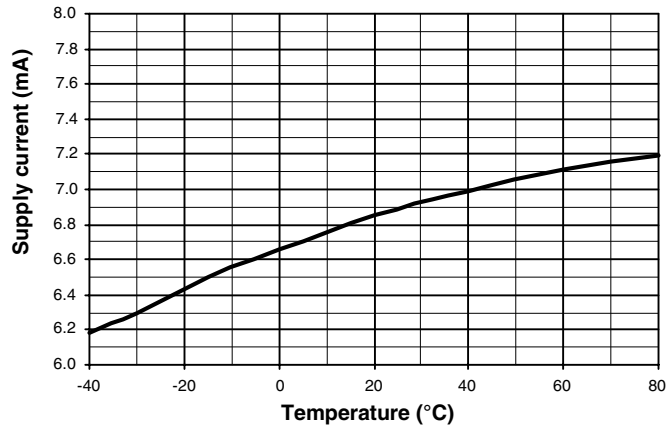


Figure 17. PA (PSSO20): Supply Current versus I_{ramp} and Temperature

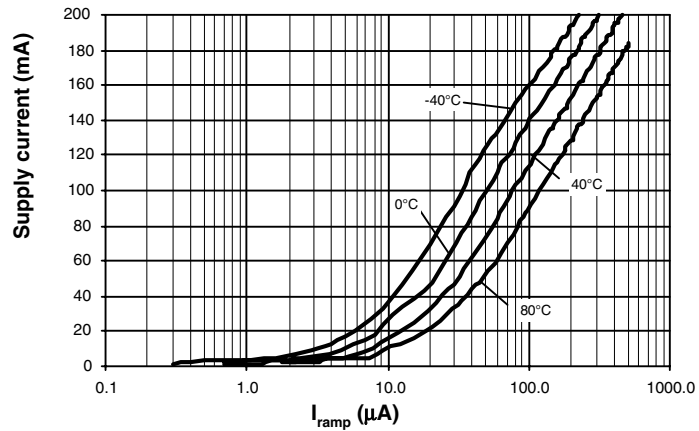


Figure 18. PA (PSSO20, QFN20): P_{out} versus V_{ramp} and Temperature

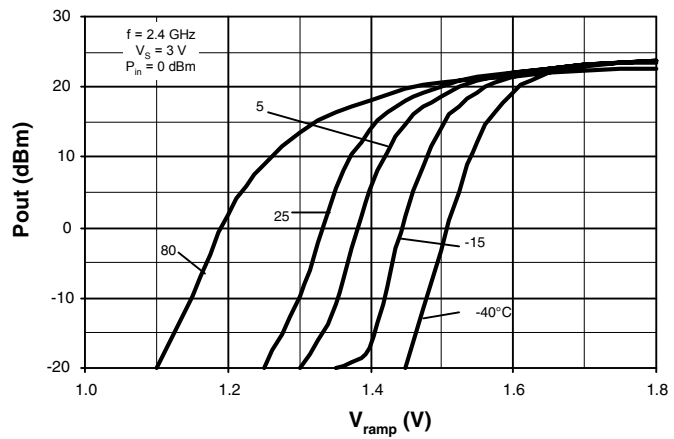
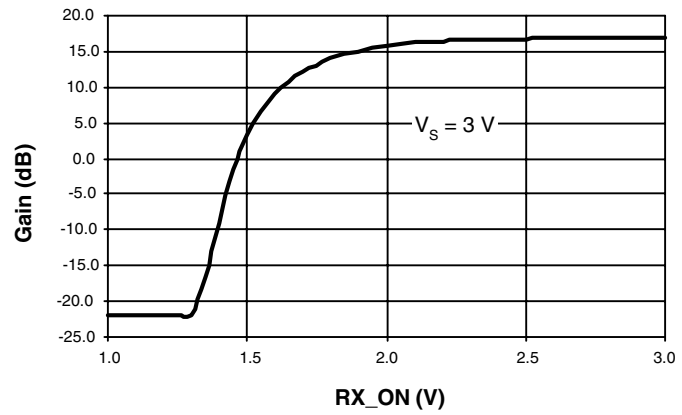


Figure 19. (PSSO20, QFN20): LNA Gain (dB) versus RX_ON (V)



Input/Output Circuits

Figure 20. Input Circuit PA_IN/V1_PA

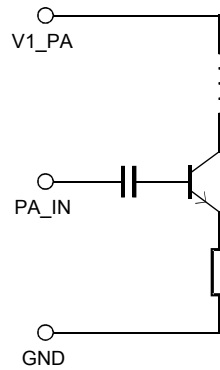


Figure 21. Input Circuit RAMP/V1_PA

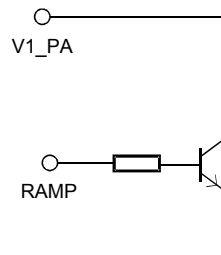


Figure 22. Input Circuit V2_PA

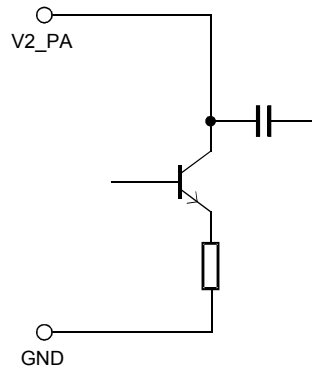


Figure 23. Input/Output Circuit V3_PA_OUT

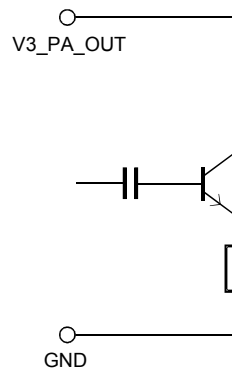


Figure 24. Input Circuit SWITCH_OUT/R_SWITCH

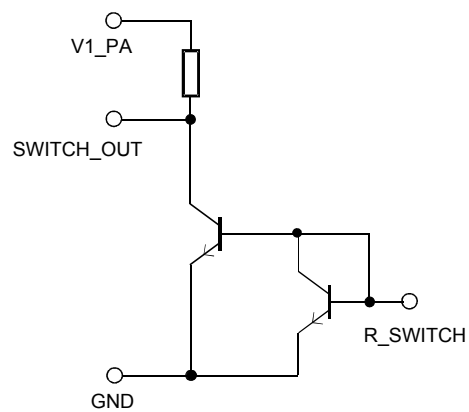


Figure 25. Input Circuit LNA_IN/VS_LNA

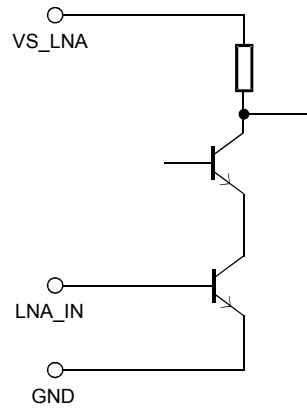


Figure 26. Input Circuit PU/RX_ON

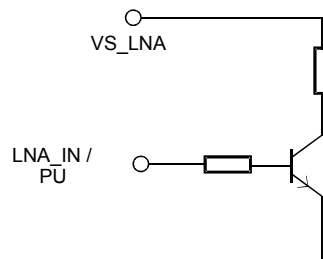


Figure 27. Output Circuit LNA_OUT

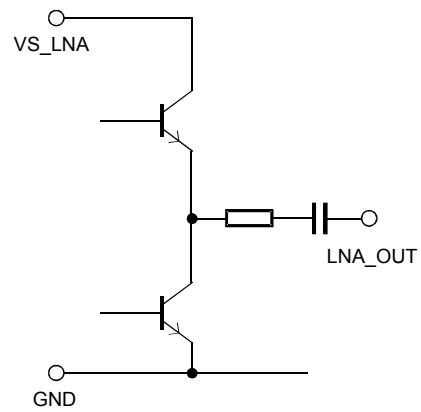


Figure 28. Typical Application T7024 (PSSO20 Package)

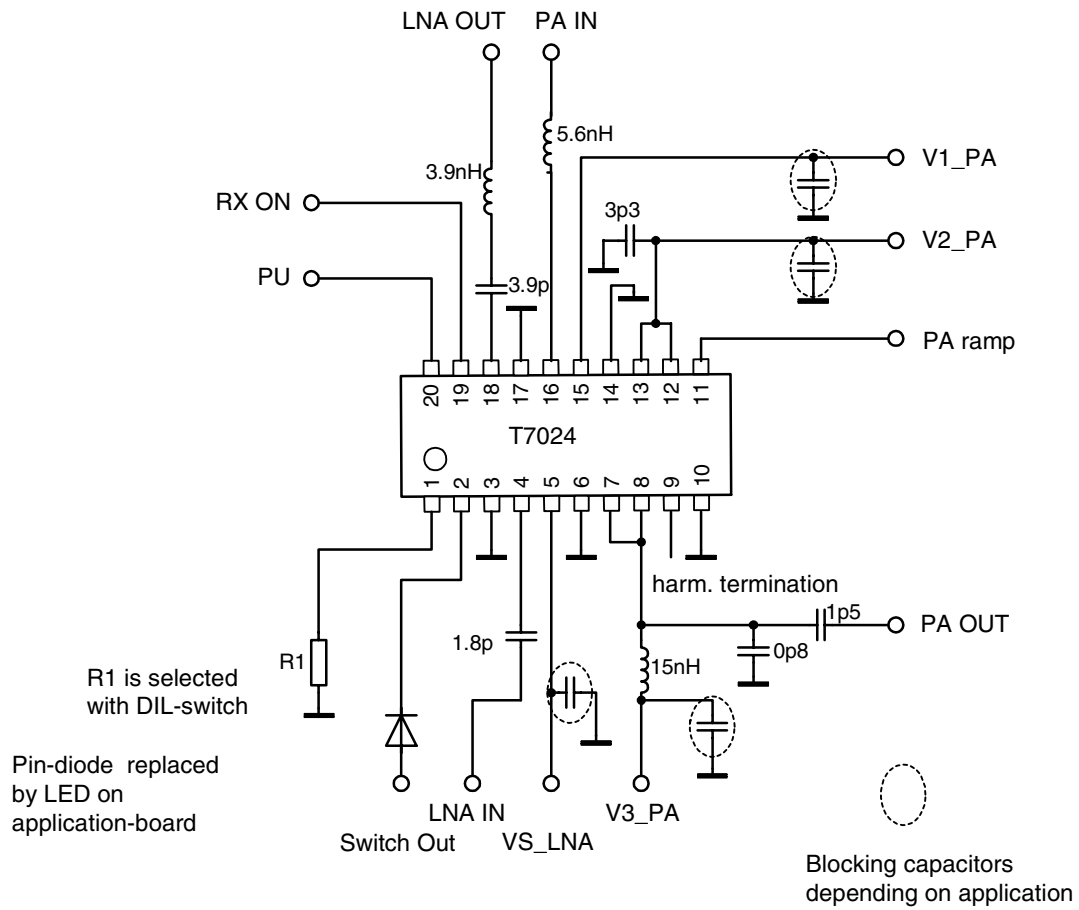
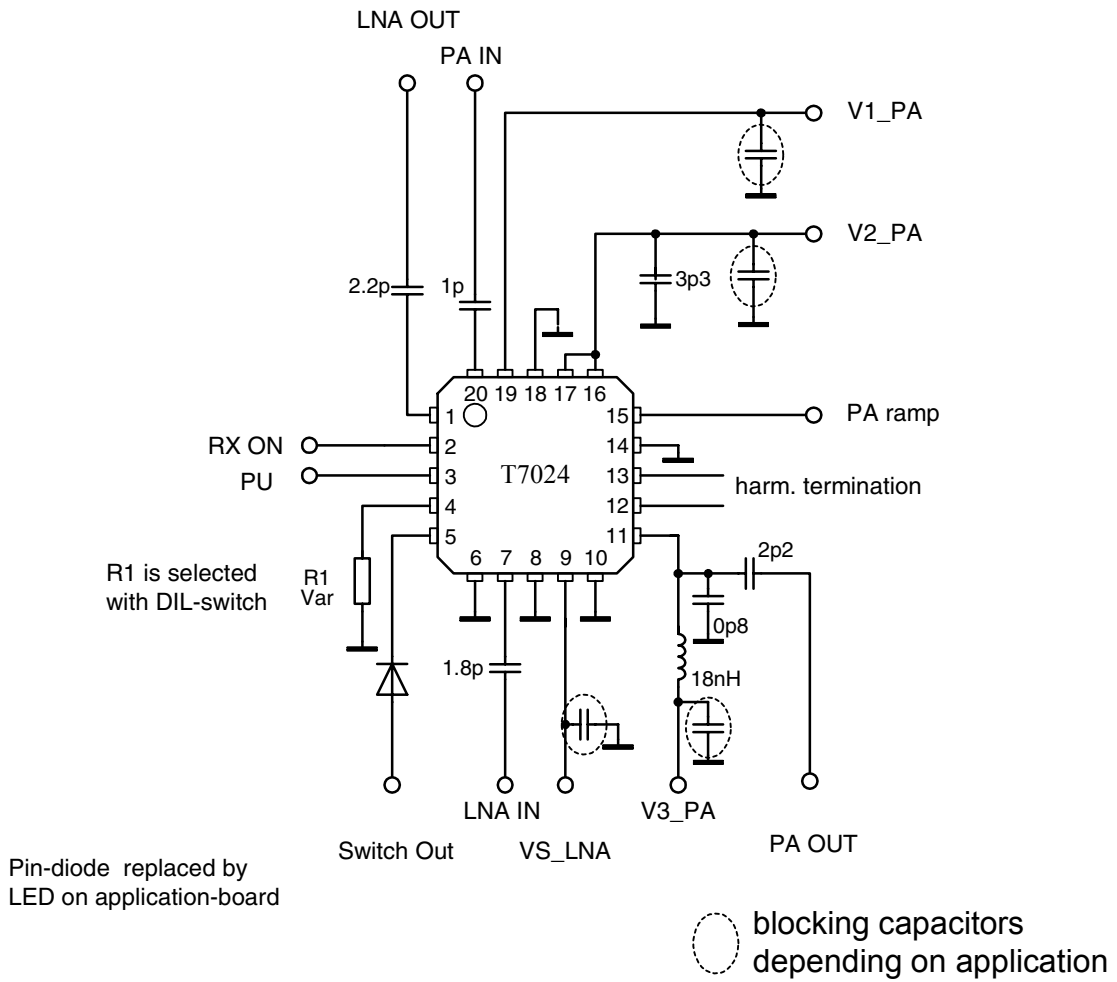


Figure 29. Typical Application T7024 (QFN20 Package)



Ordering Information

| Extended Type Number | Package | Remarks | MOQ |
|----------------------|---------|------------------|-----------|
| T7024-TRS | PSSO20 | Tube | 830 pcs. |
| T7024-TRQ | PSSO20 | Taped and reeled | 4000 pcs. |
| T7024-PGP | QN20 | Taped and reeled | 1500 pcs. |
| T7024-PGQ | QFN20 | Taped and reeled | 6000 pcs. |

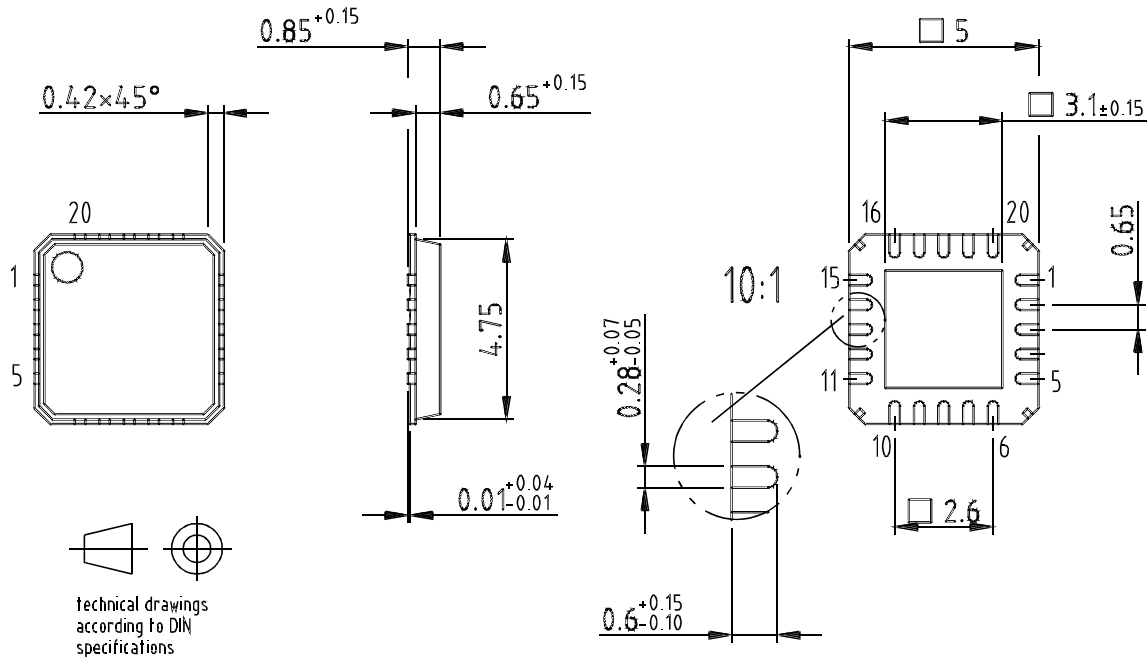
Package Information

Package: QFN 20 - 5x5

Exposed pad 3.1x3.1

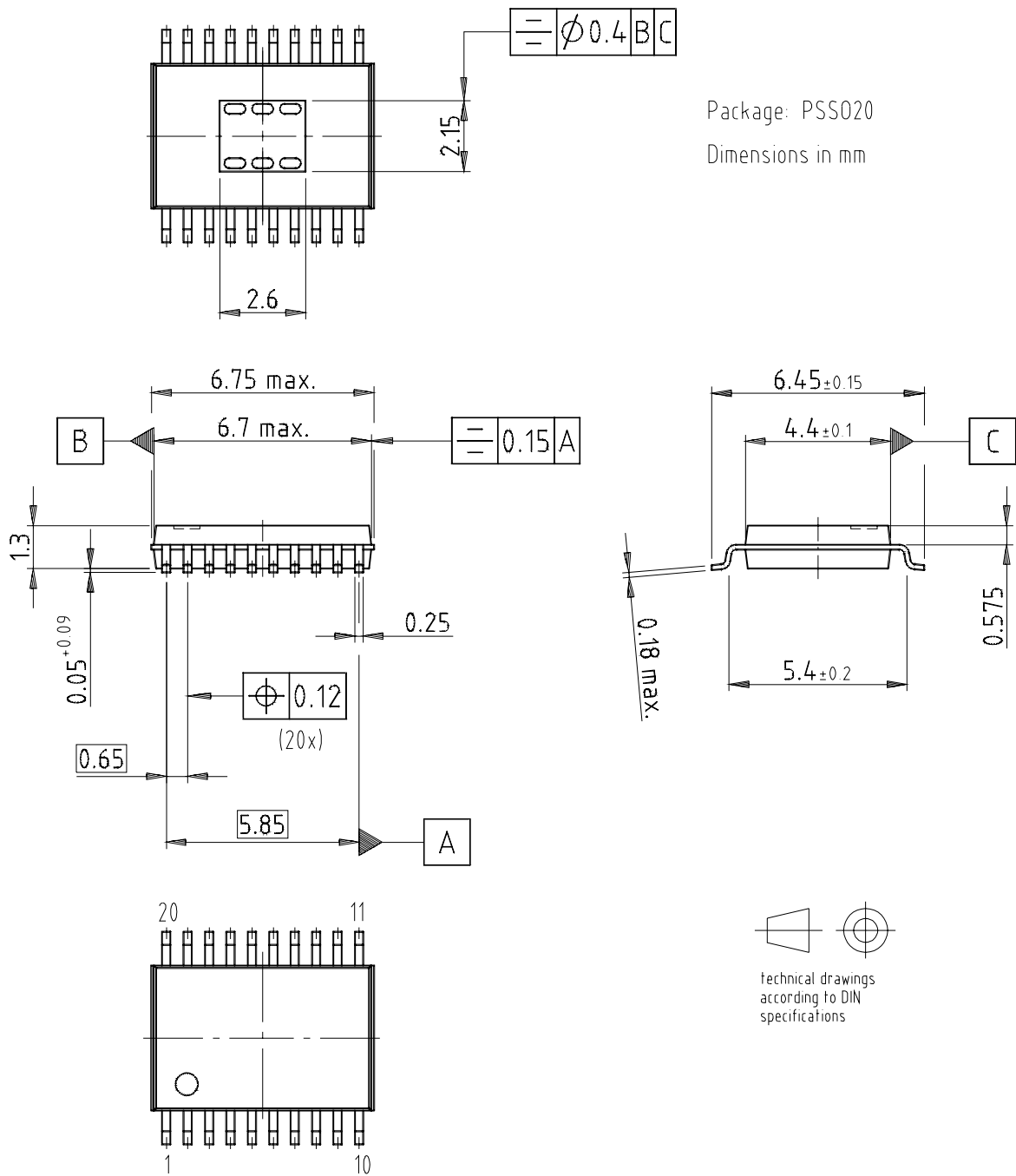
(acc. JEDEC OUTLINE No. MO-220)

Dimensions in mm



Drawing-No.: 6.543-5069.02-4

Issue: 3; 24.01.03



Drawing-No.: 6.543-5078.01-4
Issue: 1; 05.06.01



Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe

Atmel Sarl
Route des Arsenalux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia

Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan

9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards

Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive

Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/ High Speed Converters/RF Datacom

Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

Literature Requests

www.atmel.com/literature

Disclaimer: Atmel Corporation makes no warranty for the use of its products, other than those expressly contained in the Company's standard warranty which is detailed in Atmel's Terms and Conditions located on the Company's web site. The Company assumes no responsibility for any errors which may appear in this document, reserves the right to change devices or specifications detailed herein at any time without notice, and does not make any commitment to update the information contained herein. No licenses to patents or other intellectual property of Atmel are granted by the Company in connection with the sale of Atmel products, expressly or by implication. Atmel's products are not authorized for use as critical components in life support devices or systems.

© Atmel Corporation 2004. All rights reserved.

Atmel® and combinations thereof are the registered trademarks of Atmel Corporation or its subsidiaries.
The Bluetooth name and the Bluetooth trademarks are owned By Bluetooth SIG, and are used by Atmel Corporation under license.
Other terms and product names may be the trademarks of others.



Printed on recycled paper.

4533D-BLURF-01/04