Octal 10/100 Switch with Embedded Memory

The T71L6808A is an octal-port 10/100Mbps dual speed Ethernet switch integrated both with an embedded SSRAM and a 1K entries of address table. A high performance Fast Ethernet switch, fully complies with the IEEE802.3, 802.3u and 802.3x specifications, can be implemented using the T71L6808A with physical devices. The T71L6808A is intended for applications to stand-alone switch for low-cost SOHO market.

Features

- Supports eight 10/100Mbps Ethernet ports with RMII interface
- Fully non-blocking shared memory architecture using page-based embedded SSRAM.
- Incorporating with the output private buffering scheme to prevent HOL (head of line) blocking
- Wire-speed store-and-forward switching with low switching latency. Automatic address learning, local frames filtering, and adjustable aging
- Embedded 1K entries of look-up table
- Supports full and half duplex operations
- Link, speed and duplex status are auto-detected via MDIO
- Auto-negotiated Full-duplex flow control by writing the ability via MDIO to external PHY
- Supports IEEE 802.3x flow control for full-duplex operation
- Supports back-pressure flow control for half-duplex operation
- Serial EEPROM interface for auto-configuration
- Broadcast storm control
- Port trunking & load sharing
- Port-based VLAN
- Port monitoring(snooping or mirroring)
- Supports port priority per port basis QoS
- Only one 50MHz OSC
- 128-pin PQFP, 3.3V CMOS technology

General Description

The T71L6808A is a highly integrated, octal port, 10-BaseT/100Base-TX, RMII interface, Ethernet switch implemented in 0.18um CMOS technology. The T71L6808A supports a wide variety of switch features and configurations at the maximum performance levels with the lowest number of components per switch.

The switch chip supports store-and-forward switching scheme with built-in storage of incoming/ outgoing packets as well as address table. The T71L6808A adopts page-based memory architecture in order to fully utilize the embedded packet buffer. It can recognize up to 1024 different MAC addresses and enables filtering and forwarding at non-blocking 148800 packets/second wire speed.

The function modules integrated in the switch chip include 8 full-duplex compatible media access controller (MAC) with RMII interface to PHYs, address resolution logic(ARL) for MAC address searching, self-learning and automatic aging, and buffer management unit (BMU).

The T71L6808A supports IEEE 802.3x full duplex flow control and half duplex back pressure control. The ability of IEEE 802.3x flow control is auto-negotiated by writing the flow control ability via MDIO. Speed, duplex, link status and flow control can be acquired by periodically polling the status of the PHY devices via MDIO.

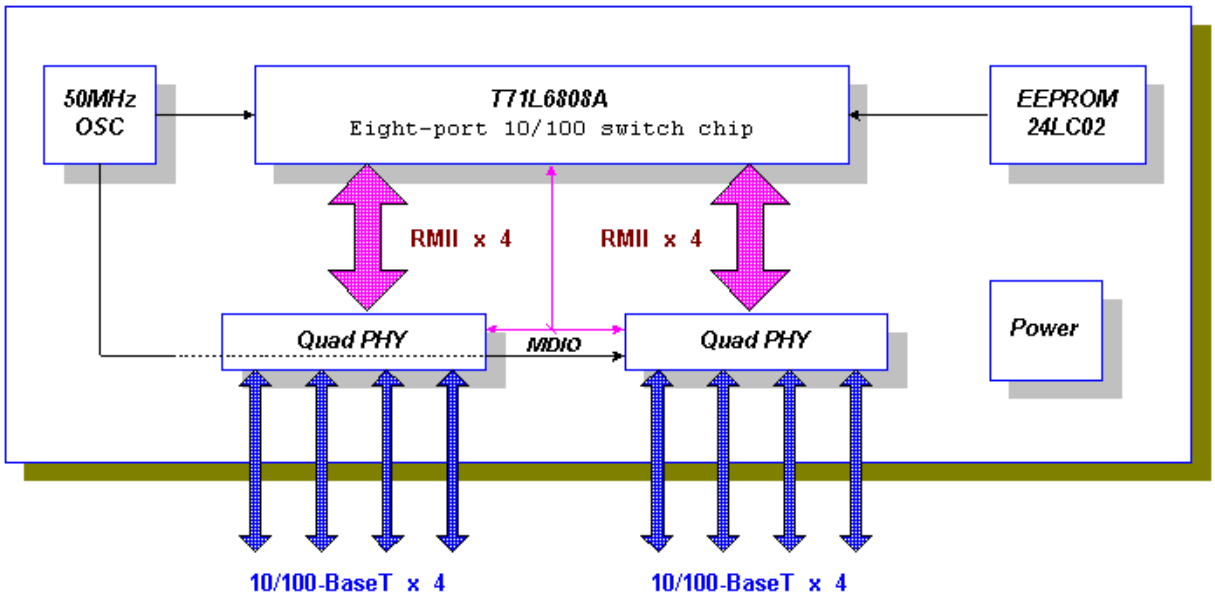
Port-based VLAN function is also provided by T71L6808A. With the aid of VLAN, broadcast packet issued within certain VLAN group will not affect the activities in other VLAN group. The two groups of four ports are suitable for SOHO application at two different working groups.

The T71L6808A also supports trunking applications. With trunking, it is possible to group up to two full-duplex links together to form a single 400 Mbit/s link.

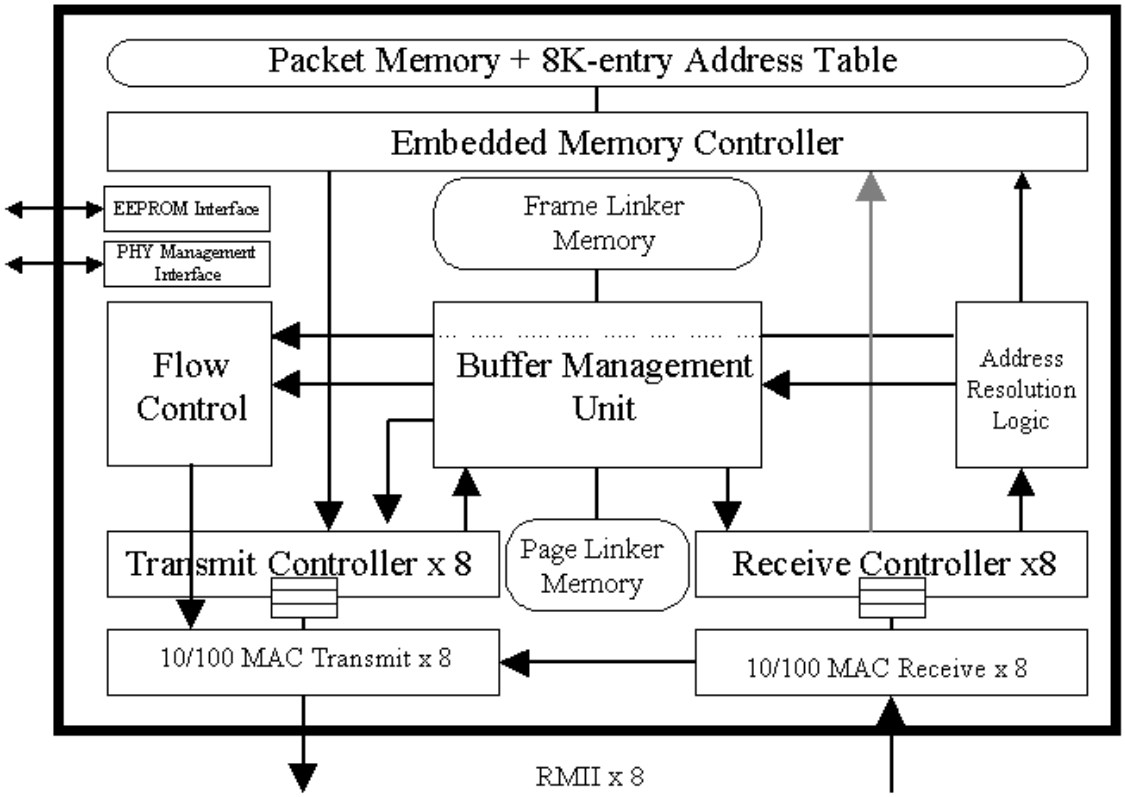
T71L6808A provides port priority to allow video servers to broadcast or unicast full color video traffic, that is, all the packets from this priority port will be forwarded to priority queue of each transmitting port.

The initialization and configuration of the switch is programmed by an external EEPROM. However, the chip can operate normally with default configuration.

System Diagram



Block Diagram



Functional Description

Reset

After power on reset, the T71L6808A will determine some features from ENFCTRL and ENBKPRS pins, auto-load the content of 24LC02 serial EEPROM, and write abilities to connected PHY management registers via MDC/MDIO.

RMII Interface

The T71L6808A provides 10/100 Mbps low pin count RMII interface for use between PHY and T71L6808A. The RMII is capable of supporting 10Mbps and 100Mbps data rates. A single clock reference, 50MHz, sourced from an external clock input is used for receive and transmit. It also provides independent 2 bit wide (di-bit) transmit and receive data paths. As the REFCLK is 10 times the data rate in 10Mbps mode each data di-bit must be output on TXD[1:0] and input on RXD[1:0] for ten consecutive REFCLK cycles.

RMII specification signals are as follows,

Signal Name	Direction (with respect to the PHY)	Direction (with respect to the T71L6808A)	Use
REFCLK	Input	Input	Synchronous clock reference for receive, transmit and control interface.
CRSDV	Output	Input	Carrier Sense/Receive Data Valid
RXD[1:0]	Output	Input	Receive Data
TXEN	Input	Output	Transmit Enable
TXD[1:0]	Input	Output	Transmit Data

Data Reception

The data reception port will go into the receive-state when CRS in the RMII interface is asserted. The RMII (Reduced Media Independent Interface) presents the received data in two-bit (di-bit) that are synchronous to the RMII reference clock (50 MHz). The T71L6808A will then attempt to detect the occurrence of the SFD (Start Frame Delimiter) pattern "10101011." All preamble data prior to SFD are discarded. Once SFD is detected from the RMII interface, the frame data is forwarded and stored in the buffer of the switch.

Illegal Frames

The T71L6808A will discard all illegal frames such as runt packet (less than 64 bytes), oversize packet (greater than 1518 or 1522 bytes) and bad CRC.

Frame Forwarding

After a packet is received, both source address (SA) and destination address (DA) are retrieved. The SA is used to update the port's address table and the DA is used to determine the frames destination port. The Address Resolution Logic will attempt to match the destination address with the addresses stored in the address table and then forwards the packet to the other port, if appropriate.

If the first bit of the destination address is "0," the frame is regarded as an unicast packet. The Address Resolution Logic uses address hashing algorithm or direct mapping method to search destination address and returns a matched destination port number to identify which port the packet should be forwarded to. If the destination port is within the same VLAN of the receiving port, the packet will be forwarded. If the destination port does not belong to the VLANs specified at the receiving ports, the packet will be discarded.

If the destination address is not found in the address table, the T71L6808A treats the packet as a broadcast packet and forwards the packet to the other ports.

If the port monitoring function is enabled, the packet forwarding decision is also subject to the port monitoring configurations.

If the first bit of the destination address is a "1," the packet will be handled as a multicast or broadcast frame. The destination ports of the broadcast packet are all ports within the same VLAN except the source port itself.

The T71L6808A automatically learns the port number of attached network devices by examining the source MAC address of all incoming packets. If the source address is not found in the address table, the switch IC adds it to the table.

Address Learning

TheT71L6808A provides an on-chip 1K MAC Address-to-PortID table for the frame destination look-up operations. It uses a hashing algorithm to learn the MAC address. The T71L6808A searches for the source address (SA) of an incoming packet in the address table and acts as follows : If the SA was not found in the address table(a new address), the T71L6808A waits until the end of the packet (no-error packet) and updates the address table. If the SA was found in the address table, then aging value of each corresponding entry will be reset to 0.

The Individual MAC Address is a 48-bit unique MAC address to be programmed or learned. Bit 0 of a SA will be masked, i.e. no multicast SA.

When the DA is PAUSE command, then the learning process will be disabled automatically by T71L6808A.

Address Aging

If the SA aging option is enabled, the learned SA will be cleared if it is not refreshed within the 300 seconds.

Broadcast Storm Control

The T71L6808A supports broadcast storm control on a per-port basis. Broadcast packets will be forwarded to all ports except the source port and thus will use too much of the switch resources

(bandwidth and available space in transmit queues). The T71L6808A will discard broadcast or multicast packets if the number of those packets exceeds the threshold .

Data Transmission

The T71L6808A transmits all packets in accordance to IEEE 802.3 standard. The T71L6808A will send the packets with a guaranteed minimum IPG (Inter Packet/Frame Gap) of 96BT even if the received packets have an IPG less than the minimum requirement. The IPG is 9.6us for 10Mbps Ethernet and is 960ns for 100Mbps fast Ethernet.

During a transmit process the packet data is read from the memory buffer and forwarded to the destination port's PHY device in di-bits. Seven bytes of preamble signal (10101010) will be generated first before the SFD (10101011). Frame data is sent after the SFD along with four-bytes of FCS at the end.

Back off Algorithm

The T71L6808A implements the truncated exponential back off algorithm compliant to 802.3 standard. The collision counter will be restarted after 16 consecutive collision.

Head-Of-Line Blocking

The T71L6808A incorporate a simple mechanism to prevent Head-Of -Line blocking problem when flow control is disabled. When flow control function is disabled, the T71L6808A will first check the

destination address of incoming packet. If the destined port is congested, the T71L6808A will discard this packet to avoid the blocking of next packet which is going to loose traffic port.

Flow Control

The T71L6808A supports IEEE 802.3x full duplex flow control and half duplex back pressure congestion control. The IEEE 802.3x flow control's ability is auto-negotiated between remote device and the T71L6808A by writing the flow control ability via MDIO to external connected PHY. The T71L6808A adopts a special back-pressure design, forwarding one packet successfully after 28 force collisions, to avoid the connected repeater being partitioned. The full duplex flow control ability can be enabled or disabled via ENFCTRL pin. And the half duplex back pressure function can be enabled or disabled via the ENBKPRS pin.

Port-based VLAN

T71L6808A can be divided up to 2 different VLAN groups by programming VLAN. Broadcast

packets (include broadcast DA and DA search missed packet) will be forwarded to those ports belong to the same VLAN group. When VLAN is programmed to 1, port 0-3 and port 4-7 are belong to two different VLAN groups. Two VLAN groups are not overlapped, thus one T71L6808A can support two 4 ports switch function whenever VLAN is programmed high.

Port Trunking

Trunking allows two ports to be connected in parallel between two switches to increase the interconnection bandwidth. The trunking algorithm determines on which of these ports a frame is transmitted so that the load is spread across these ports. However, while traffic should be shared between trunking ports as evenly as possible. The T71L6808A supports port 0 and port 1 to be one trunk group. Hense, the maximum aggregated bandwidth for trunking group is 400Mbps. (or 200Mbps, bi-directional)

Port Monitoring

The T71L6808A supports port monitoring. This feature provides complete network monitoring capability at 100 Mbit/s. A copy ingress (RX) data of the monitored port is sent to their respective snooping ports. The monitored port is selected by MPID. The T71L6808A allows receive data to be monitored by different snooping ports. The snooping ports are also selected by SPID.

Priority

In Multimedia application, the audio & voice message is time critical to users. Normally it might have discontinue phenomenon through the Ethernet network, especially if the network segment utilization more than 30%, the message can not reach users in time.

The T71L6808A supports port priority per port basis QoS. Continuous priority traffic to a destination port will take precedence against normal continuous traffic to the same destination port. Packets from priority ports will arrive at the destination port earlier than packets arrived from normal ports. Priority rules apply for ports in any speed mode and duplex mode.

T71L6808A has 2 queues for each port: One for regular traffic, another for priority traffic. The packets coming from the port(s) with priority setup (QoS) will go to the priority queue of the destination port.

Serial Management Interface MDC/MDIO

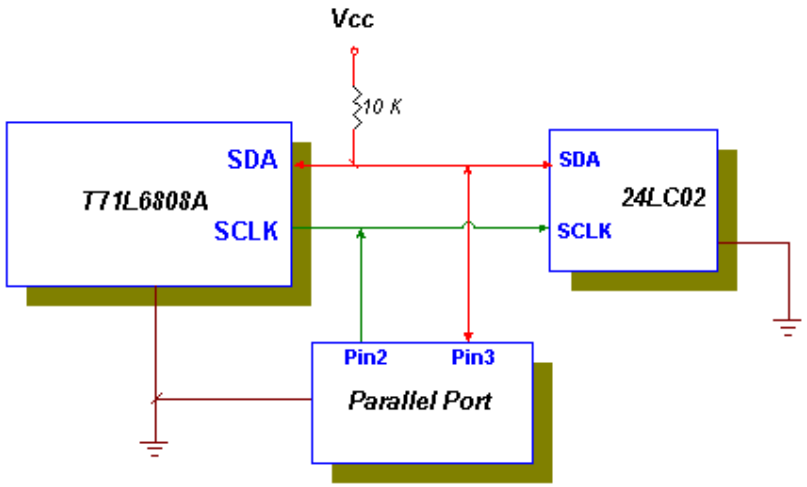
The T71L6808A supports PHY management through the serial MDIO and MDC signal lines. After power on reset, the T71L6808A write abilities to the advertisement register 4 of connected PHY and

restart the auto-negotiation process through MDIO using PHY address increasingly from 01000b to 01111b. After restarting auto-negotiation, the T71L6808A will continuously poll the link status and link partner's ability which including speed, duplex and flow control of the PHY devices via MDIO. The following is the management frame format :

Operation	*PRE*	*ST*	*OP*	*PHYAD*	*REGAD*	*TA*	*DATA*	*IDLE*
Read	1…1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
Write	1…1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

24LC02 Interface

The 24LC02 interface is a 2-wire serial EEPROM interface providing 2K bits storage space. After power on reset, the T71L6808A uses Random Read and Sequential Read commands to auto-load configuration settings, pause frame source address and so on. After auto-loaded, the 24LC02 interface pins SCL and SDA are tri-stated for on-line updating 24LC02 contents through a parallel port.



24LC02 Device Operation

Clock and Data transitions: The SDA pin is normally pulled high with an external register. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods will indicate a start or stop condition as defined below.

Start condition: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command.

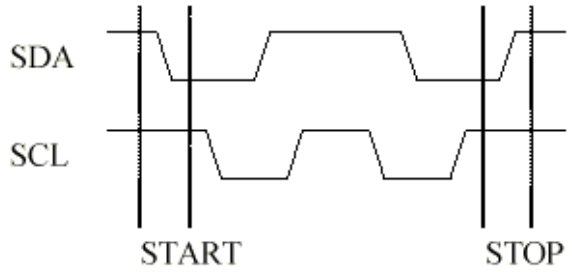
Stop condition: A low-to-high transition of SDA with SCL high is a stop condition.

Acknowledge: All addresses and data words are serially transmitted to and from the EEPROM in 8 bit words. The 24LC02 sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

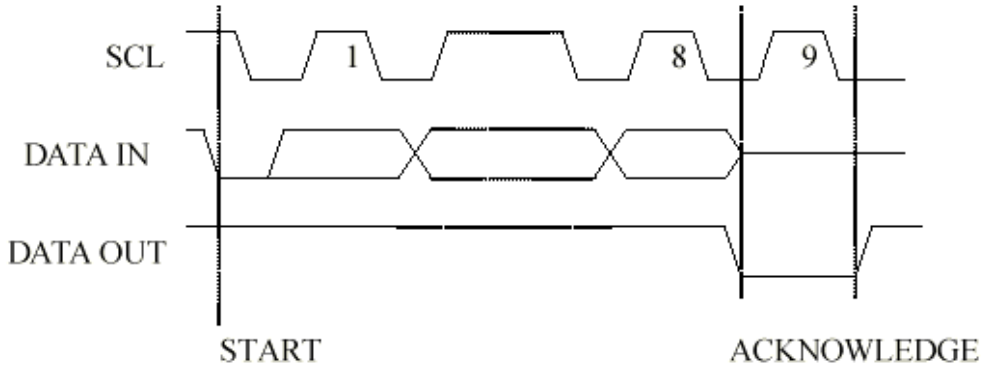
Random Read: A random read requires a "dummy" byte write sequence to load in the data word address.

Sequential Read: For T71L6808A, the sequential reads are initiated by a random address read. After the 24LC02 receives a data word, it responds with an acknowledge. As long as the 24LC02 receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words.

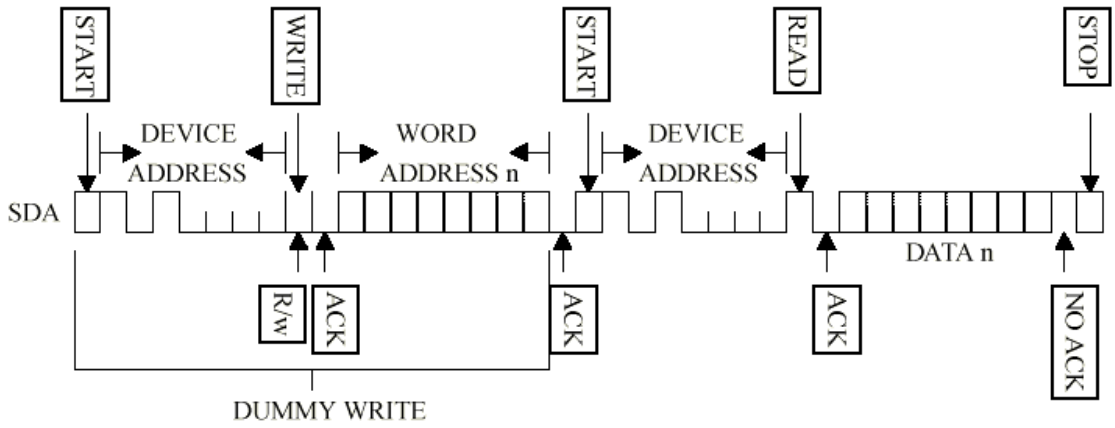
**Start and Stop Definition*



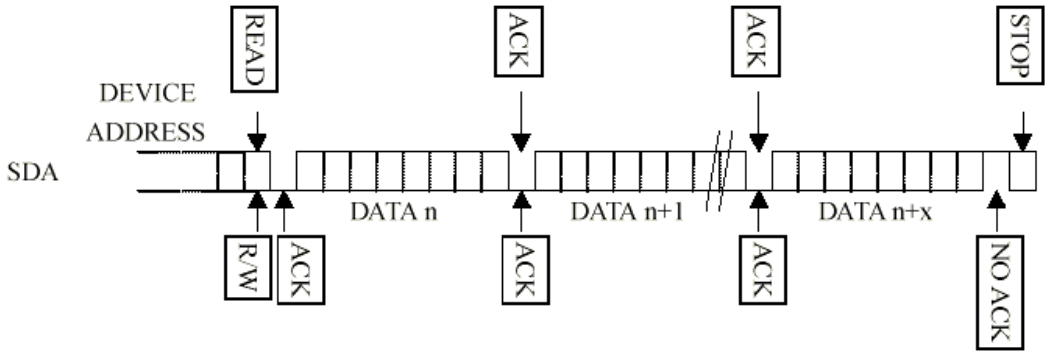
**Output Acknowledge*



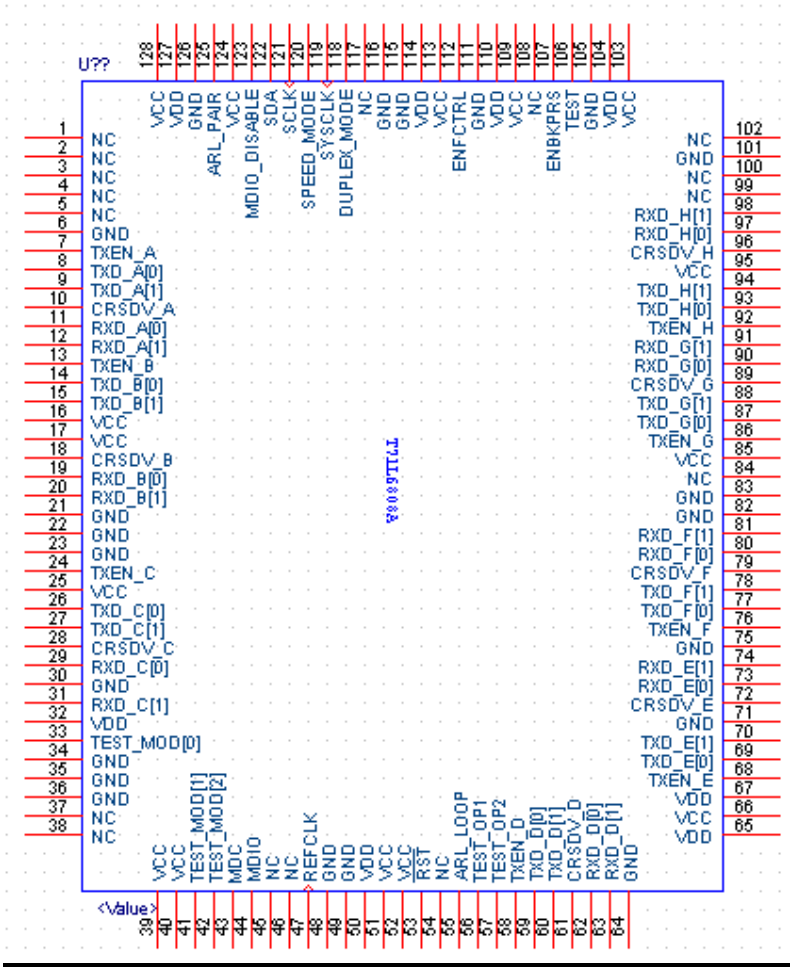
*Random Read



*Sequential Read



Pin Assignment



Pin Description

Symbol	I/O	Pin No.	Function
RMII Interface			
REFCLK	I	47	**Reference Clock.** REFCLK is a 50MHz clock that provides the timing reference for CRS_DV, RXD[1:0], TX_EN and TXD[1:0].
TXD[1:0][A] TXD[1:0][B] TXD[1:0][C] TXD[1:0][D] TXD[1:0][E] TXD[1:0][F] TXD[1:0][G] TXD[1:0][H]	O	8,9 14,15 26,27 59,60 69,70 77,78 87,88 93,94	**Transmit Data.** TXD[1:0] shall transition synchronously with respect to REFCLK. When TX_EN is asserted, TXD[1:0] are accepted for transmission by the PHY.
TXE[A:H]	O	7,13,24,58 68,76,86,92	**Transmit Enable.** TX_EN indicates that the MAC is presenting di-bits on TXD[1:0] on the RMII for transmission. It shall transmit synchronously with REFCLK.
RXD[1:0][A] RXD[1:0][B] RXD[1:0][C] RXD[1:0][D] RXD[1:0][E] RXD[1:0][F] RXD[1:0][G] RXD[1:0][H]	I	11,12 19,20 29,31 62,63 73,74 80,81 90,91 97,98	**Receive Data[1:0].** RXD[1:0] shall transition synchronously to REFCLK. For each clock period in which CRS_DV is asserted, RXD[1:0] transfers two bits of recovered data from the PHY.
CRSDV[A:H]	I	10,18,28,61 72,79,89,96	**Carrier Sense/Receive Data Valid.** CRS_DV shall be asserted by the PHY when the receive medium is non-idle and asserted asynchronously on detection of carrier due to the criteria relevant to the operating mode.
System Pins			
RST#	I	53	**Reset.** Asynchronous active low reset signal
SYSCLK	I	119	**System Clock.** System clock, 50MHz

Management Interface (MI)			
MDC	O	43	**Management Interface (MI) Clock Output.** This MI clock shifts serial data in and out of MDIO on rising edges from an external Physical Layer device.
MDIO	I/O	44	**Management Interface (MI) Data I/O.** This bi-directional pin contains serial data that is clocked in and out on rising edges of the MDC clock from an external Physical Layer device.
Serial EEPROM 24LC02 Interface			
SCLK	O	121	**Serial Clock.** Internally pulled high.
SDA	I/O	122	**Serial Data Input/Output.** Internally pulled high.
Mode Pins (Reset-read)			
ENBKPRS	I	107	**Enable Half Duplex Back Pressure Function.** Pulled high upon reset will enable the back pressure function. Pulled low upon reset will disable the back pressure function.
ENFCTRL	I	112	**Enable Full Duplex Flow Control.** Pulled high upon reset will enable the full duplex IEEE802.3x flow control function. The flow control ability will be write to the management register 4 of PHY device one and only one time after power-on reset, for advertising. Pulled low upon reset will disable the flow control function.
Test Pin			
TEST	I	106	**Test Pin.** For internal use. Must be tied to ground for normal use.
TEST_MOD [2:0]	I	33, 41, 42	**Test Pin.** For internal use.
TEST_OP1	O	56	**SSRAM Test Output.** For internal test.
TEST_OP2	O	57	**SSRAM Test Output.** For internal test.
ARL_LOOP	I	55	**Test Pin.** For internal use. Must be tied to ground for normal use.
ARL_PAIR	I	125	**Test Pin.** For internal use. Must be tied to ground for normal use.

MDIO_ DISABLE	I	123	**Test Pin.** For internal use. Must be tied to ground for normal use.
SPEED_ MODE	I	120	**Test Pin.** For internal use. Must be tied to ground for normal use.
DUPLEX_ MODE	I	118	**Test Pin.** For internal use. Must be tied to ground for normal use.
Power Ground Pin			
GND		6,21,22,23, 30,34,35,36, 48,49,64,71, 75,82,83,101, 105,111,115,116, 126	
VCC		16,17,25,39, 40,51,52,66, 85,95,103,109, 113,124,128	

Serial EEPROM 24LC02 Format

Below is the content of serial EEPROM 24LC02. The content includes configuration and CRC for flow control.

Bit / Byte	7	6	5	4	3	2	1	0
0	BRDCTRL	0	0	0	0	0	0	0
1	0	HashMode	0	0	0	0	0	0
2-7	Pause Frame Source Address PSA[47:0]							
8-11	Pause ON CRC[31:0]							
12-15	Pause OFF CRC[31:0]							
16	Port Priority PR[7:0]							
17	0	0	0	0	TrunkEn	0	AgeEn	VLAN
18	0	SnoopEn	MPID[2:0]			SPID[2:0]		

BRDCTRL: When 0, the broadcast storm control function is disabled.
When 1, the broadcast storm control function is enabled.
HashMode: When 1, address hashing algorithm used for search and learning.
When 0, address direct mapping algorithm used.

PR[7:0]: When 1, high priority for corresponding transmission port.
When 0, low priority for corresponding transmission port.
TrunkEn: When 0, port trunking disable.
When 1, port trunking enable, assign port 0 and port 1 to the trunking group.
AgeEn: When 0, the table aging process will be stopped.
When 1, the table aging process will be running to age every learned table entry.
Default value is 1 (i.e. age enable)
VLAN: When 0, all 8 ports are in the same VLAN.
When 1, two groups VLAN 0-3 and 4-7.
SnoopEn: When 0, snooping disable.
When 1, snooping enable.
MPID[2:0]: Monitored Port ID.
SPID[2:0]: Snooping Port ID for incoming frame flow.

Note : All 0-fields must be filled with 0.

Temperature Limit Ratings

Parameter	Minimum	Maximum	Unit
Storage temperature	-55	+125	J
Operating temperature	0	70	J

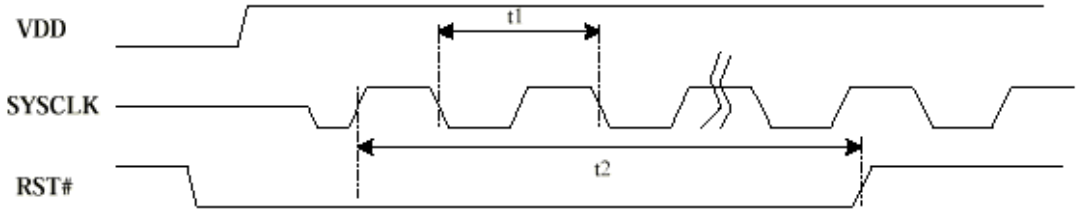
DC Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{OH}	Minimum High Level Output Voltage	I_{OH} =-8mA	0.9* V_{CC}		V_{CC}	V
V_{OL}	Maximum Low Level Output Voltage	I_{OL} =8mA			0.1* V_{CC}	V
V_{IH}	Minimum High Level Input Voltage		0.5* V_{CC}		$V_{CC+0.5}$	V
V_{IL}	Maximum Low Level Input Voltage		-0.5		0.3* V_{CC}	V
I_{IN}	Input Current	V_{IN} = V_{CC} or GND	-1.0		1.0	uA
I_{OZ}	Tri-State Output Leakage Current	V_{OUT} = V_{CC} or GND	-1.0		1.0	uA
I_{CC}	Average Operating Supply Current	I_{OUT} =0mA		160	180	mA

AC Characteristics

Reset and Clock Timing

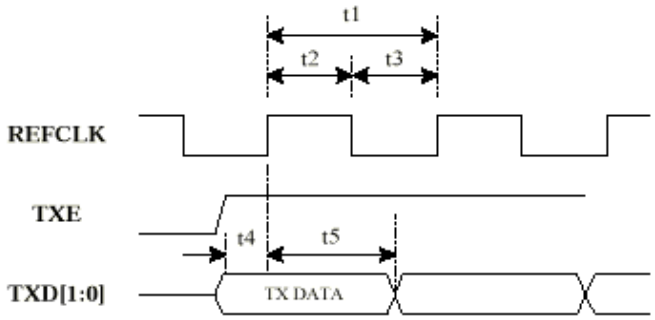
Symbol	Description	Minimum	Typical	Maximum	Units
$f_{clock\ (SYSCK)}$	SYSCLK clock frequency	40	50	66	MHZ
t1	SYSCLK clock period	15	20	25	ns
t2	RST# low pulse duration	1000	-	-	ns



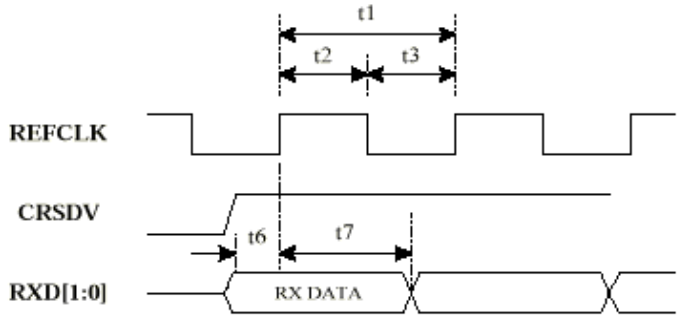
Reset and Clock Timing

RMII Timing

Symbol	Description	Minimum	Typical	Maximum	Units
t1	REFCLK clock period	-	20	-	ns
t2	REFCLK high level width	-	10	-	ns
t3	REFCLK low level width	-	10	-	ns
t4	TXE ,TXD to REFCLK rising setup time	4	-	-	ns
t5	TXE ,TXD to REFCLK rising hold time	2	-	-	ns
t6	CSRDV ,RXD to REFCLK rising setup time	4	-	-	ns
t7	CRSDV ,RXD to REFCLK rising hold time	2	-	-	ns



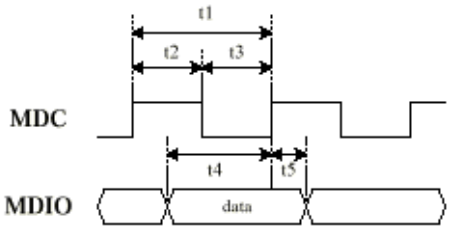
RMII Transmit Timing



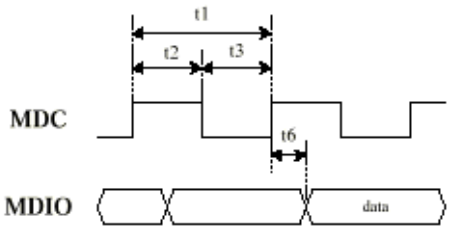
RMII Receive Timing

PHY Management Timing

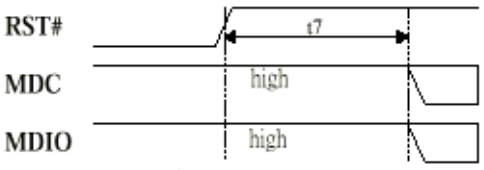
Symbol	Description	Minimum	Typical	Maximum	Units
t1	MDC clock period	-	SYSCK * 32	-	ns
t2	MDC high level width	-	SYSCK * 16	-	ns
t3	MDC low level width	-	SYSCK * 16	-	ns
t4	MDIO to MDC rising setup time (Write Bits)	10	-	-	ns
t5	MDIO to MDC rising hold time (Write Bits)	10	-	-	ns
t6	MDC to MDIO delay (Read Bits)	-	-	20	ns
t7	MDC/MDIO actives from RST# deasserted	-	94.377	-	ms



MDIO Write Timing



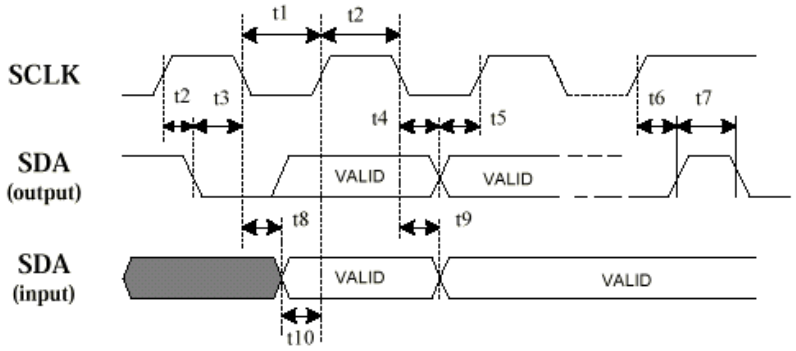
MDIO Read Timing



MDC/MDIO Reset Timing

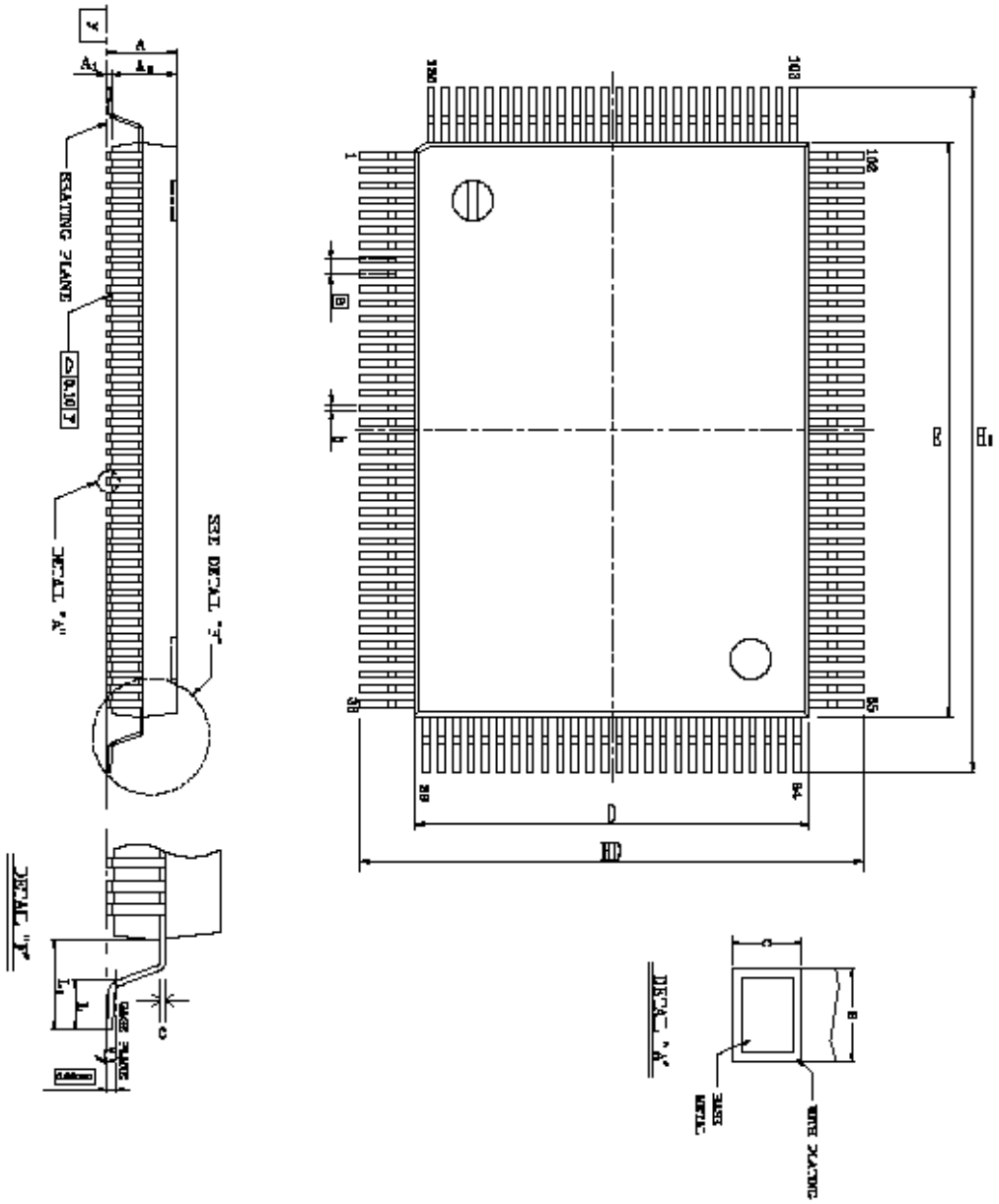
Serial EEPROM 24LC02 Timing

Symbol	Description	Minimum	Typical	Maximum	Units
fclock (EESCK)	Clock frequency , SCLK	-	-	66	kHZ
t1	Clock pulse period	23	-	-	us
t2	Delay time, form SCLK rising to SDA falling	5	-	-	us
t3	Delay time, form SDA falling to SCLK falling	5	-	-	us
t4	Delay time, form SCLK falling to SDA changing	0	-	-	us
t5	Delay time, form SDA valid output to SCLK rising	0	-	-	us
t6	Stop Set-up time	5	-	-	us
t7	Time the bus must is free before a new transmission starting	5	-	-	us
t8	Delay time, form SCLK falling to SDA valid	0	-	-	us
t9	Delay time, form SCLK falling to SDA changing	0	-	-	us
t10	Delay time, from SDA valid input to SCLK rising	10	-	-	us



EEPROM Interface Timing

IC package



Symbol	Dimension in inch			Dimension in mm		
	Min	Type	Max	Min	Type	Max
A			0.134			3.40
A1	0.004	0.010	0.036	0.10	**0.25**	0.91
A2	0.102	0.112	0.122	2.60	**2.85**	3.10
b	0.005	0.009	0.013	0.12	**0.22**	0.32
c	0.002	0.006	0.010	0.05	**0.15**	0.25
D	0.541	0.551	0.561	13.75	**14.00**	14.25
E	0.778	0.787	0.797	19.75	**20.00**	20.25
e	0.010	0.020	0.030	0.25	**0.5**	0.75
HD	0.665	0.677	0.689	16.90	**17.20**	17.50
HE	0.902	0.913	0.925	22.90	**23.20**	23.50
L	0.027	0.035	0.043	0.68	**0.88**	1.08
L1	0.053	0.063	0.073	1.35	**1.60**	1.85
y			0.004			0.10

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar rotrusion/intrusion.
3. Controlling dimension : Millimeter
4. General appearance spec. should be based on final visual inspection spec.