Sixteen-port 10/100 Switch

The T71L6816A is a sixteen-port 10/100Mbps dual speed ethernet switch integrated with a built-in 2K entries of address table and supports a 4Mb external SSRAM. T71L6816A is also a high performance Fast-Ethernet switch with fully compliance with the IEEE802.3, 802.3u and 802.3x specifications. The T71L6816A can be implemented with external PHY chips and 4Mb pipe-line SSRAM. By default, it is targeted for applications to the stand-alone switch for low-cost SOHO and small enterprise market.

Features

- Support sixteen 10/100 Ethernet ports with RMII interface.
- External memory needed for 4Mb pipe-line SSRAM.
- Incorporating with private output buffering scheme to prevent HOL (head of line) blocking.
- Each port support priority-based queues with 4 levels and 802.1p QoS.
- Wire-speed store-and-forward switching with low latency.
- Automatic address learning with filtering of local frames or illegal frames.
- Embedded 2K entries of address look-up table.
- Support full/half duplex operations.
- Support auto-negotiation via MDIO to detect speed and duplex status.
- Serial EEPROM interface for auto-configuration for features.
- Support IEEE802.3x flow control for full-duplex operation.
- Support Back-Pressure flow control for half-duplex operation.
- Support port-trunking mode to aggregate the bandwidth to provide the functions of load-sharing and link backup.
- Support broadcast storm control scheme.
- Maximum 3 port-based VLAN groups can be defined by user.
- Support port-based port monitoring/snooping defined by user.
- Only one 50Mhz oscillator needed.
- 208-pin BGA, 3.3V with .18 µm CMOS technology.

1. General Description

The T71L6816A is a highly integrated sixteen-port 10Base-T/100Base-TX Ethernet switch with RMII interface and is implemented in 0.18μm CMOS technology. The T71L6816A supports a wide variety of switch features and provides flexible configurations at maximum performance levels with lowest number of components.

This switch supports store-and-forward switching scheme with an external memory buffer for incoming/outgoing packets and a built-in memory for address table. The T71L6816A use the page-based memory architecture to fully utilize the packet buffer so that it can identify up to 2048 different MAC addresses and enable the filtering and forwarding of packets range from 64 bytes to 1522 bytes at the non-blocking wire speed, 148800 packets/sec at 64 bytes/packet.

The function modules integrated in T71L6816A include sixteen full-duplex media access controller(MAC) with RMII interface to PHYs, one address resolution logic(ARL), one flow control unit and one buffer management unit(BMU).

The T71L6816A supports IEEE 802.3x flow control in full-duplex mode and back-pressure control in half-duplex mode. Also, the T71L6816A is fully compatible to the ability for auto-negotiation with its link partner by periodically polling the status of PHYs.

The T71L6816A provides the port-based VLAN group function to help users to isolate traffic segment by segment for the sake of security and bandwidth saving. Maximum three VLANs can be divide by users and it is suitable for application in small office or home.

The T71L6816A also supports the port-based trunking applications. With trunking enabled, it is possible to aggregate up to four full-duplex links to form a single channel with 400Mbit/s data rate and to provide the load sharing effect.

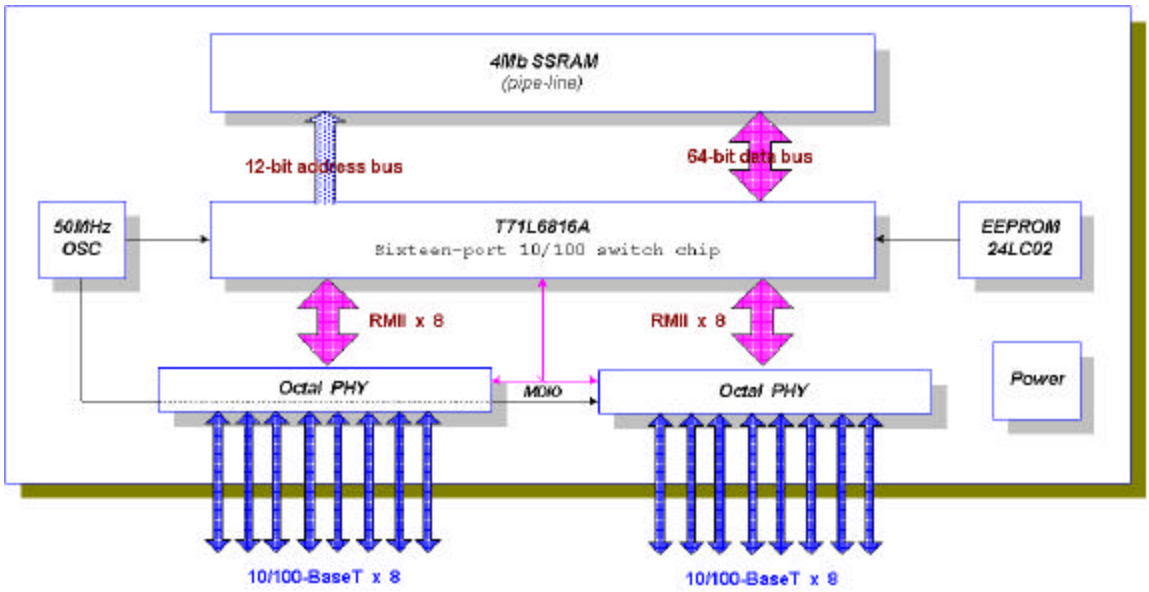
The T71L6816A will also support the QoS requirement for some networks. With QoS enabled in networks which is compatible to VLAN QoS, the T71L6816A will put incoming packets into different priority output queues by checking the QoS field in their VLAN header. If the user's network do not support VLAN QoS, the T71L6816A still offers an alternative way

to give different priority to incoming traffic from pre-defined source port.

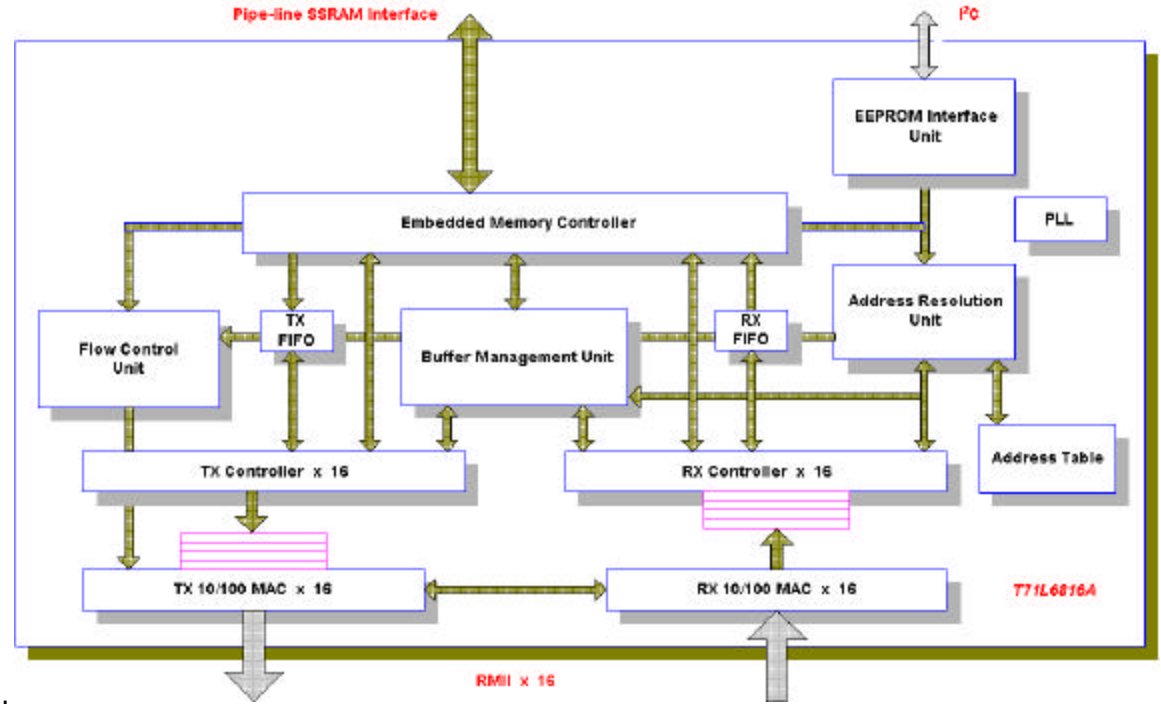
Additionally, the T71L6816A provides the configuration ability through external EEPROM to enable or disable functionality flexibly. However, the T71L6816A can operate well without any external setting by default.

2. Architecture

2.1 System Diagram



2.2 Block Diagram



3. Functional Description

3.1 Reset

The T71L6816A will determine some function features chosen by the content of 24LC02 serial EEPROM which was loaded after power on reset. Also, the T71L6816A will write the abilities derived from 24LC02 or internal default value if 24LC02 is not present to connected PHY management registers via MDC/MDIO.

3.2 RMII Interface

The T71L6816A provides the low pin count RMII (Reduced Media Independent Interface) interface capable of supporting 10/100 Mbps data rates between PHY and T71L6816A. A single clock, 50MHz, sourced from an external clock input is needed for receive(RX) and transmit(TX) to provide an independent 2-bit wide (di-bit) transmit and receive data paths. In the case of the REFCLK is 10 times the data rate, namely, 100Mbps mode, each data di-bit must be output on TXD[1:0] and input on RXD[1:0] for ten successive REFCLK cycles.

RMII specification signals are listed below:

Signal Name	Direction (with respect to PHY)	Direction (with respect to T71L6816A)	Use
REFCLK	*Input*	*Input*	*Synchronous clock reference for Rx, Tx and control interface*
CRSDV	*Output*	*Input*	*Carrier sense / receive data valid*
RXD[1:0]	*Output*	*Input*	*Receive data*
TXEN **TXD[1:0]**	*Input* *Input*	*Output* *Output*	*Transmit enable* *Transmit data*

3.3 Data Reception

The port will enter the receive-state when the CRSDV signal in the RMII interface is asserted and then the RMII presents the received data in two-bit(di-bit) format that are synchronous to the RMII reference clock, namely, REFCLK. The T71L6816A will then try to identify the occurrence of the SFD(Start Frame Delimiter) pattern "10101011". Once the SFD was identified, all preamble data prior to SFD will be discarded and the frame data will be forwarded and stored in the buffer of the switch.

3.4 Illegal Frames

The T71L6816A will check the errors of incoming frames and discard all illegal packets if any non-recovered error found. The kinds of errors include FCS error, illegal packet length, symbol error and dribble error. However, for preamble error, the T71L6816A will try to identify the SFD even if the preamble error happened and the packet will be dropped only if the T71L6808A can not well identify the incoming packet.

3.4.1 FCS Error

The T71L6816A will generate the 4 bytes of CRC checksum through every incoming packets and compare the checksum with the FCS field to identify if the packet is corrupt or not. If it is found that the CRC checksum is not matched with the FCS field, the T71L6816A will discard this packet due to something wrong on data transmission.

3.4.2 Alignment Error

The T71L6816A will discard the packets with the frame length is of non-integer in octet unit. Exactly, the kind of such packet usually results in CRC checksum error and is called as alignment error.

3.4.3 Dribble Error

Dribble error is that the packets contains some extra bit after four bytes of FCS. The T71L6816A will drop those packets because those packets are usually similar to the FCS error.

3.4.4 Length of Frames

The T71L6816A can recognize the legal frame with length ranges from 64 bytes to 1522 bytes including four bytes of FCS. Any packet with length smaller than 64 bytes or larger than 1522 bytes will be discarded.

3.5 Frame Forwarding

The first six bytes(DA) and the second six bytes(SA) of every incoming packet received by T71L6816A will be retrieved and passed to Address Resolution Logic unit(ARL). The ARL will use the SA to update the address table and use the DA to determine which destination port the packet should be forwarded to by address table lookup.

3.5.1 Unicast Forwarding

If the first bit of the DA is "0", the packet is regarded as an unicast packet and the ARL will use the DA as an key to search for a matched entry in address table by either hashing algorithm or direct mapping method chosen by the configuration from EEPROM.

If an matched entry is found, the ARL will return a destination port number. If the port number returned is within the same VLAN group but not the same of incoming port, the packet will be forwarded to the destination port, otherwise it will be discarded. Also, if the trunking scheme is enabled and the returned port is defined as a member of trunking group, the real output port could be any one of the trunking ports and is dependent on trunking scheme currently used.

If ARL can't find any entry matched in address table, the packet will be regarded as an broadcast packet and forwarded to other ports that belong to the same VLAN group of the incoming port.

3.5.2 Multicast Forwarding

If the first bit of the DA is "1", the packet is regarded as a multicast packet. The packet will be forwarded to other ports that belong to the same VLAN group of the incoming port.

3.6 Data Transmission

According to the standard of IEEE 802.3, the T71L6816A will transmit all output packets with a guaranteed minimum IPG(Inter Packet/Frame Gap) of 96BT(bit time) even if the incoming packets have an IPG less than 96BT. However, the T71L6816A will drop excess incoming packets which input continuously with smaller IPG than 96BT due to run out of packet buffer and result in the packet loss. The 96BT should be 96ns for 10Mbps and 960ns for 100Mbps.

During the transmit process, the T71L6816A will read the packet data from SSRAM and forward it to the PHY device of the destination port in di-bit format. Also, the T71L6816A will generate seven bytes of preamble(10101010) and SFD(10101011) prior to the frame data followed by four bytes of FCS generated by T71L6816A automatically.

3.7 Address

3.7.1 Address Learning

The T71L6816A has a on-chip address table with 2K entries to map the MAC address to port-ID for the operation of packet forwarding engine. The T71L6816A use either hash algorithm or direct mapping to locate every entry and each entry contains the information about incoming port number, partial MAC address and age timer.

The T71L6816A learns the MAC address of attached network devices by checking the source MAC address(SA) of all incoming packets and acts as follows: If the SA is an unicast address and can't be found in address table, the T71L6816A will allocate an entry for this address after this packet has been received with no error detected. If the SA was found in address table, the T71L6806A will update the aging value of the corresponding entry to zero.

The T71L6816A will disable the learning process while the incoming packet is a PAUSE command defined by IEEE 802.3x.

3.7.2 Address Aging

If the "AgeEn" option configured in EEPROM is set, the T71L6816A will periodically check every entry in address table and mark the entry as invalid if its aging timer is over 300 seconds. Once a entry is marked as invalid, this entry no longer be used for address lookup until it is remarked as valid for new address.

3.8 Broadcast Storm Control

In general, the T71L6816A will forward the broadcast packets to other ports. It's obviously broadcast packets will use switch resources(bandwidth and available transmit queue) much more than normal packets. In extreme case of unstable network with something wrong, it may produce massive broadcast packets from one mal-functional device and results in the crash of whole network, that is so-called broadcast storm.

If the "BRDCTRL" option configured in EEPROM is set, the T71L6816A provide a scheme to prevent the broadcast storm by temporarily discarding the broadcast/multicast packets if the number of those kind of packets exceeds the internal threshold.

3.9 Back-off Algorithm

For every port that operates in half-duplex mode, the T71L6816A implements the truncated exponential back-off algorithm compliant to IEEE 802.3 standard and the collision counter based on per port will be restarted after every 16 consecutive collision. That is, the T71L6816A will guarantee no packet loss if the times of consecutive collision is less than 16.

3.10 Buffer Management

The T71L6816A provides an interface to the external 64x64K(4Mb) SSRAM which operates in 66MHz pipeline mode as the packet storage buffer. For purpose of efficiency, the T71L6816A divide the 4Mb space to 1K pages and each page contains 512 bytes, therefore, maximum 3 pages or minimum 1 page is needed for every Ethernet packets.

3.11 Head-of-Line Blocking

One common requirement for Ethernet switch is to prevent the Head-of-Blocking problem. In other words, in case of some ports under heavy traffic or congestion, the switch must keep all other ports function well and don't be affected by those congested ports.

The T71L6816A provide a alternative way to achieve above requirement while customer disable the flow control function. Say, the T71L6816A will first check the status of the destination port of incoming packets, the packets will be dropped if the destined port is congested and therefore the T71L6816A can reserve the finite spaces of the packet buffer for other normal traffic ports.

3.12 Flow Control

3.12.1 Flow Control in Full Duplex Mode

The T71L6816A support the IEEE 802.3x flow control scheme in full duplex mode. The IEEE 802.3 define the format of pause frame as follow:

By set the "FlowCtrl_En" in EEPROM for any specific port, The T71L6816A will check the DA field of every incoming 64-byte packet from the specific port to see if it is the address "0x0180c2000001" or not. If it is the legal pause frame, the T71L6816A will hold the data forwarding to the specific port for a time period depended on the value defined in the pause timer field, otherwise the pause frame will be dropped if its format is illegal.

Also, if flow control is enabled for one port, the T71L6816A will automatically send out one pause frame with pause timer "0xffff" to that port if the free pages of T71L6816A drop below the low watermark.

3.12.1 Flow Control in Half Duplex Mode

The T71L6816A support the back pressure congestion control scheme in half duplex mode with two different way, force-collision and force-carrier.

By set the "BackPress_En" in EEPROM, the T71L6816A will enable the back-pressure scheme while the free pages of T71L6816A drop below the low watermark. If the internal resources is low, The T71L6816A will force collision on the incoming packet if "BackMode" is set to be '0' and will occupy the carrier signal to stop packets receiving if "BackMode" is set to be '1'.

3.13 Port-based VLAN

Sometimes users want to divide some segments on their network for some reasons such as security or traffic. The T71L6816A provide the port-based VLAN(Virtual LAN) scheme to divide the attached devices into maximum three different segments defined by configuring the EEPROM. Once different VLANs were defined, the T71L6816A will forward the traffic within the same VLAN segment and prevent them from flowing into ports not belong to the same VLAN. So, users can isolate traffics between any two different VLANs but the common port.

The T71L6816A use the VLAN_1/VLAN_2 fields defined in EEPROM to determine the effective VLANs. That is, if any bit is set to '1' in VLAN_1/VLAN_2, the corresponding port is belonging to the VLAN group 1 or 2 and all other ports without inclusion in VLAN_1 or VLAN_2, if exists, will form the third VLAN group. If one port belongs to more than one

VLAN group, it can receive all of the traffic within those VLAN groups.

For example, if we write VLAN_1[15:8] as "0xff", VLAN_1[7:0] as "0x00", VLAN_2[15:8] as "0x0f" and VLAN_2[7:0] as "0xf0", the T71L6816A will recognize that VLAN group 1 contains port 15 to port 8, VLAN group 2 contains port 11 to port 4 and VLAN group 3 contains port 3 to port 0.

3.14 Port-based Trunking

Trunking scheme allows more than two ports to be connected in parallel between two switchs to increase the traffic bandwidth. The T71L6816A supports up to four ports to form the trunking backbone with four different mode to balance traffic load and maximum 400Mbps of data rate is allowed. Also, the T71L6816A supports the link-redirect scheme for trunking so that the T71L6816A can backup the link circuit automatically while one link is down and restore the circuit after the circuit is up.

3.15 Port Monitoring

The T71L6816A provides the simple network monitoring scheme for persons who need to snoop the traffic input from one specific port. By set "SnoopEn" bit in EEPROM, beyond of the normal forwarding, the T71L6816A will make a duplication of any packet input from the specified port defined in SPID and forward this copy to another specific port defined in MPID, i.e., only one pair of snooping/monitoring port can be defined.

3.16 Queue Priority

There are four queues supported by T71L6816A with different priorities for every output port. In general, the T71L6816A will treat all output packets as the same and put them into one queue with lowest priority. However, if any packet which contains the 802.1Q tagging with 3-bit priority value larger than 0 or comes from one port defined as high priority is found, those packets will be put into other three output queues with more higher priorities. The T71L6816A will use weighted round-robin method to serve every output queue for each port that has packets in queues.

3.17 Interface of PHY management

The T71L6816A supports the PHY management through two signal lines, MDC and MDIO. The T71L6816A will write physical abilities to the register 4 and register 5 of connected

PHYs and restart the auto-negotiation process by polling each PHYs with PHY address

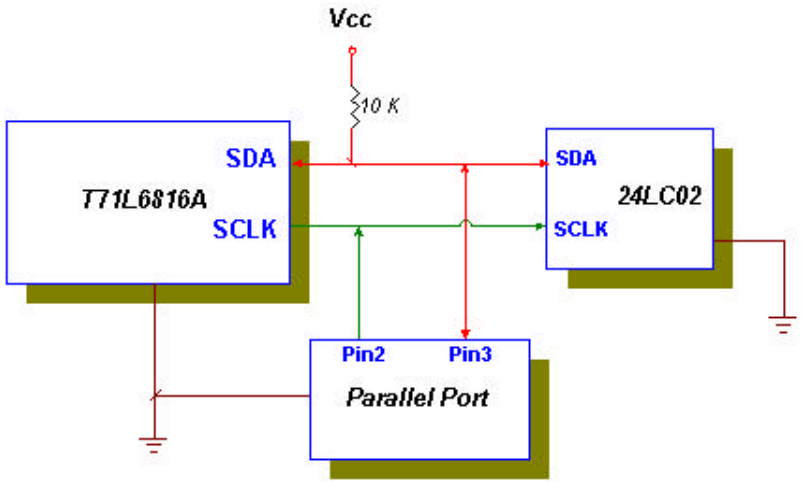
increasing from 01000b to 01111b after power on reset. The polling process will be performing continuously to refresh the link status and the link partner's abilities such as speed, duplex and flow control until power off.

The following table shows the format of MDIO management frames:

Operation	Preamble	ST	OP	PHYaddr	REGaddr	TA	DATA	IDLE
Read	1……1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
Write	1……1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

3.17 Interface of 24LC02

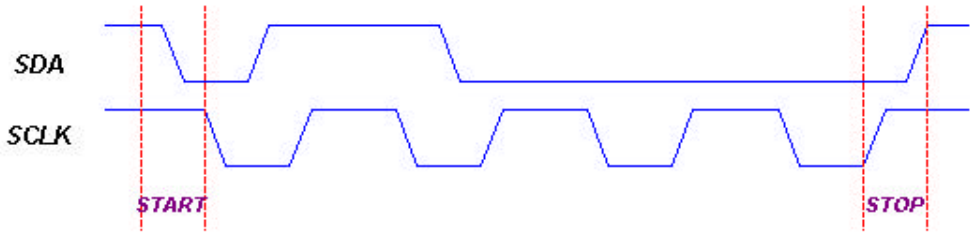
3.17.1 Block Diagram



The 24LC02 is an EEPROM chip providing 2K bits storage space with 2-wire I^2C interface. After power on reset, the T71L6816A will use a sequential read command to load the configuration settings defined by user in the 24LC02 and configure the features from those settings for later normal operation. Once loading completed, the T71L6816A will tri-state the two pins SDA and SCLK to be ready for on-line updating 24LC02 through the parallel port.

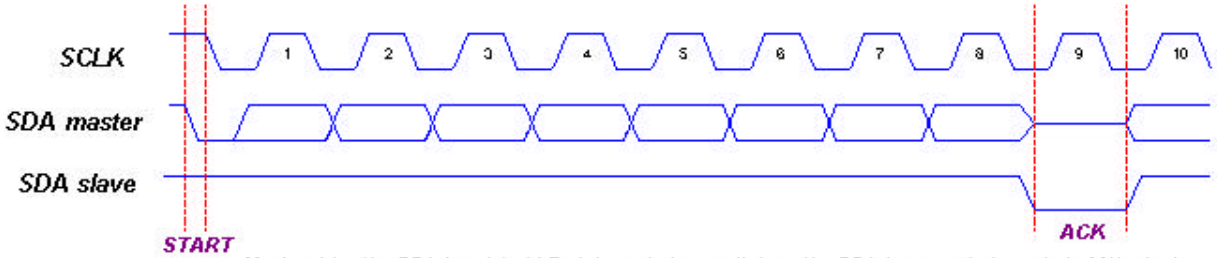
As shown above, the user can run a simple program on WinNT/Win98 to configure the external 24LC02 through the parallel port which is popular in most personal/notebook computer. The whole system can then be reset after the external 24LC02 been reconfigured to adapt for different environments.

3.17.2 Timing

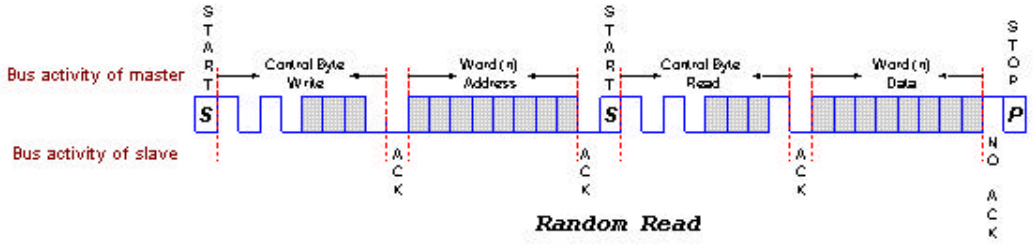


SDA from high to low while SCLK is high

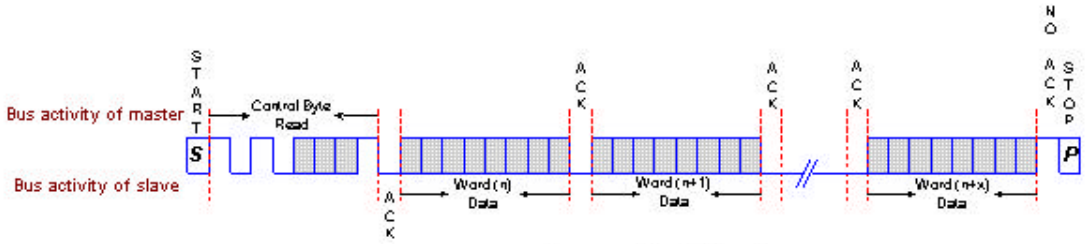
SDA from low to high while SCLK is high



Master drive the SDA bus into hi-Z state and slave pull down the SDA bus on whole period of 9th clock



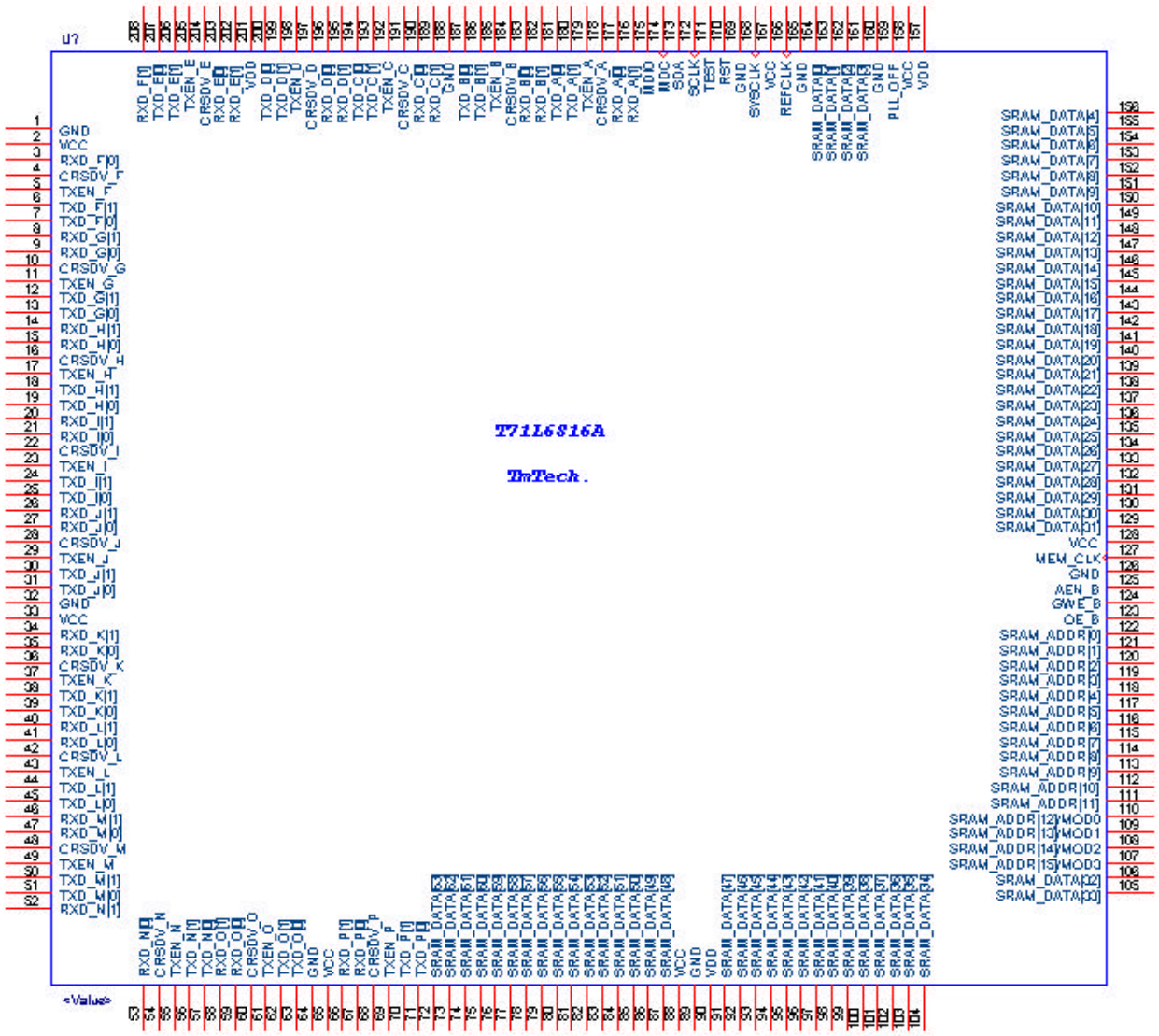
Random Read



Sequential Read

4. Pin Assignment

4.1 Pin Assignment



4.2 Pin Description

Symbol	I/O type	Pin Number	Function
		RMII Interfaces	
REFCLK	I	166	**Reference Clock.** Reference clock with 50MHz to provide the timing reference for CRSDV, RXD[1:0], TXEN and TXD[1:0]
TXD_A[1:0]	O	180, 181	**Transmit Data.** TXD[1:0] must operate synchronously with respect to REFCLK and the TXD[1:0] will be accepted by PHY transmission when TXEN is asserted.
TXD_B[1:0]		186, 187	
TXD_C[1:0]		193, 194	
TXD_D[1:0]		199, 200	
TXD_E[1:0]		206, 207	
TXD_F[1:0]		6, 7	
TXD_G[1:0]		12, 13	
TXD_H[1:0]		18, 19	
TXD_I[1:0]		24, 25	
TXD_J[1:0]		30, 31	
TXD_K[1:0]		38, 39	
TXD_L[1:0]		44, 45	
TXD_M[1:0]		50, 51	
TXD_N[1:0]		56, 57	
TXD_O[1:0]		62, 63	
TXD_P[1:0]		70, 71	
RXD_A[1:0]	I	176, 177	**Receive Data.** RXD[1:0] must operate synchronously with respect to REFCLK and the RXD[1:0] will transfer 2-bit data recovered from PHY to MAC on every REFCLK period while CRSDV is high.
RXD_B[1:0]		182, 183	
RXD_C[1:0]		189, 190	
RXD_D[1:0]		195, 196	
RXD_E[1:0]		202, 203	
RXD_F[1:0]		208, 3	
RXD_G[1:0]		8, 9	
RXD_H[1:0]		14, 15	
RXD_I[1:0]		20, 21	
RXD_J[1:0]		26, 27	
RXD_K[1:0]		34, 35	
RXD_L[1:0]		40, 41	
RXD_M[1:0]		46, 47	
RXD_N[1:0]		52, 53	
RXD_O[1:0]		58, 59	
RXD_P[1:0]		66, 67	

Symbol	I/O type	Pin Number	Function
		RMII Interfaces (cont.)	
TXEN_A ~ TXEN_P	O	179, 185, 192, 198, 205, 5, 11, 17, 23, 29, 37, 43, 49, 55, 61, 69	**Transmit Enable.** TXEN indicates the MAC is presenting 2-bit data on TXD[1:0] for transmission.
CRSDV_A ~ CRSDV_P	I	178, 184, 191, 197, 204, 4, 10, 16, 22, 28, 36, 42, 48, 54, 60, 68	**Carrier Sense / Receive Data Valid.** CRSDV indicates the PHY is presenting 2-bit data on RXD[1:0] for transmission.
		SRAM Interfaces	
MEM_CLK	O	127	**Memory Clock.**
AEN_B	O	125	**Address Enable.**
GWE_B	O	124	**Group Write Enable.**
OE_B	O	123	**Output Enable.**
SRAM_DATA[63:0]	I/O	72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100, 101, 102, 103, 104, 105, 106, 129, 130, 131, 132, 133, 134, 135, 136, 137, 138, 139, 140, 141, 142, 143, 144, 145, 146, 147, 148, 149, 150, 151, 152, 153, 154, 155, 156, 161, 162, 163, 164	**SRAM Data Bus.**

Symbol	I/O type	Pin Number	Function
			SRAM Interfaces (Cont.)
SRAM_ADDR[15:0]	O	107, 108, 109, 110, 111, 112, 113, 114, 115, 116, 117, 118, 119, 120, 121, 122	**SRAM Address Bus.**
			Power Pins
VCC		2, 33, 65, 88, 128, 158, 167	**Power Pins for System.** 3.3V DC power.
GND		1, 32, 64, 89, 126, 160, 165, 169, 188	**Ground Pin.** DC ground.
VDD		90, 157, 201	**Power Pins for Core.** 1.8V DC power.
			Serial EEPROM Interfaces
SCLK	O	172	**Serial Clock.** SCLK is used to synchronize the SDA and to be pulled high internally.
SDA	I/O	173	**Serial Data/Access.** Bi-directional serial data I/O line which is pulled high internally.
			PHY Management Interfaces
MDC	O	174	**PHY Management Interface Clock.** The MDC provides the reference clock for shifting serial data in/out from PHY device on rising edges.
MDIO	I/O	175	**PHY Management Interface Data I/O.** Bi-directional serial data contains information which is read from or written to the PHY devices.
			Test Pins
TEST	I	171	**Test Mode Enable.** For normal use, this pin must be tire to low.
MOD[3:0]	I	107, 108, 109, 110	**Test Mode Select.** For normal use, those pins should be tired to low.
			System Interfaces
RST	I	170	**Reset.** Asynchronous active low reset signal.
SYSCLK	I	168	**System Clock.** 50MHz clock for system.
PLL_OFF	I	159	**Phase-Loop-Lock enable/disable.** High to disable the internal PLL circuit.

5. Reference Design

Please contact our sales for more detailed information.

6. Configuration of Serial EEPROM(24LC02)

6.1 Mapping of Configuration

Bit / Byte	7	6	5	4	3	2	1	0
0	BRDCTRL	HashMode	AgeEn	BackMode	SnoopEn	Reserved	Reserved	Reserved
1	VLAN_1[15:8]							
2	VLAN_1[7:0]							
3	VLAN_2[15:8]							
4	VLAN_2[7:0]							
5	TrunkPort[1:0]		TrunkBase[1:0]		Reserved	Reserved	Reserved	Reserved
6	MPID[3:0]				SPID[3:0]			
7	Port-base setting for port 0							
8	Port-base setting for port 1							
9	Port-base setting for port 2							
10	Port-base setting for port 3							
11	Port-base setting for port 4							
12	Port-base setting for port 5							
13	Port-base setting for port 6							
14	Port-base setting for port 7							
15	Port-base setting for port 8							
16	Port-base setting for port 9							
17	Port-base setting for port A							
18	Port-base setting for port B							
19	Port-base setting for port C							
20	Port-base setting for port D							
21	Port-base setting for port E							
22	Port-base setting for port F							
23	PauseFrameSourceAddress[47:40]							
24	PauseFrameSourceAddress[39:32]							
25	PauseFrameSourceAddress[31:24]							
26	PauseFrameSourceAddress[23:16]							
27	PauseFrameSourceAddress[15: 8]							
28	PauseFrameSourceAddress[7: 0]							
29	PauseFrameOnCRC[31:24]							
30	PauseFrameOnCRC[23:16]							
31	PauseFrameOnCRC[15: 8]							
32	PauseFrameOnCRC[7: 0]							
33	PauseFrameOffCRC[31:24]							
34	PauseFrameOffCRC[23:16]							
35	PauseFrameOffCRC[15: 8]							
36	PauseFrameOffCRC[7: 0]							

6.2 Description of Configuration

BRDCTRL: When 0, the broadcast storm control function is disabled
When 1, the broadcast storm control function is enabled

HashMode: When 0, the address direct mapping algorithm is used
When 1, the address hashing algorithm is used

AgeEn: When 0, the aging-out mechanism for address table is disable
When 1, the aging-out mechanism for address table is enabled

BackMode: When 0, chip generates jam sequence to any regulated port that start to receive a frame while the switch becoming congested
When 1, chip generates carrier signal on any regulated port that start to receive a frame while the switch becoming congested

SnoopEn: When 0, the snooping function is disabled
When 1, the snooping function is enabled
(also refers to MPID/SPID)

TrunkPort[1:0]: When 00, no trunking
When 01, port0 and port1 are trunking ports
When 10, port0, port1 and port2 are trunking ports
When 11, port0, port1, port2 and port3 are trunking ports

TrunkBase[1:0]: When 00, based on (DA xor SA)
When 01, based on DA only
When 10, based on SA only
When 11, based on port

MPID[3:0]: Port ID of port used to snoop other port snooped

SPID[3:0]: Port ID of port to be snooped

VLAN_1[15:0]: Port mapping of ports belong to VLAN group 1

VLAN_2[15:0]: Port mapping of ports belong to VLAN group 2

Port-base setting format

Priority[1:0]	802_En	SpeedMode	DuplexMode	MDIO_En	FlowCtrl_En	BackPress_En

Priority[1:0]: Port-base priority level, the '11' means highest level and '00' means lowest level

802_En: IEEE802.1p format, '1' means enable and '0' means disable

SpeedMode: Speed mode, '1' for 100Mb and '0' for 10Mb

DuplexMode: Duplex mode, '1' for full-duplex and '0' for half-duplex

MDIO_En: *Auto-negoiation from MDIO, '1' means enable and '0' means disable*

FlowCtrl_En: *Flow control, '1' means enable and '0' means disable*

BackPress_En: *Back-pressure mechanism, '1' means enable and '0' means disable*

7. Temperature Limit Ratings

unit : C

Parameter	Min.	Max.
Storage temperature	-55	+125
Operating temperature	0	70

8. DC Characteristics

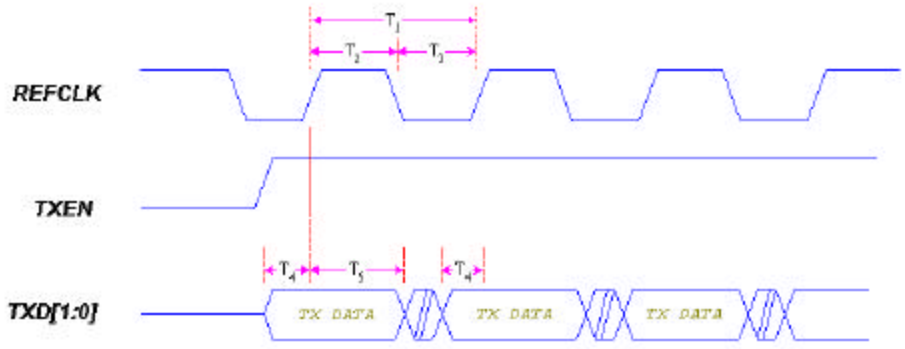
Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
V_{OH}	Output High Level Voltage	I_{OH} = -8mA	0.9*V_{CC}		V_{CC}	V
V_{OL}	Output Low Level Voltage	I_{OL} = 8mA			0.1*V_{CC}	V
V_{IH}	Input High Level Voltage		0.5*V_{CC}		V_{CC}+0.5	V
V_{IL}	Input Low Level Voltage		-0.5		0.3*V_{CC}	V
I_{INPUT}	Input Current	V_{IN} = V_{CC}	-1.0		1.0	uA
I_{OZ}	Output Leakage Current in Tri-State	V_{IN} = V_{CC}	-1.0		1.0	uA
I_{CC}	Average Operating Supply Current	I_{OUT} = 0mA		160	180	mA

9. AC Characteristics

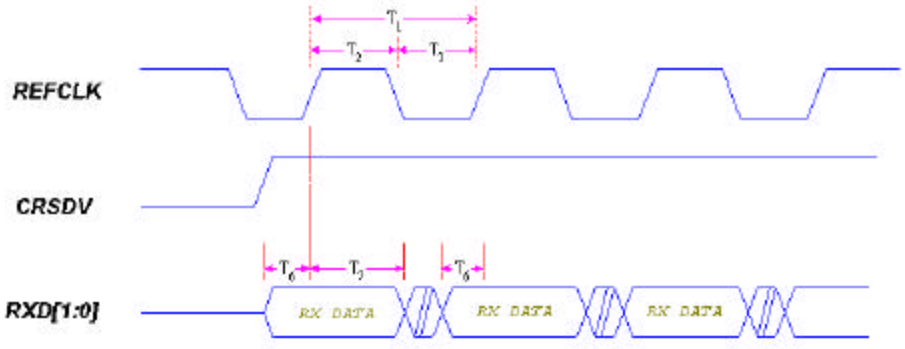
9.1 RMII Timing

unit : ns

Symbol	Description	Min.	Typ.	Max.
T_1	Reference clock period	-	20	-
T_2	Reference clock high level period	-	10	-
T_3	Reference clock low level period	-	10	-
T_4	setup time for TXEN and TXD[1:0]	4	-	-
T_5	hold time for TXD[1:0]	2	-	-
T_6	setup time for CRSDV and RXD[1:0]	4	-	-
T_7	hold time for RXD[1:0]	2	-	-



RMII Transmit Timing

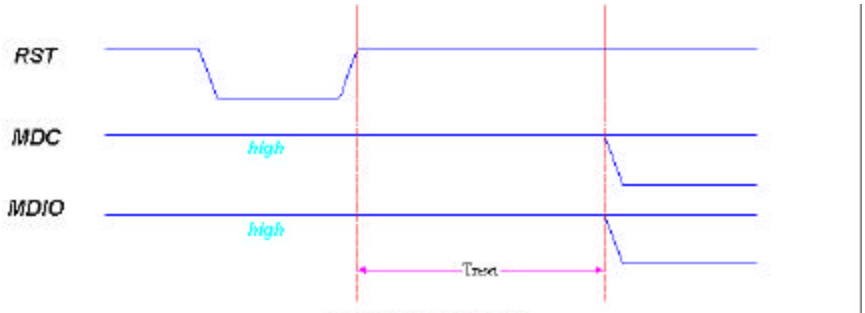


RMII Receive Timing

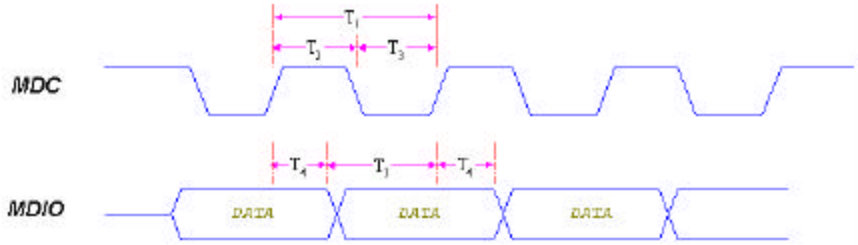
9.3 PHY Management Timing

unit : ns

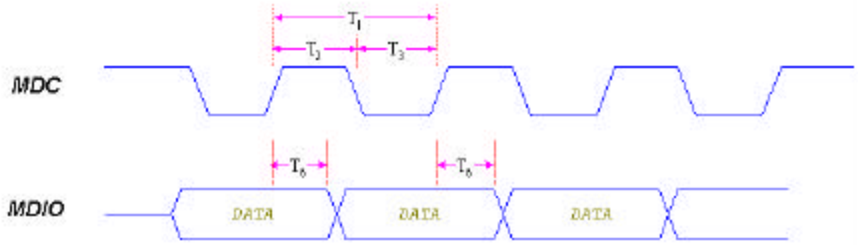
Symbol	Description	Min.	Typ.	Max.
T_1	MDC clock period	-	SYSCLK*32	-
T_2	MDC clock high level period	-	SYSCLK*16	-
T_3	MDC clock low level period	-	SYSCLK*16	-
T_4	hold time for MDIO on writing	10	-	-
T_5	setup time for MDIO on writting	10	-	-
T_6	hold time for MDIO on reading	-	-	20
T_{reset}	waiting time required after reset	-	-	-



EEPROM Reset Timing



EEPROM Write Timing



EEPROM Read Timing