Data Sheet
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microelectronics group

Lucent Technologies
Bell Labs Innovations

# T7274B Quad Differential Line Driver

## Features

- Four line drivers per package
- CMOS level inputs
- Complementary outputs from each line driver
- 25 mA drive capability
- High output drive for 100 Ω, 110 Ω, and 150 Ω balanced lines
- 2.0 ns minimum (0 to +85 °C), 1 ns minimum (−40 °C to +85 °C), and 4.75 ns maximum propagation delays
- 0.1 ns typical output skew, low pulse-width distortion
- 7 ns minimum input pulse width
- 140 Mbits/s data rate at 50% duty cycle
- Single 5 V supply
- Low-power CMOS technology
- −40 °C to +85 °C operating temperature available

## Description

The T7274B Quad Differential Line Driver integrated circuit is a single-input-to-balanced-output converter that drives digital signals over balanced differential transmission lines. The input requires typical CMOS signals. The output has typical CMOS voltage swings and can drive 100 Ω, 110 Ω, and 150 Ω twisted-pair lines through a resistor attenuation network.

This CMOS device is similar to the general-trade 26LS31 device; however, it has decreased power consumption and generates lower levels of electromagnetic interference (EMI).

The T7274B line driver is compatible with many line receivers, including the AT&T T7275C and 41LF devices, and the general-trade 26LS32 device. The quad differential line driver is available in a 16-pin, plastic DIP or in a 16-pin, plastic SOJ package for surface mounting.

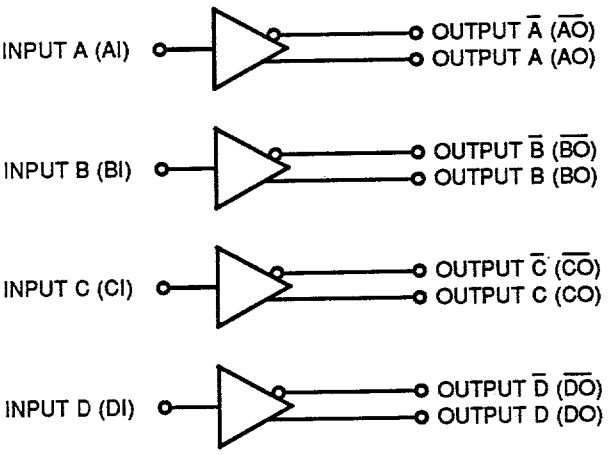



**Figure 1. Block Diagram**

## Pin Information

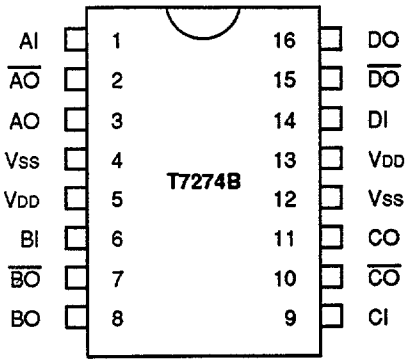



**Figure 2. Pin Diagram**

**Table 1. Pin Descriptions**

| Pin | Symbol | Type | Name/Function |
|---|---|---|---|
| 1 | AI | I | A-Line Driver Input. |
| 2 | $\overline{AO}$ | O | Inverted A-Line Driver Output. |
| 3 | AO | O | A-Line Driver Output. |
| 4 | VSS | — | Ground Pin. |
| 5 | VDD | — | 5 V Supply Pin. |
| 6 | BI | I | B-Line Driver Input. |
| 7 | $\overline{BO}$ | O | Inverted B-Line Driver Output. |
| 8 | BO | O | B-Line Driver Output. |
| 9 | CI | I | C-Line Driver Input. |
| 10 | $\overline{CO}$ | O | Inverted C-Line Driver Output. |
| 11 | CO | O | C-Line Driver Output. |
| 12 | VSS | — | Ground Pin. |
| 13 | VDD | — | 5 V Supply Pin. |
| 14 | DI | I | D-Line Driver Input. |
| 15 | $\overline{DO}$ | O | Inverted D-Line Driver Output. |
| 16 | DO | O | D-Line Driver Output. |

## Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability. External leads can be bonded or soldered safely at temperatures up to 300 ° C.

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Power Supply Voltage | $V_{DD}$ | — | 7.0 | V |
| Ambient Operating Temperature Range | $T_A$ | −40 | 85 | ° C |
| Storage Temperature Range | $T_{stg}$ | −40 | 125 | ° C |
| Power Dissipation | $P_{dis}$ | — | 500 | mW |

## Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. AT&T employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. No industry-wide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and therefore can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using these circuit parameters.

**Table 2. ESD Threshold Voltage**

| Human-Body Model ESD Threshold | |
|---|---|
| Device | Voltage |
| T7274B | >2000 V |

## Typical Application

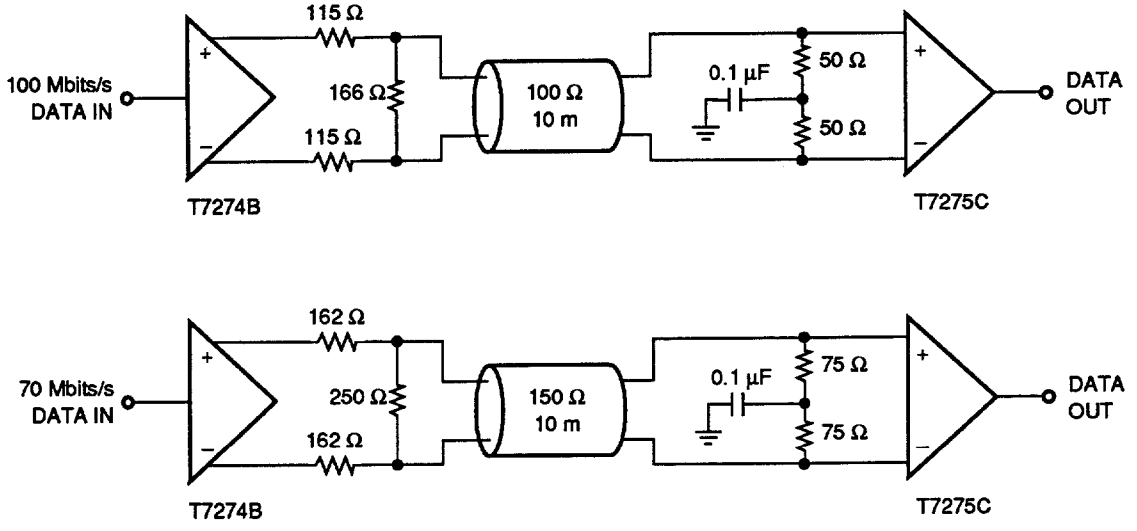



**Figure 3. T7274B and T7275C in 100 Ω and 150 Ω Systems**

## Electrical Characteristics

$T_A$ = −40 ° C to +85 ° C, or 0 ° C to 85 ° C (see the Ordering Information section), $V_{DD}$ = 5.0 V ± 0.25 V

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltages: | | | | | |
| Low, $I_{OL}$ = 12.5 mA | $V_{OL}$ | — | — | 0.5 | V |
| Low, $I_{OL}$ = 25 mA | $V_{OL}$ | — | — | 1.0 | V |
| High, $I_{OH}$ = −12.5 mA | $V_{OH}$ | 4.25 | — | — | V |
| High, $I_{OH}$ = −25 mA | $V_{OH}$ | 3.75 | — | — | V |
| Output Impedance | — | — | 20 | 40 | Ω |
| Input Voltages:* | | | | | |
| Low | $V_{IL}$ | −0.5 | — | 1.0 | V |
| High | $V_{IH}$ | 3.75 | — | $V_{DD}$ + 0.5 | V |
| Threshold | $V_{TH}$ | — | $V_{DD}/2$ | — | V |
| Input Currents:† | | | | | |
| Low, $V_{IN}$ = 0.5 V | $I_{IL}$ | — | 5 | 10 | μA |
| High, $V_{IN}$ = $V_{DD}$ | $I_{IH}$ | — | 50 | 100 | μA |
| Power Supply Current: | | | | | |
| dc Conditions‡ | $I_{DD}$ | — | 0.25 | 0.5 | mA |
| 100 Mbits/s (including load in Figure 4), Data = . . .1010. . . | $I_{DD}$ | — | 75 | 80 | mA |
| Power Dissipation Capacitance per Channel | $C_{PD}$ | — | 44.0 | — | pF |
| Input Capacitance | $C_I$ | — | 5.0 | — | pF |

* Input rise and fall times (10% to 90%) of less than 4 ns are necessary to meet maximum propagation delay, pulse-width distortion, and skew specifications.
† Each input typically has 100 kΩ to Vss. Thus, a no-connect input is pulled low.
‡ Input voltage equals $V_{DD}$ or GND.

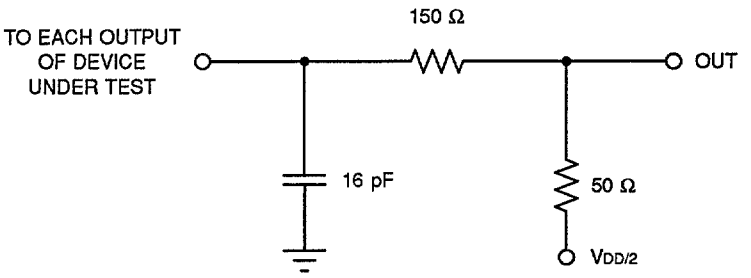
## Timing Characteristics

$T_A$ = −40 ° C to +85 ° C, for T7274B-PL/EL, (except as specified) 0 ° C to 85 ° C for T7274B-PE/EE, $V_{DD}$ = 5.0 V ± 0.25 V, Figure 4 test circuit connected to output. Characteristics in this table apply to Figures 5 and 6. Input rise and fall times (10% to 90%) of less than 4 ns are necessary to meet maximum propagation delay, pulse-width distortion, and skew specifications.

| Symbol | Parameter | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|---|
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay, Input to Output:<br>For All Outputs | 2.0 | 3.0 | 4.75 | ns | 0 ° C to 85 ° C |
| $t_{PLH}$<br>$t_{PHL}$ | For All Outputs | 1.0 | 3.0 | 4.75 | ns | −40 ° C to +85 ° C |
| $t_{SKEW}$ | Difference Between Propagation Delays<br>$\lvert t_{PHL} - t_{PLH} \rvert$ | — | 100 | 300 | ps | — |
| $t_{PWD}$ | Pulse-width Distortion $\lvert t_{IN} - t_{OUT} \rvert$ | — | 200 | 500 | ps | — |
| $t_R$, $t_F$ | Rise and Fall Time (10% to 90%) | — | 1.5 | 3.0 | ns | — |
| $t_{IN}$ | Input Pulse Width | 7 | — | — | ns | — |

## Timing Characteristics (continued)

### Timing Diagrams




Note: See Figure 7 for variations in propagation delay with capacitance.

**Figure 4. Timing Test Circuit**

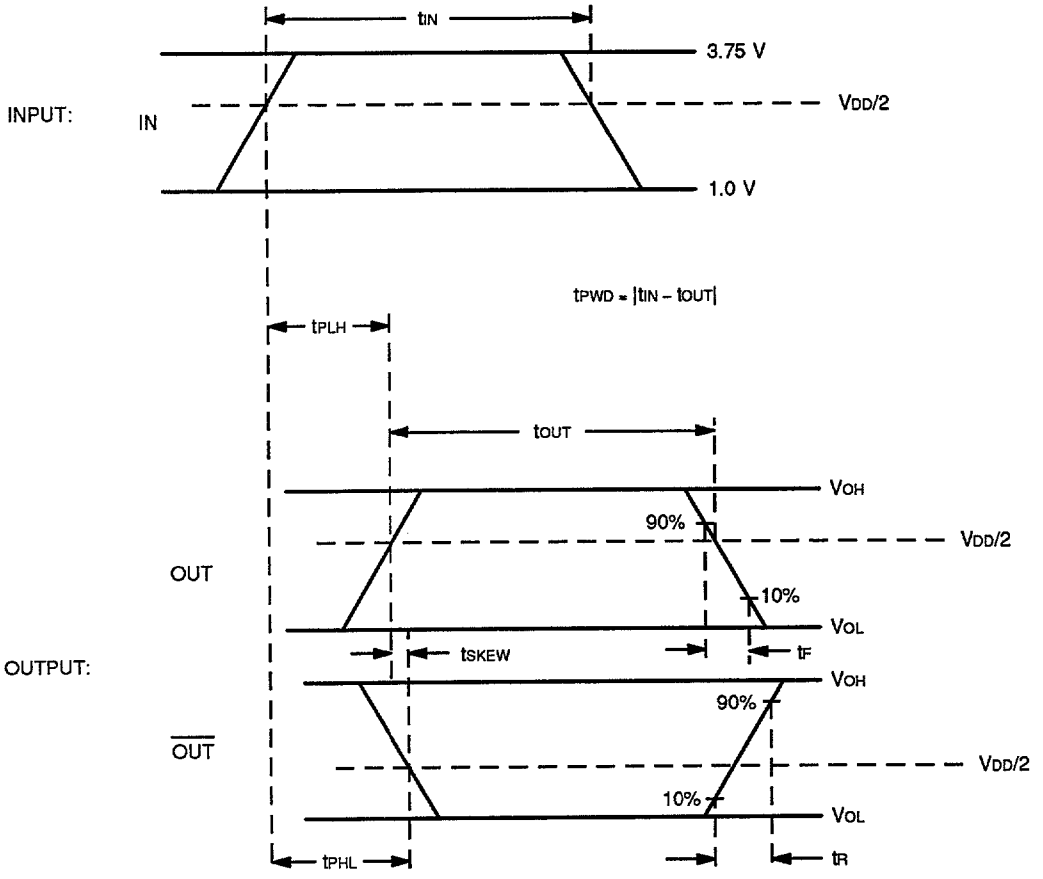



**Figure 5. Timing Waveforms, Positive Input Pulse**

## Timing Characteristics (continued)

### Timing Diagrams (continued)

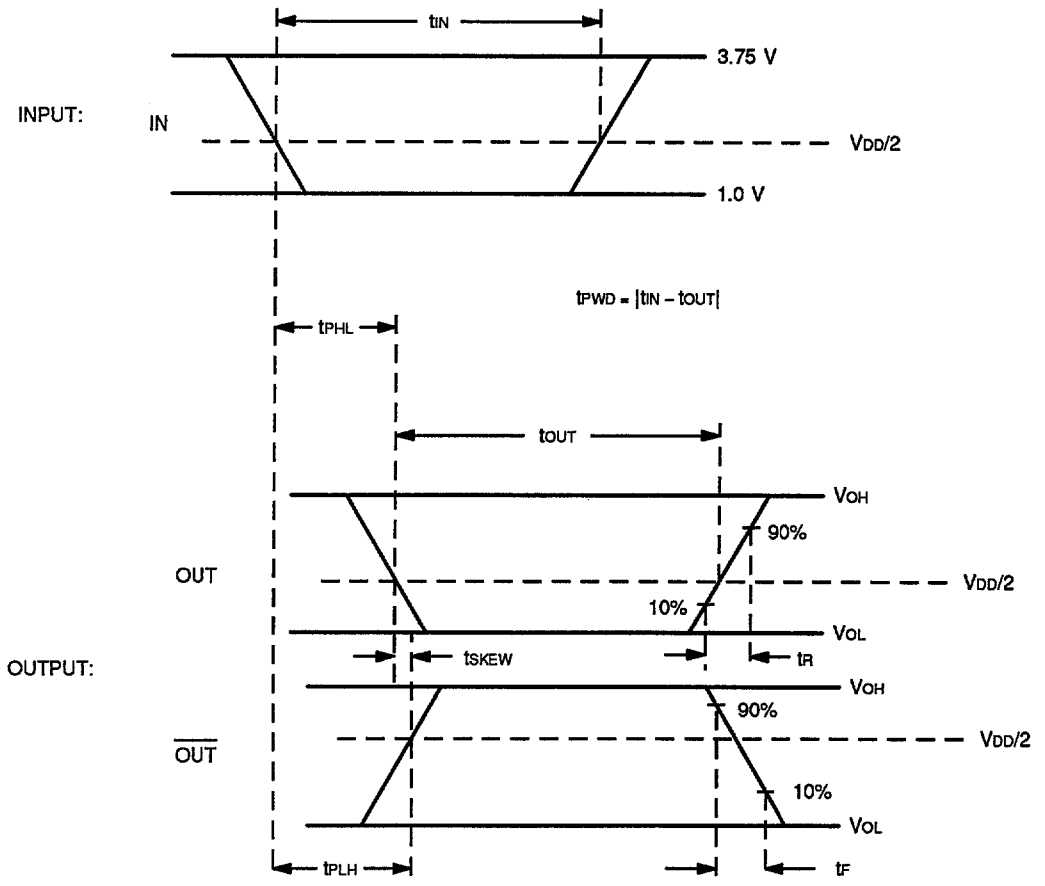



**Figure 6. Timing Waveforms, Negative Input Pulse**

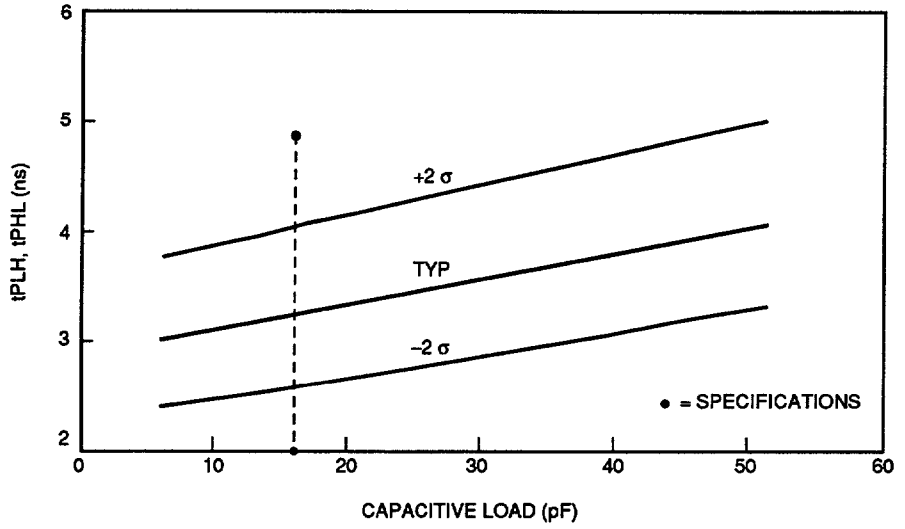
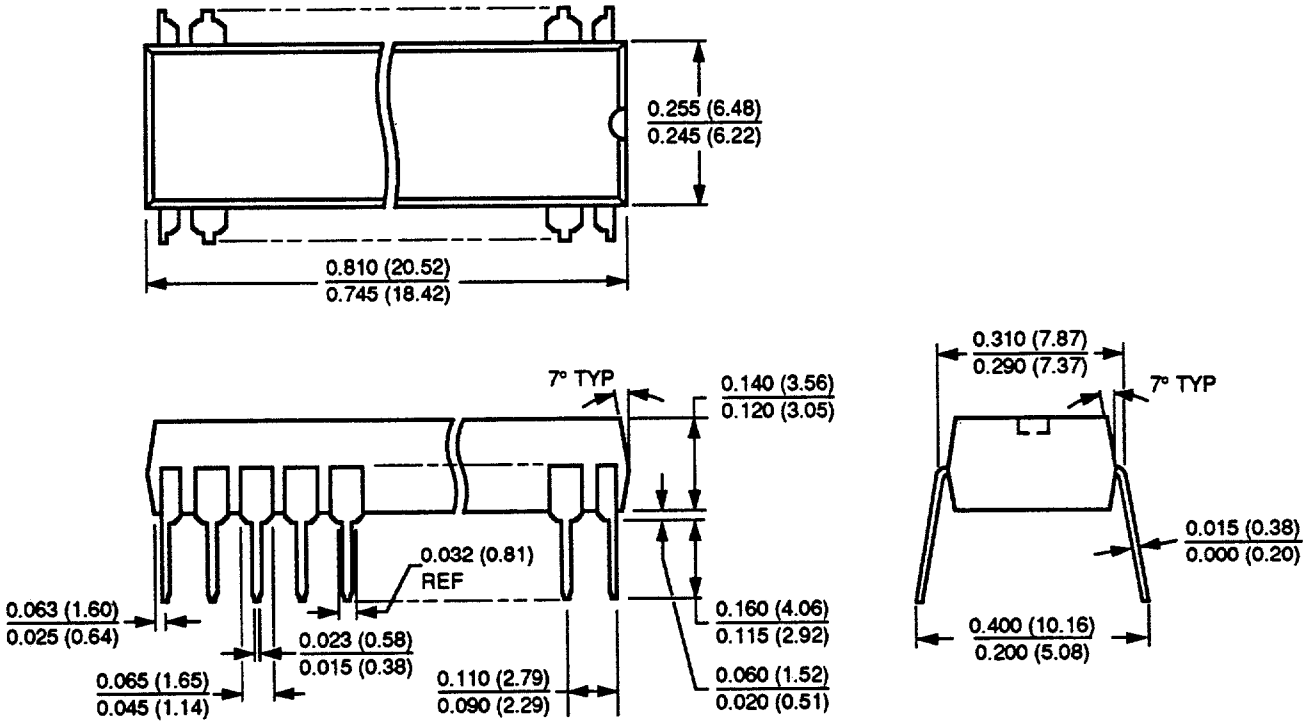



**Figure 7. Propagation Delay vs. Loading Capacitance**

# Outline Diagrams

## 16-Pin, Plastic DIP

Dimensions are in inches and (millimeters).



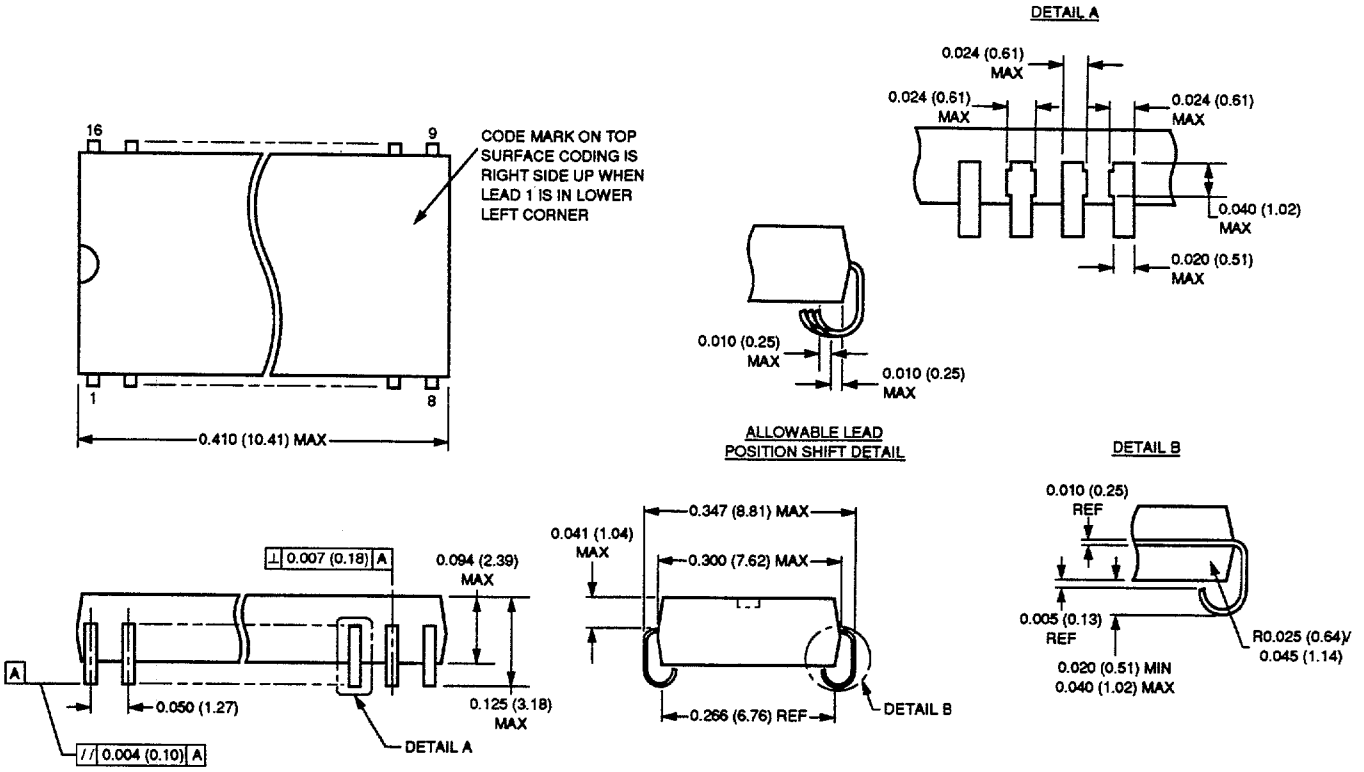

Notes:
Meets JEDEC standards.

Index mark may be semicircular notch or circular dimple located in index area.

## Outline Diagrams (continued)

### 16-Pin, Plastic SOJ, Surface Mounting

Dimensions are in inches and (millimeters).




## Ordering Information

| Device Code | Package | Temperature | Comcode |
|---|---|---|---|
| T7274B-PE | 16-Pin, Plastic DIP | 0 ° C to 85 ° C | 106279722 |
| T7274B-EE | 16-Pin, Plastic SOJ | 0 ° C to 85 ° C | 106279706 |
| T7274B-PL | 16-Pin, Plastic DIP | −40 ° C to +85 ° C | 106601339 |
| T7274B-EL | 16-Pin, Plastic SOJ | −40 ° C to +85 ° C | 106279946 |

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