Data Sheet
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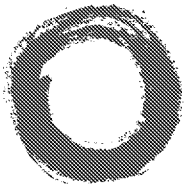
Lucent Technologies
Bell Labs Innovations



T7289A DS1 Line Interface

Features

- Fully integrated DS1 line interface
- Intended for use in systems that must comply with PUB 43802, CB119, TR-TSY-000170, and TR-TSY-000499 (Category I equipment)
- Low power dissipation
- On-chip transmit equalization
- Monolithic clock recovery
- High jitter accommodation
- Excellent transmit template performance
- Single-rail/dual-rail interface
- Pin-selectable B8ZS encoder and decoder (during single-rail mode only)
- Loopback modes for fault isolation
- Multiple link-status and alarm features
- Minimal external circuitry required

Description

The Lucent Technologies Microelectronics Group T7289A DS1 Line Interface is an integrated circuit that provides a line interface between the DS1 cross connect (DSX) and terminal equipment circuits for cable distances of up to 655 ft. for 22-gauge, plastic, insulated cable (PIC). The T7289A device performs receive-pulse regeneration, timing recovery, and transmit-pulse shaping and equalization functions. The device is manufactured by using low-power CMOS technology and is available in a 28-pin, plastic DIP or in a 28-pin, plastic SOJ package. The T7289A device is functionally compatible with the T7289, LC1046A, and LC1046C devices for 1.544 Mbits/s operation but provides improved jitter transfer and crosstalk characteristics with a selectable single-rail/dual-rail system interface.

Description (continued)

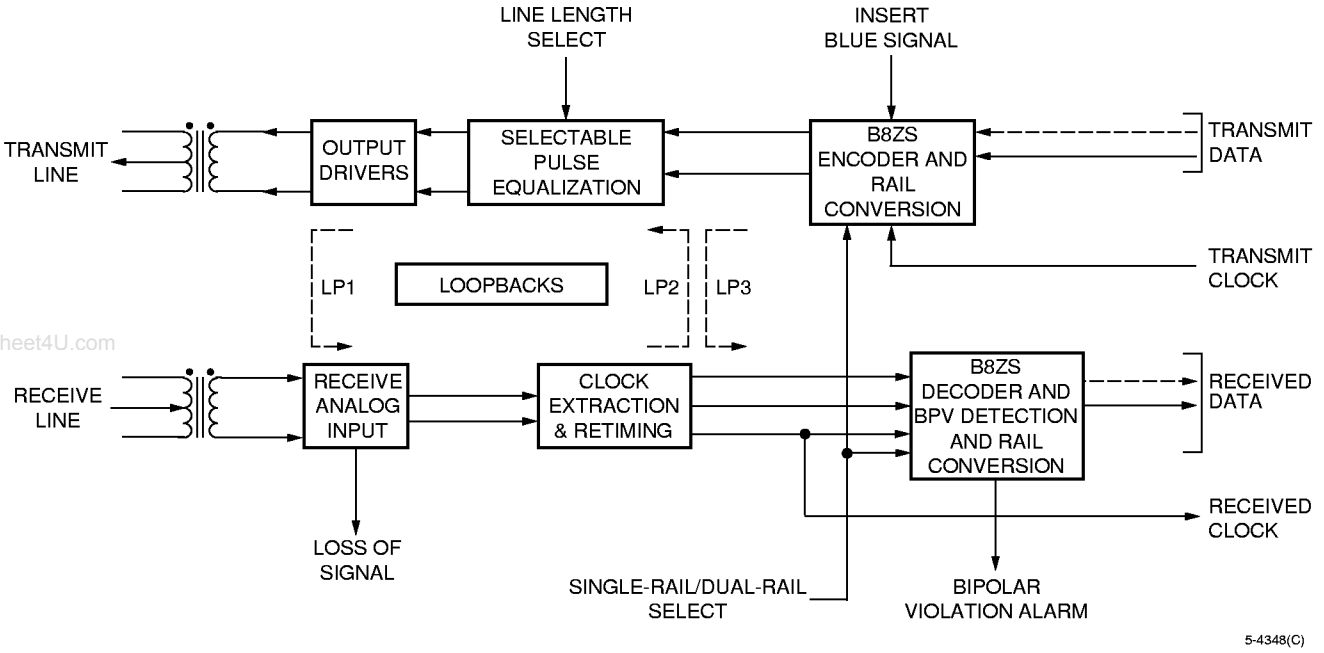


Figure 1. T7289A Block Diagram

Pin Information

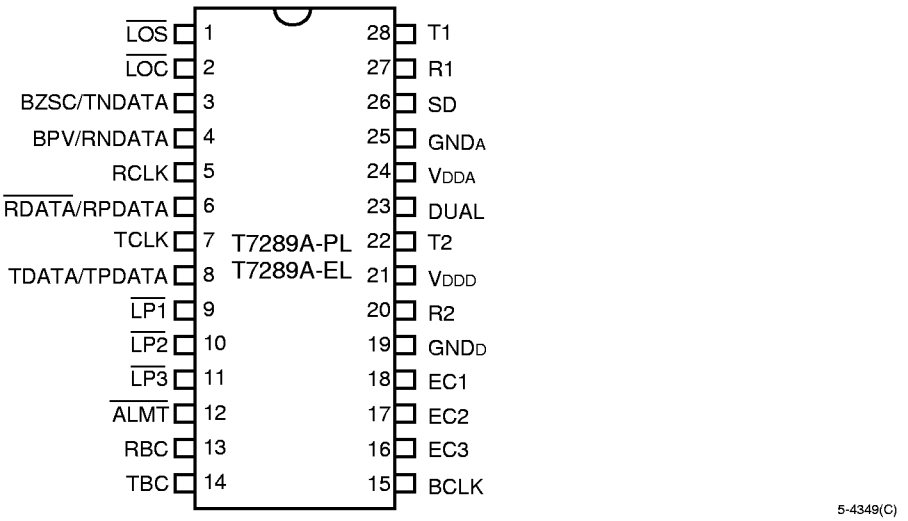


Figure 2. Pin Diagram

Pin Information (continued)

Table 1. Pin Descriptions

This table refers to a cleared pin as low (0) and a set pin as high (1).

Pin	Symbol	Type*	Name/Function
1	$\overline{\text{LOS}}$	O^u	**Loss of Signal (Active-Low).** This pin is cleared upon loss of the data signal at the receiver inputs.
2	$\overline{\text{LOC}}$	O^u	**Loss of Clock (Active-Low).** This pin is cleared when SD = 1 and $\overline{\text{LOS}}$ = 0, indicating that a loss of clock has occurred. When $\overline{\text{LOC}}$ = 0, no transitions occur on the RCLK and $\overline{\text{RDATA}}$ outputs. A valid clock must be present at BCLK for this function to operate properly.
3	BZSC/TNDATA	I^d	**B8ZS Enable/Transmit Data Negative Rail.** If dual = 0, this pin is set to insert a B8ZS substitution code on the transmit side and to remove the substitution code on the receive side. If dual = 1, this pin is used as the transmit data negative rail.
4	BPV/RNDATA	O	**Bipolar Violation/Receive Data Negative Rail.** If dual = 0, this pin is set upon detection of a bipolar violation on the receive-side input after the removal of the B8ZS substitution code that contains legal violations. If dual = 1, this pin is used as the receive data negative rail.
5	RCLK	O	**Receive Clock.** Output receive clock signal to the terminal equipment.
6	$\overline{\text{RDATA}}$ /RPDATA	O	**Receive Data (Active-Low)/Receive Data Positive Rail.** If dual = 0, this pin is used as 1.544 Mbits/s inverted unipolar output data with a 100% duty cycle. If dual = 1, this pin is used as the transmit data positive rail.
7	TCLK	I	**Transmit Clock.** DS1 input clock signal (1.544 MHz ± 130 ppm).
8	TDATA/TPDATA	I	**Transmit Data/Transmit Data Positive Rail.** If dual = 0, this pin is used as 1.544 Mbits/s unipolar input data. If dual = 1, this pin is used as the transmit data positive rail.
9	$\overline{\text{LP1}}$	I^u	**Loopback 1 Enable (Active-Low).** This pin is cleared for a full local loopback (transmit converter output to receive converter input). Most of the transmit and receive analog circuitry is exercised in this loopback.
10	$\overline{\text{LP2}}$	I^u	**Loopback 2 Enable (Active-Low).** This pin is cleared for a remote loopback (DSX to DSX). In loopback 2, a high on TBC (pin 14) inserts the blue signal on the transmit side.
11	$\overline{\text{LP3}}$	I^u	**Loopback 3 Enable (Active-Low).** This pin is cleared for a digital local loopback. Only the transmit and receive digital sections are exercised in this loopback.
12	$\overline{\text{ALMT}}$	I^u	**Alarm Test Enable (Active-Low).** This pin is cleared, forcing $\overline{\text{LOS}}$ = 0, $\overline{\text{LOC}}$ = 0, and BPV = 1 for testing without affecting data transmission.
13	RBC	I^d	**Receive Blue Control.** This pin is set to insert the blue signal on the receive side. During single-rail mode, $\overline{\text{RDATA}}$ is cleared. During dual-rail mode, RPDATA and RNDATA toggle at half the blue clock rate. Blue clock must be present.

* I = input, O = output, I^u = input with pull-up, I^d = input with pull-down, O^u = output with pull-up.
† See Table 2.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

Pin	Symbol	Type	Name/Function
14	TBC	I^d	**Transmit Blue Control (AIS).** This pin is set to insert the blue signal (all 1s) on the transmit side. This control has priority over a loopback 2 if both are operated simultaneously.
15	BCLK	I	**Blue Clock.** DS1 blue clock signal (1.544 MHz ± 130 ppm). This clock is independent of the transmit clock.
16	EC3	I^d	**Equalizer Control 3†.** One of three control leads for selecting transmit equalizers.
17	EC2	I^d	**Equalizer Control 2†.** One of three control leads for selecting transmit equalizers.
18	EC1	I^d	**Equalizer Control 1†.** One of three control leads for selecting transmit equalizers.
19	GND_D	—	**Digital Ground.**
20	R2	O	**Transmit Bipolar Ring.** Negative bipolar transmit output.
21	V_{DDD}	—	**5 V Digital Supply (±10%).**
22	T2	O	**Transmit Bipolar Tip.** Positive bipolar transmit output.
23	DUAL	I^d	**Dual-Rail Mode Select.** This pin is cleared for single-rail mode and set for dual-rail mode.
24	V_{DDA}	—	**5 V Analog Supply (±10%).**
25	GND_A	—	**Analog Ground (±10%).**
26	SD	I^d	**Shutdown.** This pin is set forcing RCLK high, $\overline{RDATA}$ high, and $\overline{LOC}$ low (for single-rail operation) if a loss of signal is detected ($\overline{LOS}$ = 0). For dual-rail mode, RPDATA and RNDATA are forced low.
27	R1	I	**Receive Bipolar Ring.** Negative bipolar receive input.
28	T1	I	**Receive Bipolar Tip.** Positive bipolar receive input.

* I = input, O = output, I^u = input with pull-up, I^d = input with pull-down, O^u = output with pull-up.
† See Table 2.

Table 2. Equalizer Control

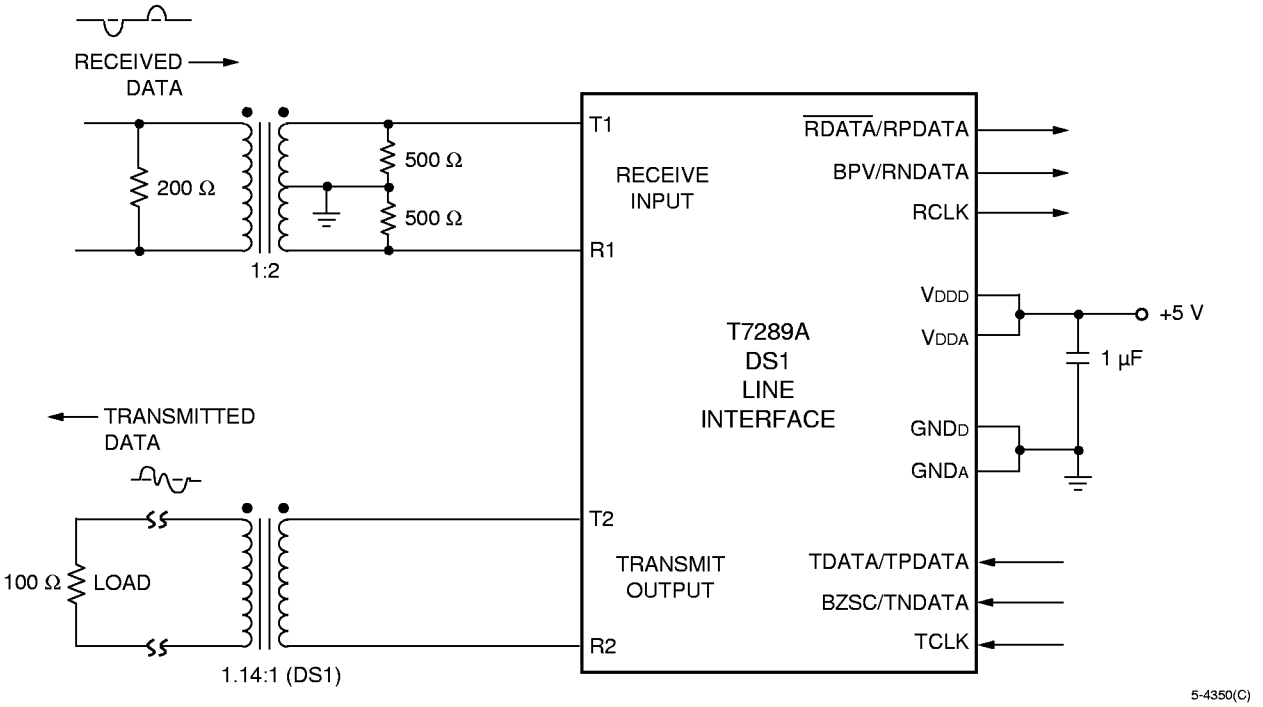
Other bit combinations represent test modes not to be used for normal operation.

Distance to DSX (Ft.)* (Applies Only to 22-gauge PIC [ABAM] Cable)	Maximum Cable Loss (dB at 772 kHz)	EC1	EC2	EC3
0—133	0.6	0	0	0
133—267	1.2	0	0	1
267—400	1.8	0	1	0
400—533	2.4	0	1	1
533—655	3	1	0	0

* Use maximum loss figures for other cable types.

Overview

The T7289A device is a fully integrated DS1 line interface that requires only two line-interface transformers and three input termination resistors to provide a bidirectional line interface between a DS1 cross connect (DSX) and terminal equipment. A typical application diagram is shown in Figure 3. This device is specified for use with 22-gauge, plastic-insulated ABAM cable, as well as other cable types. The circuit is divided into three main blocks: transmit converter, receive converter, and logic. The transmit and receive converters process information signals through the device in the transmit and receive directions, respectively; the logic is the control and status interface for the device.



Note: Lucent 2745 family pulse transformers for through-hole mounting or Lucent 2758 family pulse transformers for surface mounting are recommended.

Figure 3. Typical Application Diagram for Bipolar Signal Interfacing

Transmit Converter

The line-interface transmission format is return-to-zero, bipolar alternate mark inversion (AMI), requiring transmission and sensing of alternately positive and negative pulses. During single-rail operation, the transmit converter accepts unipolar data at TDATA and converts the signal to a balanced bipolar data signal. Binary 1s in the TDATA data stream become pulses of alternating polarity transmitted between the two output rails, T2 and R2. For dual-rail operation, a binary 1 on TPDATA results in the transmission of a positive pulse between T2 and R2, and a binary 1 on TNDATA results in a negative pulse. Binary 0s are transmitted as null pulses. All necessary transmit pulse shaping is done on-chip, eliminating the need for external shaping networks. This is done by shaping the pulses at the bipolar output (T2, R2) according to the selected equalizer control (EC1—EC3) inputs (see Table 2).

The output pulse waveform consists of four distinct levels: overshoot, pulse, backswing, and tail. They are produced by a high-speed D/A converter and are driven onto the line by using low-impedance output buffers. There are five different pulse shapes, corresponding to 133-ft. increments of cable, that are obtained by setting the appropriate equalizer control inputs. The positive and negative pulses meet the amplitude, rise and fall time, overshoot, undershoot, template, and power requirements for the office DSX cross connect as given in Compatibility Bulletin 119 (CB119). A typical DS1 output waveform at the DSX relative to the CB119 template is shown in Figure 4. The analog circuitry is shown in Figure 5.

The clock multiplier shown in Figure 5 produces the high-speed timing waveforms needed by the D/A converter. The clock multiplier also eliminates the need for the tightly controlled transmit clock duty cycle usually required in discrete implementations. Transmitter specifications are given in Table 7.

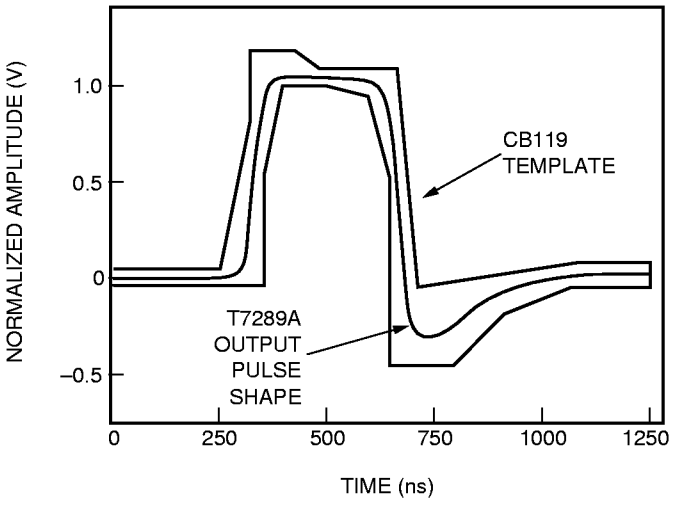


Figure 4. Typical T7289A Output Waveform at DSX

Transmit Converter (continued)

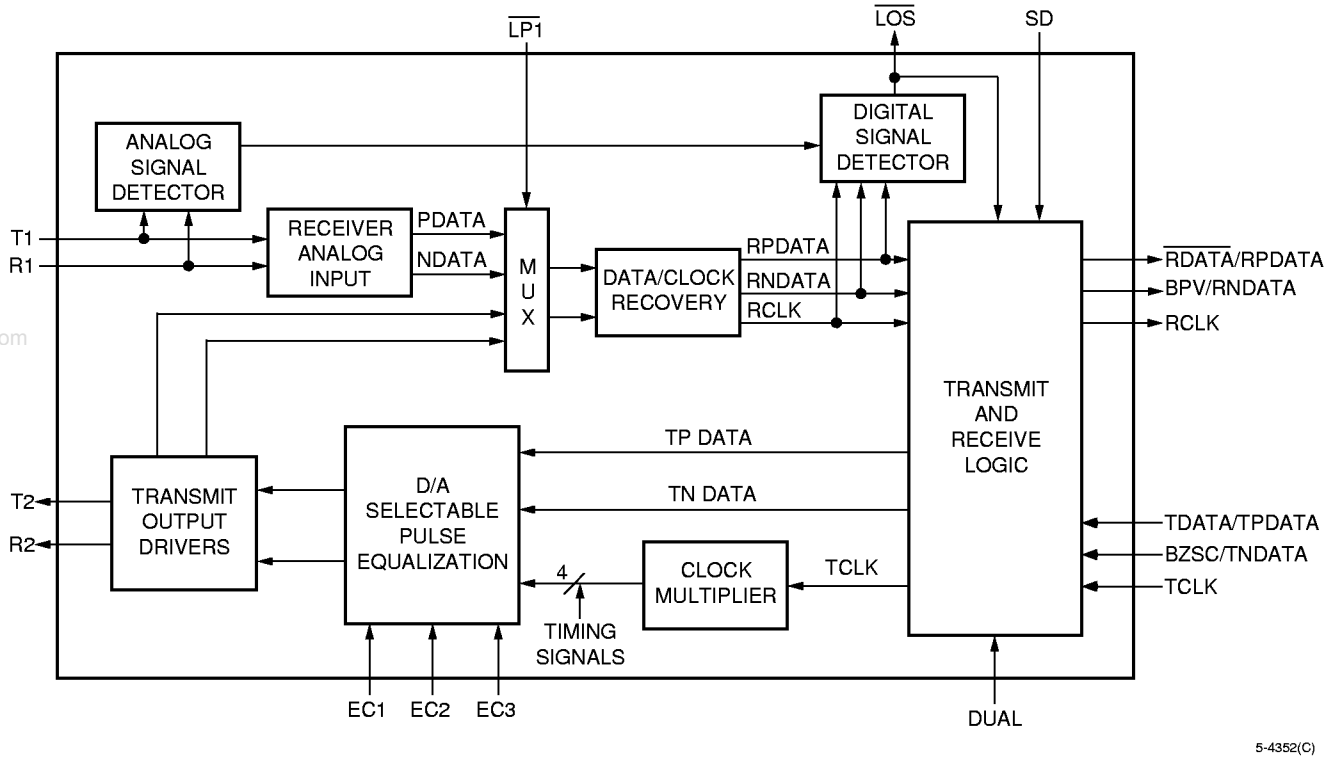


Figure 5. T7289A Analog Block Diagram

Receive Converter

The receive converter accepts bipolar input signals (T1, R1), coupled through a receive transformer, from the cross connect over a maximum of 655 ft. of 22-gauge PIC (ABAM) cable. The received signal is rectified while the amplitude and rise time are restored. These input signals are peak-detected and sliced by the receiver front end, producing the digital signals PDATA and NDATA (Figure 5). The timing is extracted by means of phase-locked loop (PLL) circuitry that locks an internal, free-running, current-controlled oscillator (ICO) to the 1.544 MHz (DS1 signal) component.

The PLL employs a 3-state phase detector and a low-voltage/temperature coefficient ICO. The ICO free-running frequency is trimmed to within ±2.5% of the data rate at wafer probe, with V_{DD} = 5.0 V and T_A = 25 °C. For all operating conditions (see Operating Conditions section), the free-running oscillator frequency deviates from the data rate by less than ±6%, alleviating the problem of harmonic lock.

For robust operation, the PLL is augmented with a frequency-acquisition capability. The frequency acquisition circuitry is intended to guarantee proper phase-locking during start-up conditions, such as powerup or data activation. Once the T7289A device is phase-locked to data, the frequency-acquisition mode will **not** be activated.

A continuous (i.e., ungapped, unswitched) 1.544 MHz reference clock must be present at TCLK to enable the frequency-acquisition circuitry. However, the receive PLL will operate even in the absence of TCLK.

Because the clock output of the receive converter is derived from the ICO, a free-running clock can be present at the output of the receive converter without data being present at the input. A shutdown pin (SD) is provided to block this clock, if desired, to eliminate the free-running clock upon loss of the input signal.

Receive Converter (continued)

Two methods of loss-of-signal detection are used in this chip. The analog signal detector shown in Figure 5 uses the output of the receiver peak detector to determine if a signal is present at T1 and R1. If the input amplitude drops below approximately 0.5 V, the analog detector output becomes active. Hysteresis (250 mV) is provided in the analog detector to eliminate $\overline{LOS}$ chattering. In addition, the digital signal detector counts 0s in the recovered data. If more than 128 consecutive 0s occur, the digital signal detector becomes active. In normal operation, the detector outputs are ORed together to form $\overline{LOS}$; however, in loopback 1, only the digital signal detector is used to monitor the looped signal. Table 3 describes the operation of the shutdown, $\overline{LOS}$, and $\overline{LOC}$ functions in normal operation and in loopback 1.

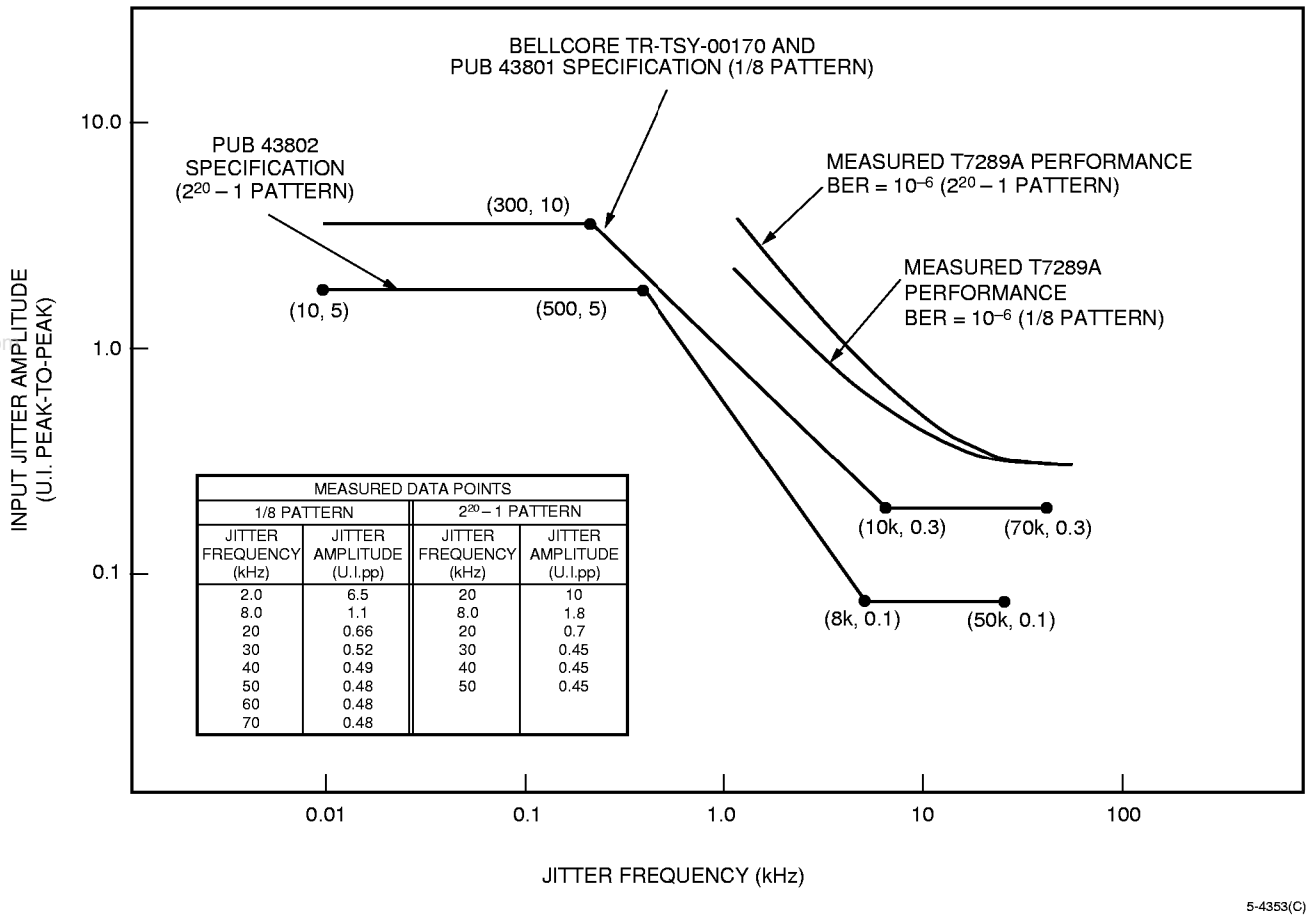
The PLL is designed to accommodate large amounts of input jitter with high power supply rejection for operation in noisy environments. Low jitter sensitivity to power supply noise allows compact line-card layouts that employ many line interfaces on one board. The minimum input jitter tolerance, as specified in AT&T Publication 43802, and the measured T7289A device jitter tolerance are shown for the DS1 rate in Figure 6. The data shown is typical for measurement to a BER of 10^{-6}. Subtracting approximately 0.02 U.I. from the given data yields the jitter accommodation for error-free operation. Receiver specifications are shown in Table 8.

Table 3. Shutdown, $\overline{LOS}$, and $\overline{LOC}$ Truth Table

x = don't care.

Inputs					Outputs			
$\overline{LP1}$	SD	$\overline{ALMT}$	Input Signal at T1, R1	Loopback 1 Signal	$\overline{LOS}$	$\overline{LOC}$	Receive Side	Active LOS Detectors
1	0	1	Active	x	1	1	Normal	Analog and digital
1	0	1	No Signal	x	0	1	Free-running VCO	Analog and digital
1	1	1	Active	x	1	1	Normal	Analog and digital
1	1	1	No Signal	x	0	0	No output	Analog and digital
0	0	1	x	Active	1	1	Normal loopback	Digital only
0	0	1	x	No Signal	0	1	Free-running VCO	Digital only
0	1	1	x	Active	1	1	Normal loopback	Digital only
0	1	1	x	No Signal	0	0	No output	Digital only
x	x	0	x	x	0	0	Unaffected	x

Receive Converter (continued)



MEASURED DATA POINTS			
1/8 PATTERN		2^20 – 1 PATTERN	
JITTER FREQUENCY (kHz)	JITTER AMPLITUDE (U.I.pp)	JITTER FREQUENCY (kHz)	JITTER AMPLITUDE (U.I.pp)
2.0	6.5	20	10
8.0	1.1	8.0	1.8
20	0.66	20	0.7
30	0.52	30	0.45
40	0.49	40	0.45
50	0.48	50	0.45
60	0.48		
70	0.48		

Figure 6. DS1 Jitter Tolerance

Digital Logic

The logic provides alarms, optional B8ZS coding, blue-signal insertion (AIS) circuits, and maintenance loop-backs. It accepts dual-rail or single-rail data patterns.

Single-Rail/Dual-Rail Option

To implement the rail-select feature, the dual pin (pin 23) is cleared for single-rail mode and set for dual-rail mode. When single-rail mode is selected, pin 8 (TDATA/TPDATA) accepts transmit data and pin 6 ($\overline{\text{RDATA}}$/RPDATA) outputs inverted receive data. When dual-rail mode is selected, pin 8 (TDATA/TPDATA) accepts the positive rail transmit data, and pin 3 (BZSC/TNDATA) is reconfigured to accept negative rail transmit data. Pin 6 ($\overline{\text{RDATA}}$/RPDATA) outputs positive rail receive data, and pin 4 (BPV/RNDATA) is reconfigured to output negative rail receive data. In dual-rail mode, the B8ZS and bipolar violation functions are disabled.

For single-rail operation, TDATA is active-high and $\overline{\text{RDATA}}$ is active-low. For dual-rail operation, TPDATA, TNDATA, RPDATA, and RNDATA are all active-high. This interface scheme is consistent with the dual-rail interfaces of other Lucent Line Interface products.

Digital Logic (continued)

Single-Rail/Dual-Rail Option (continued)

Alarms

An independent loss-of-clock ($\overline{\text{LOC}}$) output is provided so that loss of clock is detected when the shutdown option is in effect. $\overline{\text{LOS}}$ and $\overline{\text{LOC}}$ can be wire-ORed to produce a single alarm.

A bipolar violation (BPV) output is included, giving an alarm each time a violation (two or more successive 1s on a rail) occurs. The violation alarm output is held in a latch for one cycle of the internal clock (RCLK). In the B8ZS mode, bipolar violations within the legal substitution code are not detected and, therefore, do not produce an alarm. The bipolar violation function is disabled when dual = 1.

An alarm test pin ($\overline{\text{ALMT}}$) is provided to test the alarm outputs, $\overline{\text{LOS}}$, $\overline{\text{LOC}}$, and BPV. Clearing this pin forces the alarm outputs to the alarm state without affecting data transmission.

In order to meet the requirement that the system not report LOS for a string of <100 consecutive 0s and that LOS be reported for ≥250 consecutive 0s, the digital LOS threshold counter is set at 128. However, between 32 and 64 consecutive 0s, the device changes from locking on incoming data to locking on TCLK. If the phase of TCLK is sufficiently different from the received data, the device can count both 1s and 0s as 0s. This can cause the digital LOS counter to exceed its threshold, even though the number of consecutive 0s in the data is less than 100.

B8ZS Option

The T7289A device contains a B8ZS encoder and decoder that can be selected by setting the BZSC pin. This allows the encoder to substitute a zero-substitution code for eight consecutive 0s detected in the data stream, as illustrated in Table 4. A V represents a violation of bipolar code, and a B represents a bipolar pulse of correct polarity. The decoder detects the zero-substitution code and reinserts eight 0s in the data stream. The B8ZS option is disabled when dual = 1.

Table 4. B8ZS Substitution Code

Before B8ZS	00000000
After B8ZS	000VB0VB

Blue-Signal (AIS) Generators

There are two blue-signal generators in this device. If RBC = 1, an all-1s signal is output on the receive data output pin(s). If TBC = 1, a bipolar all-1s signal is transmitted through T2 and R2 and into the network. Both receive and transmit blue signals are synchronous with BCLK.

Loopback Paths

The T7289A device has three independent loopback paths that are activated by clearing the respective control inputs, $\overline{\text{LP1}}$, $\overline{\text{LP2}}$, or $\overline{\text{LP3}}$. Loopback 1 bridges the data stream from the transmit converter (transmit converter included) to the input of the receive converter. The maintenance loop includes most of the internal circuitry.

Loopback 2 provides a loopback of data from the bipolar inputs (T1, R1) and the associated recovered clock to the bipolar outputs of the transmit converter (T2, R2). The receive front end, receive PLL, and transmit driver circuitry are all exercised. The loop can be used to isolate failures between systems.

Loopback 3 loops the data stream as in loopback 1, but bypasses the transmit and receive converters. The blue signal can be transmitted towards the DSX when in this loopback. Loopbacks 2 and 3 can be operated simultaneously to provide transmission loops in both directions.

Device Anomaly

T7289A-EL, T7289A-PL, T7289A-EL2, and T7289A-PL2

The T7289A-EL, T7289A-PL, T7289A-EL2, and T7289A-PL2 devices have been found to be sensitive to slow powerup ramp on the +5 V device supply. In general, if the powerup time is >50 µs, the device may not operate properly. The device must be power-cycled with a power-ramp interval of less than 50 µs to clear the condition. This anomaly is corrected in the T7289A-EL4 and T7289A-PL4.

T7289A-EL, T7289A-PL, T7289A-EL2, T7289A-PL2, T7289A-EL3, and T7289A-PL3

The T7289A-EL, T7289A-PL, T7289A-EL2, T7289A-PL2, T7289A-EL3, and T7289A-PL3 devices have been found to be sensitive to voltage surges on the transmit analog interface leads. The device may latch-up when excessive voltage surges are present on the line. The device must be power-cycled to clear the condition. The immunity to voltage surges has been enhanced in the T7289A-EL4 and T7289A-PL4.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
dc Supply Voltage Range	V_{DD}	–0.5	6.5	V
Power Dissipation	P_{dis}	—	500	mW
Storage Temperature Range	T_{stg}	–65	125	°C

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Lucent employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. No industry-wide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and therefore can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using these circuit parameters:

Human-Body Model ESD Threshold	
Device	**Voltage**
T7289A	>2000 V

Electrical Characteristics

Operating Conditions

T_A = –40 °C to +85 °C; V_{DD} = 5 V ± 10%

Table 5. Power Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Power Dissipation*	P_D	—	115	138	mW

* Measurement conditions with 50% 1s on the transmit side, T_A = 25 °C, and equalizer settings: EC1 = 0, EC2 = 1, EC3 = 0 (V_{DD} = 5 V). Power supply current varies by less than 5% with variations in temperature and power supply voltage.

Electrical Characteristics (continued)

Operating Conditions (continued)

Table 6. Logic Interface Electrical Characteristics

Parameter	Symbol	Condition	Min	Max	Unit
Input Voltage:					
Low	V_{IL}	—	GND$_D$	0.8	V
High	V_{IH}	—	2.0	V_{DDD}	V
Output Voltage (except $\overline{LOS}$ and $\overline{LOC}$):					
Low	V_{OL}	I_{OL} = 4.9 mA	—	0.4	V
High	V_{OH}	I_{OH} = –4.9 mA	2.4	—	V
High, CMOS	V_{OHC}	I_{OHC} = –0.49 mA	3.5	V_{DDD}	V
Output Voltage ($\overline{LOS}$, $\overline{LOC}$):					
Low	V_{OL}	I_{OL} = 4.9 mA	—	0.4	V
High	V_{OH}	I_{OHC} = –10 µA	3.5	V_{DDD}	V
Input Capacitance	C_I	—	20	—	pF
Load Capacitance	C_L	—	40	—	pF

Internal pull-up devices are provided on the following input leads: $\overline{LP1}$, $\overline{LP2}$, $\overline{LP3}$, and $\overline{ALMT}$. Internal pull-down devices are provided on the following leads: SD, RBC, BZSC/TNDATA, TBC, DUAL, EC1, EC2, and EC3. The internal pull-up or pull-down devices require the input to source or sink no more than 20 µA. Output pull-up is provided on leads $\overline{LOS}$ and $\overline{LOC}$.

Table 7. Transmitter Specifications

Parameter	Min	Typ	Max	Unit
Output Pulse Amplitude (at the DSX)	2.4	3.0	3.6	V
Pulse Width (50%)	333	350	362	ns
Output Power Levels:				
2 kHz Band at 772 kHz	12.6	16.5	17.9	dBm
2 kHz Band at 1544 kHz	–29	–39	—	dB*
Positive/Negative Pulse Imbalance†	—	—	0.5	dB
Rise/Fall Time (20%—80%)	—	—	50	ns
Output Termination	95	100	105	Ω
Output Transformer Turns Ratio	1:1.12	1:1.14	1:1.16	—
PSRR:				
dc < Frequency < 200 kHz	35	—	—	dB
200 kHz < Frequency < 500 kHz	25	—	—	dB
500 kHz < Frequency < 5 MHz	8	—	—	dB

* Below the power at 772 kHz.
† Total power difference.

Electrical Characteristics (continued)

Operating Conditions (continued)

Table 8. Receiver Specifications

Parameter	Condition	Min	Typ	Max	Unit
Receiver Sensitivity (at input of device)	—	0.85	—	—	Vp
PLL: 3 dB Bandwidth Peaking	 1/8 input 1/8 input	 — —	 33 1.2	 — 2.0	 kHz dB
Allowed Cable Loss* at BER = 10^{-9}	V_{DD} = 5.0 V; Vac on V_{DD} = 0.5 Vpp, from dc to 4 MHz	—	12	9	dB
Input Density (1s)	Maximum number of consecutive 0s = 15	12.5	—	—	%
ICO Free-running Frequency Error	—	—	—	±6	%
Input Transformer Turns Ratio	—	1:1.9	1:2.0	1:2.1	—
Input Termination	—	—	100	—	Ω
Input Resistance, R1 or T1	Each Input to Ground	0.9	—	3.0	kΩ

* Minimum sensitivity (maximum cable loss limit) occurs when the frequency of Vac is near the clock rate.

Timing Characteristics

All duty cycle and timing relationships are referenced to a TTL 1.4 V threshold level.

Loss-of-Clock Indication Timing

The clock must be absent 5.18 µs to guarantee a loss-of-clock indication. However, it is possible to produce a loss-of-clock indication if the clock is absent for 2.59 µs depending on the timing relationship of the interruption with respect to the timing cycle.

The returning clock must be present 5.18 µs to guarantee a normal condition on the loss-of-clock pin ($\overline{LOC}$). However, the loss-of-clock indication can return to normal immediately, depending on the timing relationship of the signal return with respect to the timing cycle.

Table 9. System Interface

Symbol	Description	Min	Typ	Max	Unit
tTCLTCL	TCLK Clock Period	*	647.7	*	ns
tTCHTCL	TCLK Duty Cycle	40	50	60	%
tTDVTCL	Data Setup Time, TDATA to TCLCK	50	—	—	ns
tTCLTDV	Data Hold Time, TCLK to TDATA	40	—	—	ns
tr	Clock Rise Time (10%—90%)	—	—	40	ns
tf	Clock Fall Time (10%—90%)	—	—	40	ns
tRCHRDV	Data Hold Time, RCLK to $\overline{RDATA}$, BPV	227	—	—	ns
tRDVRCH	Data Setup Time, $\overline{RDATA}$, BPV to RCLK	187	—	—	ns
tRCLRDV	Propagation Delay, RCLK to $\overline{RDATA}$	—	—	40	ns

* A tolerance of ±130 ppm.

Timing Characteristics (continued)

Loss-of-Clock Indication Timing (continued)

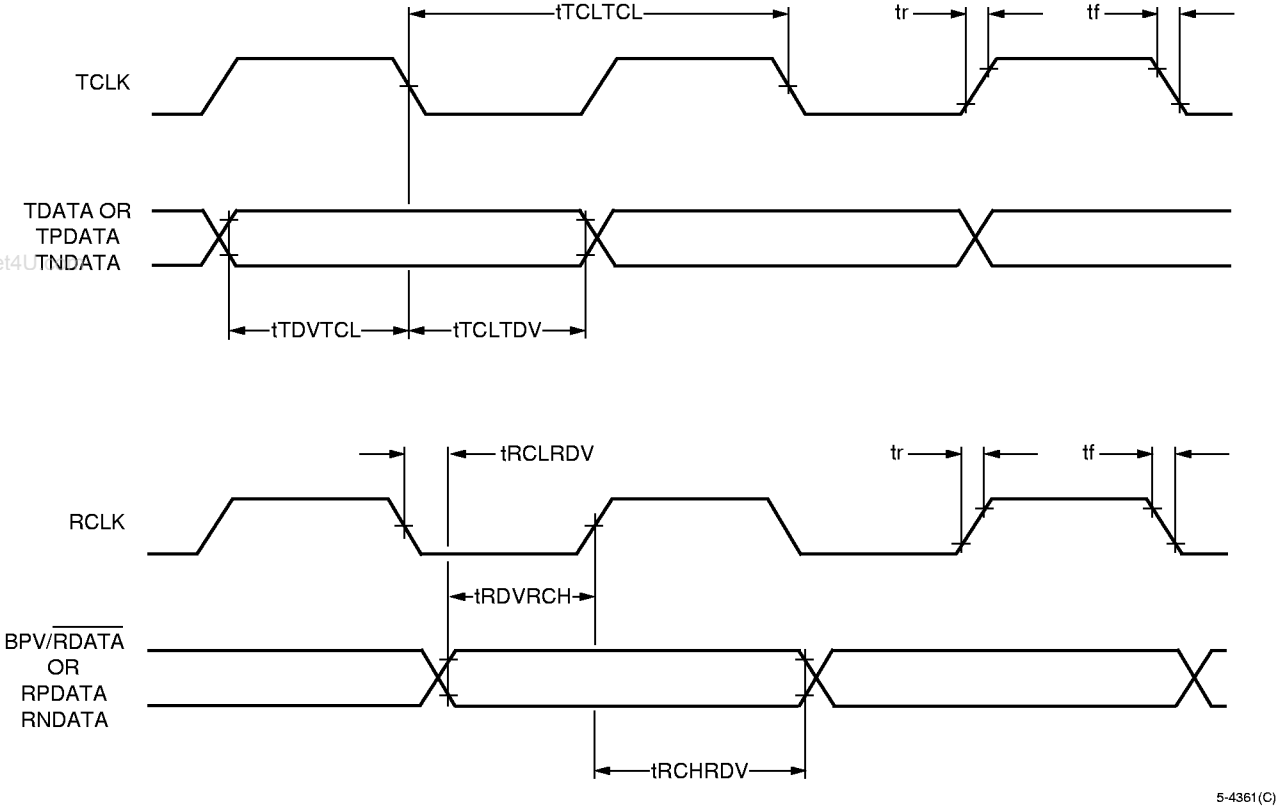
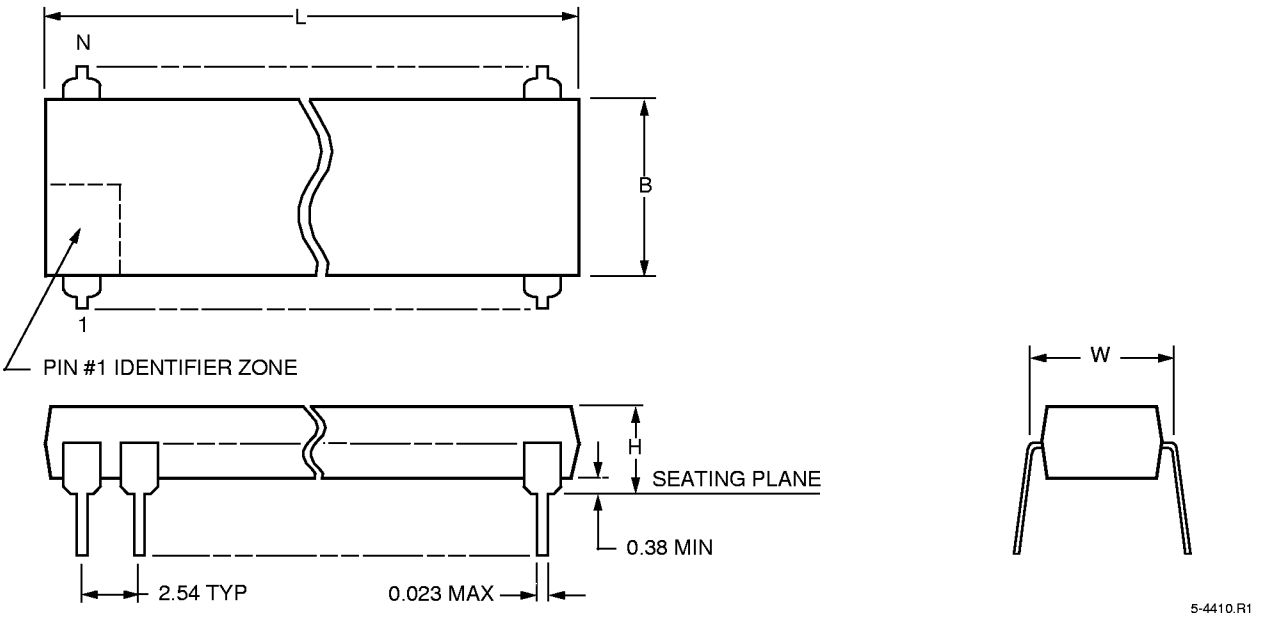


Figure 7. Timing Diagram (Single-Rail or Dual-Rail)

Outline Diagrams

28-Pin, Plastic DIP

Dimensions are in millimeters.

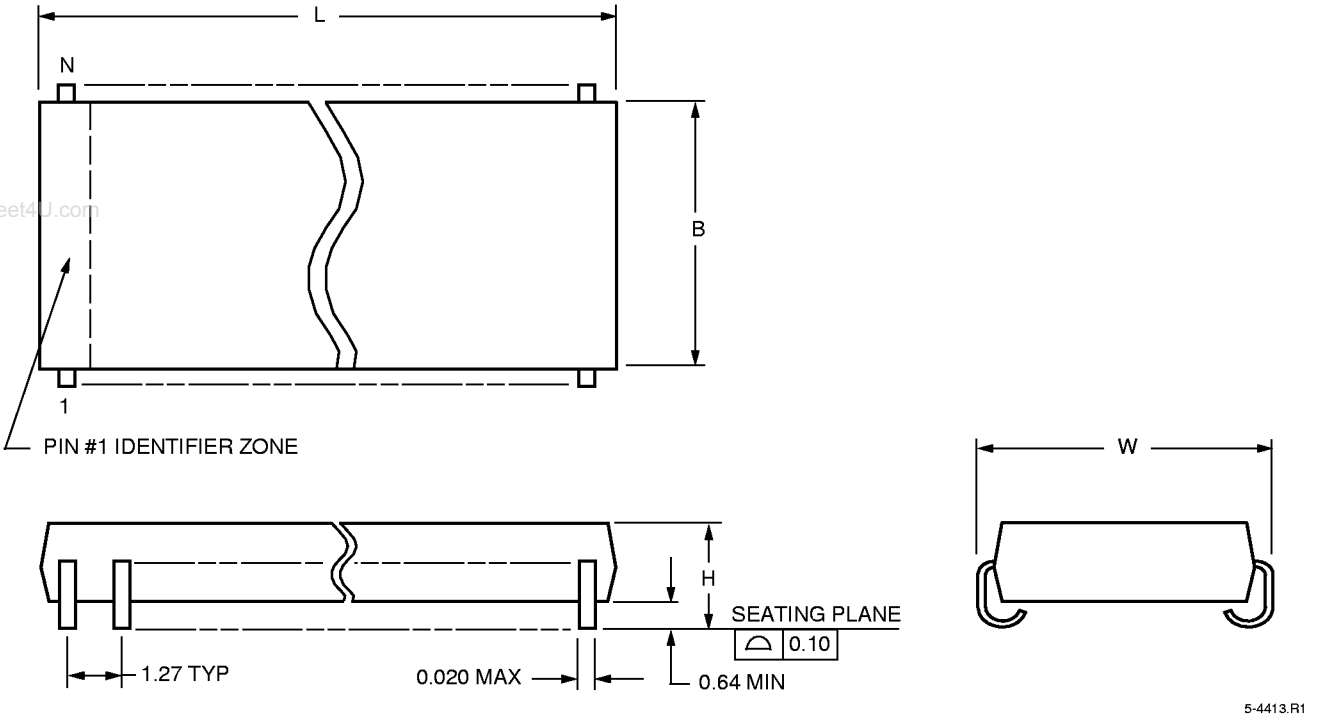


Number of Pins (N)	Package Dimensions (DIP)			
	Maximum Length Including Leads (L)	Maximum Width Without Leads (B)	Maximum Width Including Leads (W)	Maximum Height Above Board (H)
28	37.34	13.97	15.49	5.59

Outline Diagrams (continued)

28-Pin, Plastic SOJ

Dimensions are in millimeters.



Number of Pins (N)	Package Dimensions (SOJ)			
	Maximum Length Including Leads (L)	Maximum Width Without Leads (B)	Maximum Width Including Leads (W)	Maximum Height Above Board (H)
28	18.03	7.62	8.81	3.18

Ordering Information

Device Code	Package	Temperature	Comcode (Ordering Number)
T - 7289A - - - PL4	28-Pin DIP	–40 °C to +85 °C	107056699
T - 7289A - - - EL4	28-Pin SOJ	–40 °C to +85 °C	107056673

DS97-196TIC Replaces DS92-072SMOS Catalog CA95-003TIC Version to Incorporate the Following Updates

1. Data sheet format.
2. **Note:** CA95-003TIC version of data sheet had device advisory AY93-025TCOM incorporated in it.