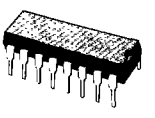
SGS-THOMSON MICROELECTRONICS

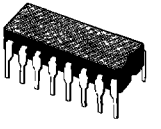
T74LS164

SERIAL-IN PARALLEL-OUT SHIFT REGISTER

- TYPICAL SHIFT FREQUENCY OF 35 MHz
- ASYNCHRONOUS MASTER RESET
- GATED SERIAL DATA INPUT
- FULLY SYNCHRONOUS DATA TRANSFERS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

T74LS164 D1 T74LS164 C1
T74LS164 B1 T74LS164 M1

DESCRIPTION

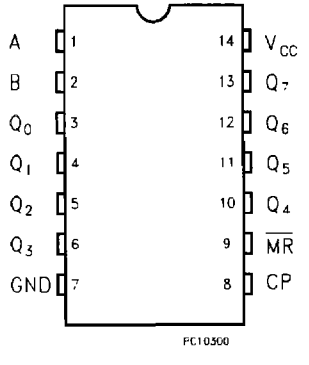
The T74LS164 is a 8-Bit Serial-In Parallel-Out Shift Register. Serial data is entered through a 2-Input AND gate synchronous with LOW to HIGH transition of the clock. The device features an asincronous Master Reset which clears the register setting all outputs LOW indipendent of the clock. It utilizes the Schottky diode clamped process to archive high sppeds and is fully compatible with all TTL roducts.

PIN NAMES

A, B	Data Input
CP	Clock (Active HIGH Going Edge) Input
MR	Master Reset (Active LOW) Input
Q_0-Q_7	Outputs

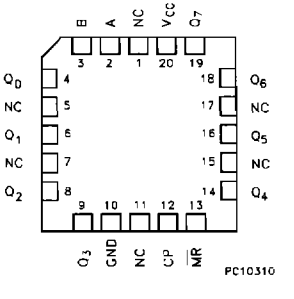
PIN CONNECTION (top view)

DUAL IN LINE



PC10300

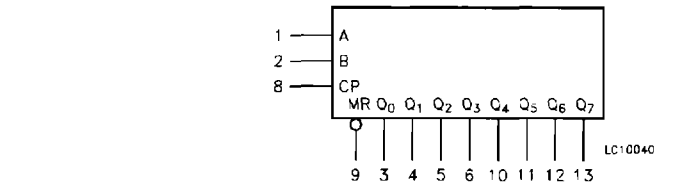
CHIP CARRIER

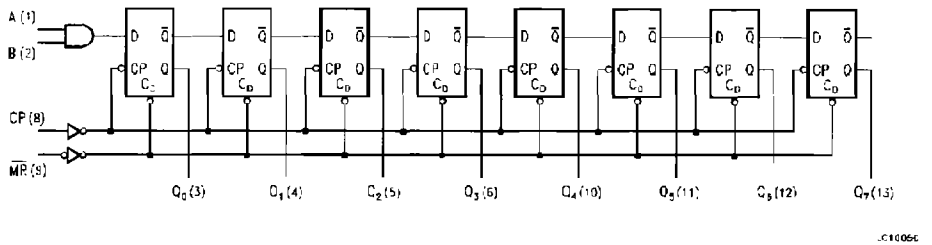


PC10310

NC = No Internal Connection

LOGIC SYMBOL AND LOGIC DIAGRAM





V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS164XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

FUNCTIONAL DESCRIPTION

The LS164 is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputss can be used as an active HIGH Enable for data entry through the other input. An unused input must be tied HIGH, or both inputs connected together.

Each LOW to HIGH transition on the Clock (CP) input shifts data one place to the right and enters into Q0 the logoical AND of the two inputs (A B) that existed before the rising clock edge.

A LOW level on the Master Reset (MR) input overrides all other inputs and clears the register asynchronous, forcing all Q outputs LOW.

TRUTH TABLE

OPERATING MODE	INPUTS				
	MR	A	B	Q_0	Q_1-Q_7
Reset (Clear)	L	X	X	L	L-L
Shift	H	l	l	L	q_0-q_6
	H	l	h	L	q_0-q_6
	H	h	l	L	q_0-q_6
	H	h	h	H	q_0-q_6

L (l) = LOW Voltage Levels
H (h) = HIGH Voltage Levels
X = Don't Care
q_n = Lower case letters indicate the state of the referenced input or output one set-up time prior to the LOW to HIGH clock transition

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Input		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Input		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.5		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current			20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current (Note 3)		16	27	V_{CC} = MAX		mA

Notes : 1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions
2. Not more than one output should be shorted at a time.
3. I_{CC} is measured with outputs open serial input at 2 4V, and a momentary ground, hen 4 5V applied to clear.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
f_{MAX}	Maximum Clock Frequency	25	36		Figures 1	V_{CC} = 5.0 V C_L = 15 pF	MHz
t_{PLH} t_{PHL}	Propagation Delay, Positive Going Clock to Outputs		17 21	27 32	Figures 1		ns
t_{PHL}	Propagation Delay, Negative Going MR to Outputs		24	36	Figures 2		ns

AC SET-UP REQUIREMENTS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
t_s	Set-Up Time, A or B Input to Positive-Going CP	15			Figure 3	V_{CC} = 5.0 V C_L = 15 pF	ns
t_h	Hold Time, A or B Input to Positive-Going CP	5			Figure 3		ns
$t_{wCP(H)}$	CP Pulse Width (HIGH)	20			Figure 1		ns
$t_{wCP(L)}$	CP Pulse Width (LOW)	20			Figure 1		ns
$t_{wMR(L)}$	MR Pulse Width (LOW)	20			Figure 2		ns
t_{rec}	Recovery Time, Positive-Going MR to Positive-Going CP	20			Figure 2		ns

AC WAVEFORMS

Figure 1

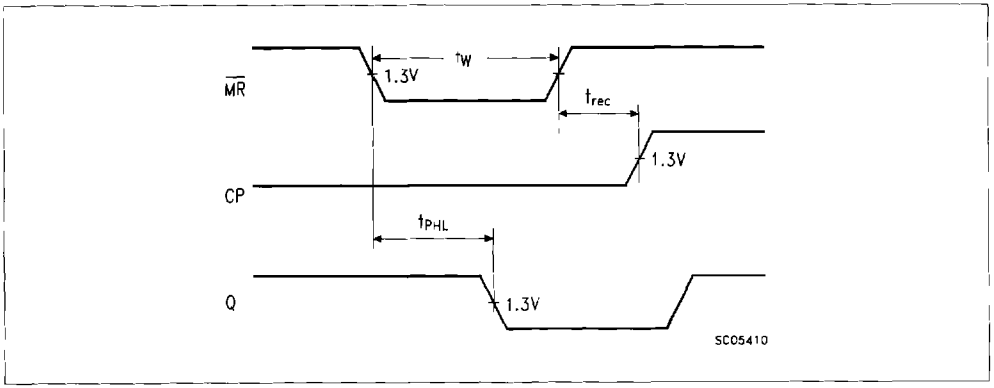


Figure 2

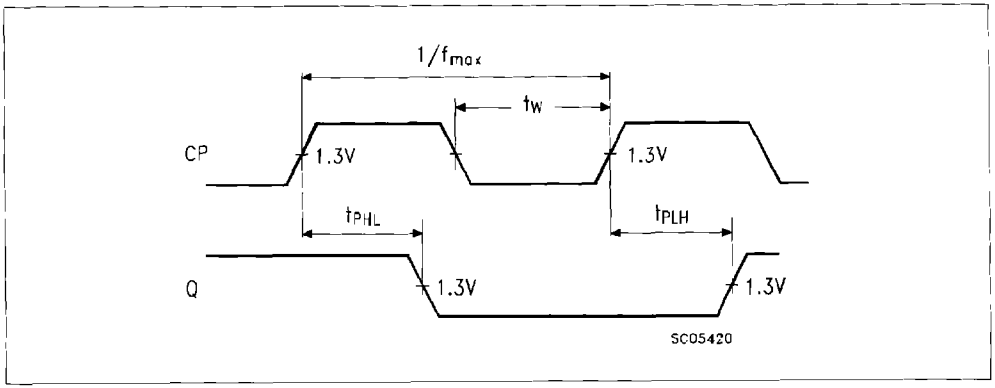
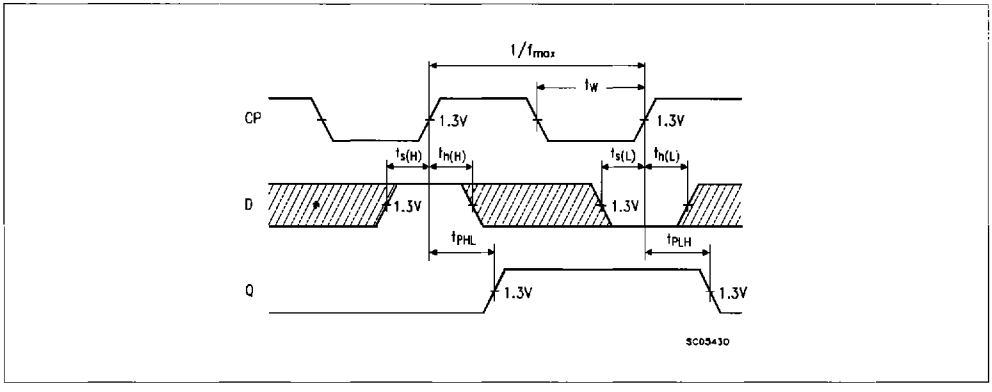


Figure 3


1/fmax
tw
CP
1.3V
1.3V
ts(H)
th(H)
ts(L)
th(L)
D
1.3V
1.3V
tPHL
tPLH
Q
1.3V
1.3V
SC03430