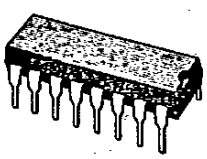
T74LS170

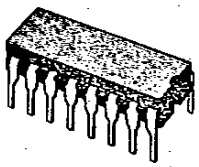
T-46-09-09

4 x 4 REGISTER FILE

- SIMULTANEOUS READ/WRITE OPERATION
- EXPANDABLE TO 512 WORDS OF n-BIT
- TYPICAL ACCESS TIME OF 20 ns
- LOW LEAKAGE OPEN COLLECTOR OUTPUTS FOR EXPANSION
- TYPICAL POWER DISSIPATION OF 125 mW
- INPUT CLAMP DIODE LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY COMPATIBLE



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

T74LS170 D1	T74LS170 C1
T74LS170 B1	T74LS170 M1

DESCRIPTION

The T74LS170 is a high speed, low power 4 x 4 Register File organized as four word by four bits. Separate read and write inputs, both address and enable, allow simultaneous read and write operation.

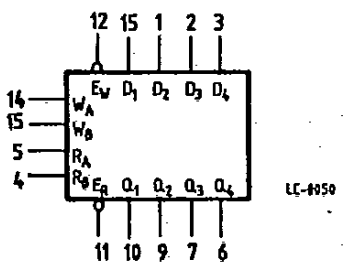
Open Collector outputs make it possible, to connect up to 128 outputs in a wired-AND configuration to increase the word capacity up to 512 words. Any number of these devices can be operated in parallel to generate an n-bit length.

The T74LS670 provides a similar function tothis device but it features 3-state outputs.

PIN NAMES

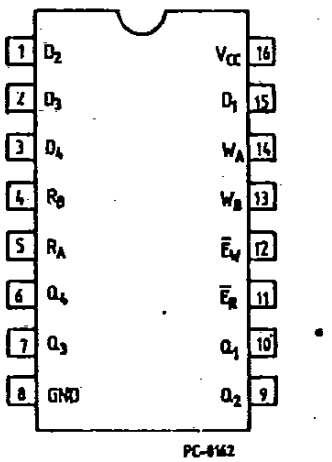
D_1-D_4	Data Inputs
W_A-W_B	Write Address Inputs
$\overline{E}_W$	Write Enable (Active LOW) Input
R_A-R_B	Read Address Inputs
$\overline{E}_R$	Read Enable (Active LOW) Input
Q_1-Q_4	Outputs

LOGIC DIAGRAM

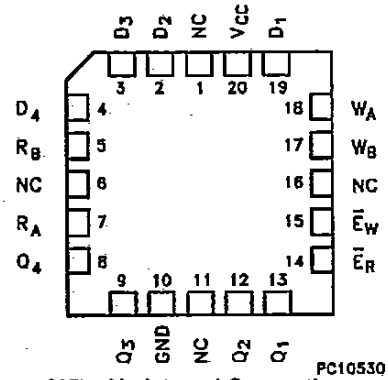


PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER



NC = No Internal Connection

WRITE TRUTH TABLE

WRITE INPUTS			WORD			
W_B	W_A	$\overline{E}_W$	0	1	2	3
L	L	L	Q = D	Q_0	Q_0	Q_0
L	H	L	Q_0	Q = D	Q0	Q0
H	L	L	Q_0	Q0	Q = D	Q0
H	H	L	Q_0	Q0	Q0	Q = D
X	X	H	Q_0	Q0	Q0	Q0

READ TRUTH TABLE

READ INPUTS			OUTPUTS			
R_B	R_A	$\overline{E}_R$	Q_1	Q_2	Q_3	Q_4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	H	H	H	H

NOTES: H= HIGH Level, L = LOW Level, X = Don't Care
(Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.
Q0 = The level of Q before the indicated input conditions were established.
W0B1 = The first bit of word 0 etc.

ABSOLUTE MAXIMUM RATINGS

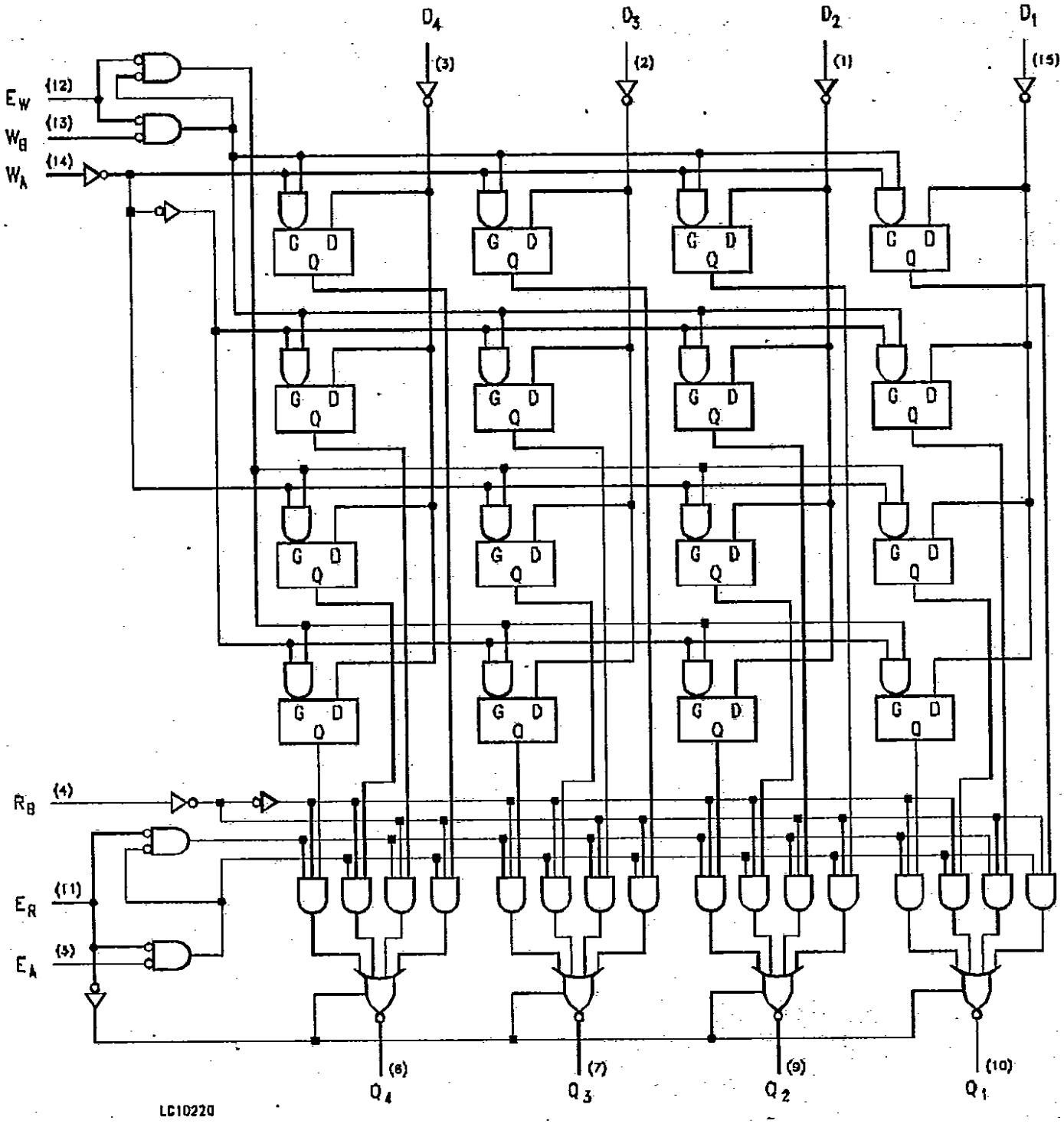
Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	0 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS170XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
I_{OH}	Output HIGH Current			20	V_{CC} = MIN, V_{OH} = - 5.5 V V_{IN} = V_{IH} or V_{IL} per Truth Table		µA
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current Any D, R or W $\overline{E}_R$ or $\overline{E}_W$			 20 40	V_{CC} = MAX, V_{IN} = 2.7 V		µA
	Any D, R or W $\overline{E}_R$ or $\overline{E}_W$			0.1 0.2	VCC = MAX, V_{IN} = 7.0 V		mA
I_{IL}	Input LOW Current Any D, R or W $\overline{E}_R$ or $\overline{E}_W$			 - 0.4 - 0.8	VCC = MAX, V_{IN} = 0.4 V		mA
I_{CC}	Power Supply Current (Note 2)		25	40	V_{CC} = MAX		mA

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. I_{CC} is measured under the following worst case conditions: 4.5 V is applied to all data inputs and both enable inputs, all address inputs are grounded, and all outputs are open.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
t_{PLH} t_{PHL}	Propagation Delay, Negative Going $\overline{E}_R$ to Q Outputs		20 20	30 30	Figures 1	V_{CC} = 5.0 V C_L = 15 pF R_L = 2 KΩ	ns
t_{PLH} t_{PHL}	Propagation Delay, RA or R_B to Q Outputs		25 24	40 40	Figures 2		ns
t_{PLH} t_{PHL}	Propagation Delay, Negative Going $\overline{E}_W$ to Q Outputs		30 26	40 40	Figures 1		ns
t_{PLH} t_{PHL}	Propagation Delay, Data Inputs to Q Outputs		30 22	45 35	Figures 1		ns

AC SET-UP REQUIREMENTS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
t_W	Clock Pulse Width (LOW) for $\overline{E}_W$	25				ns
t_sD (Note 3)	Set-up Time, Data Inputs whith Respect to Positive-Going $\overline{E}_W$	10				ns
t_hD (Note 4)	Hold Time, Data Inputs whith Respect to Positive-Going $\overline{E}_W$	15			V_{CC} = 5.0 V	ns
t_sW (Note 5)	Set-up Time, Write Select Input W_A and W_B whith Respect to Positive-Going $\overline{E}_W$	15			Fig. 3	ns
t_hW (Note 4)	Hold Time, Write Select Input W_A and W_B whith Respect to Positive-Going $\overline{E}_W$	15				ns
t_{LATCH}	Latch Time	25				ns

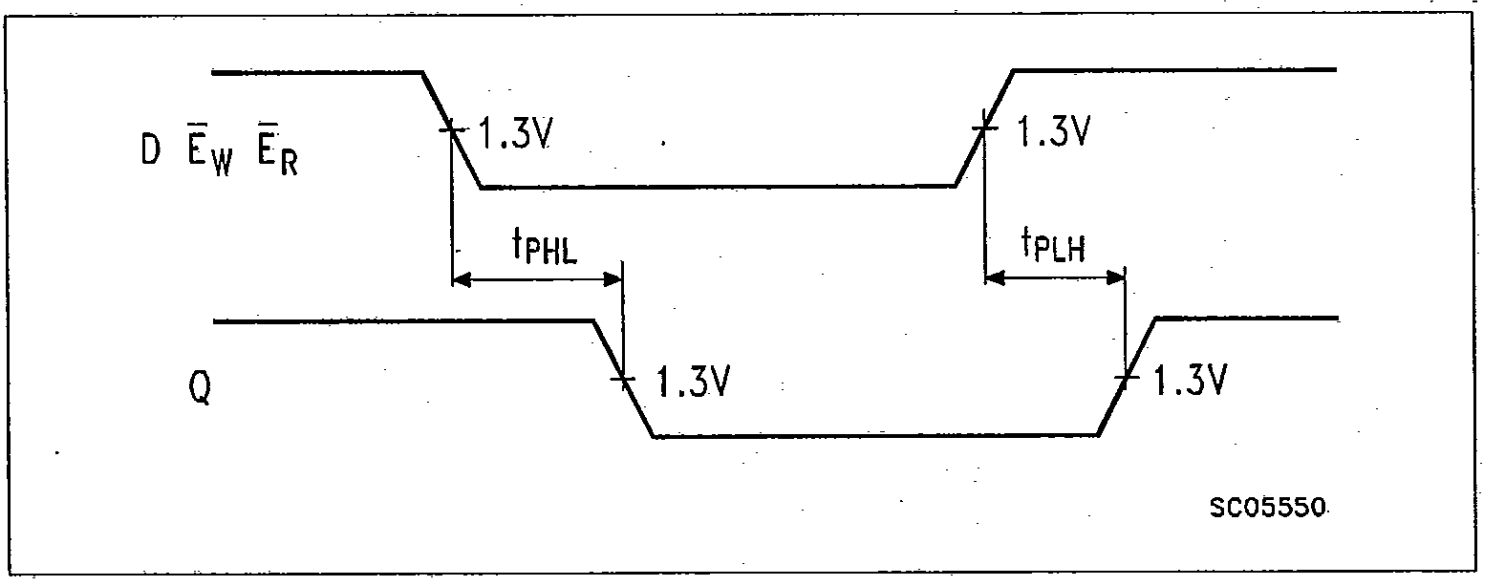
Notes: 3) The Data to Enable Set-up Time is defined as the time required for the logic level to be present at the Data input prior to the enable transition for LOW to HIGH in order from the latch to recognize and store the new data.

4) The Hold Time (th) is defined as the minimum time following the enable transition from LOW to HIGH that the logic level must be maintained at the input inorder toensure continued recognition.

5) The address to Enable Set-up Time is the time before the HIGH to LOW Enable transition the Address must be stable so that the crrect latch is addressed and the other latches are not affect.

AC WAVEFORM

Fig 1.



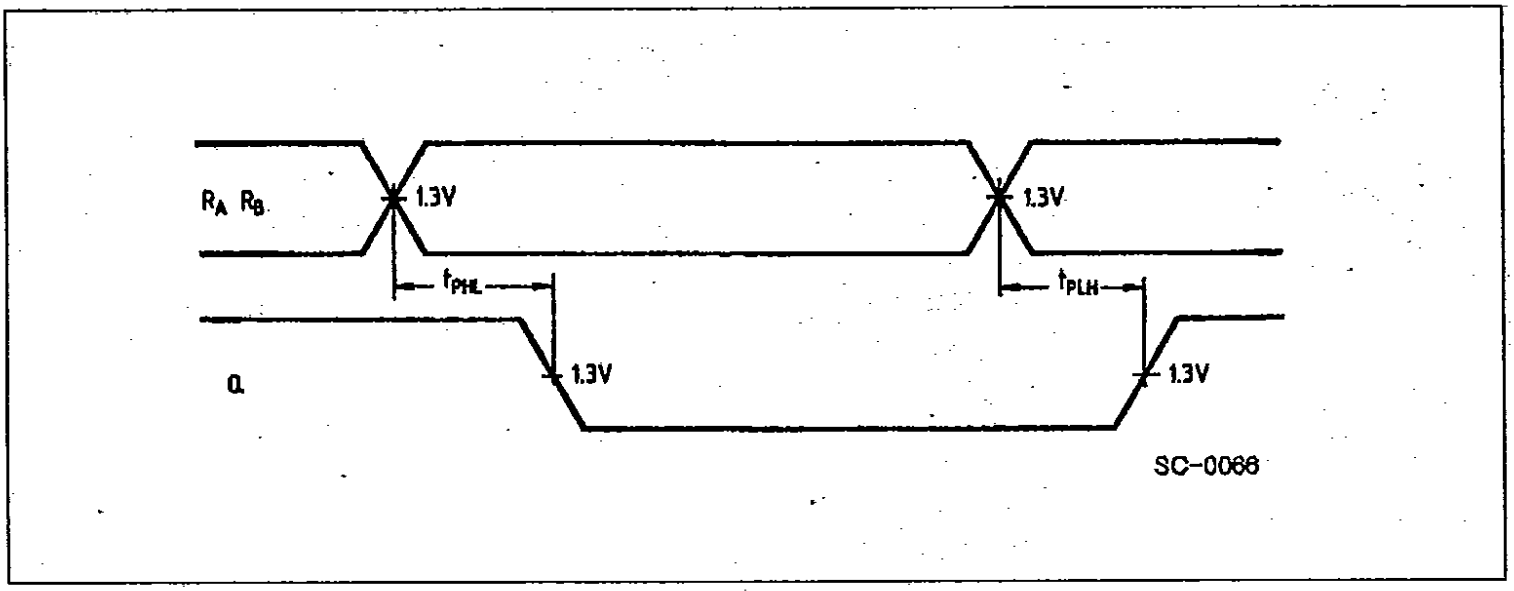
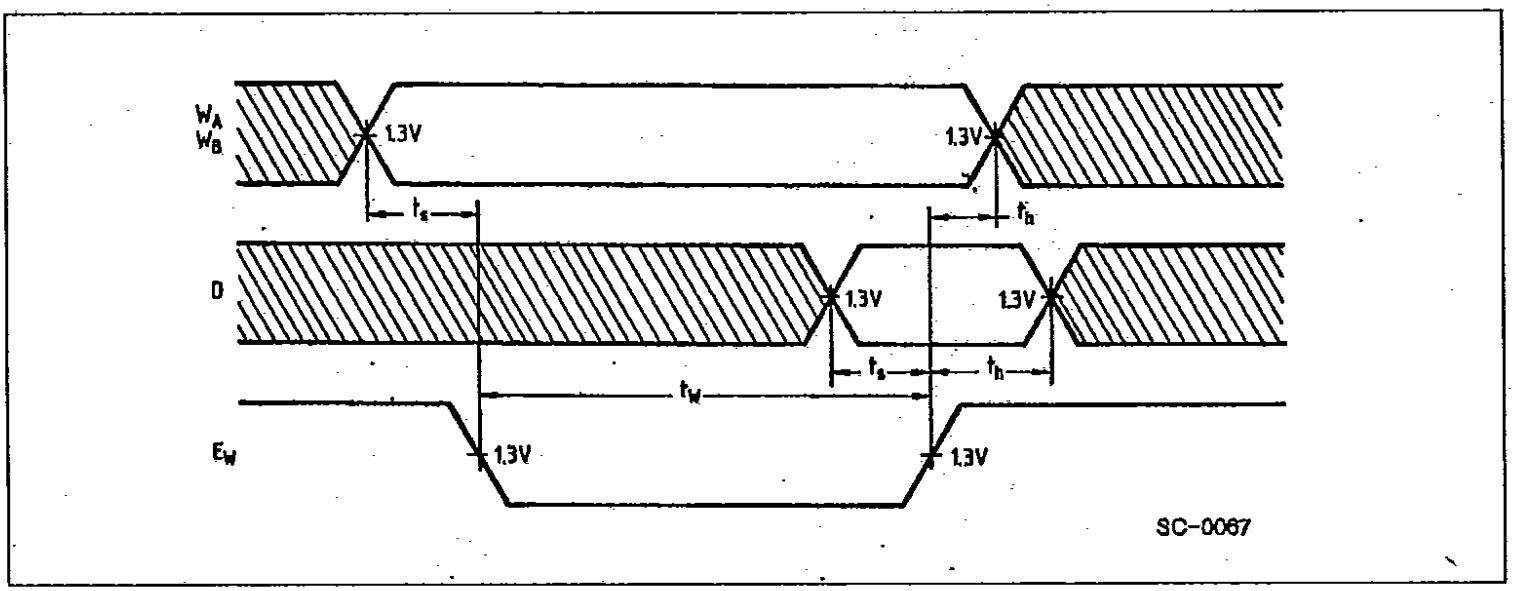


Fig 3.



The shaded areas indicate when the inputs are permitted to change for predictable output performance.