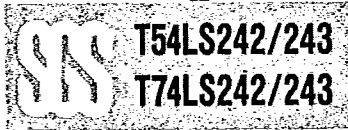


# LOW POWER SCHOTTKY INTEGRATED CIRCUITS



67C 16338

D T-52-31

PRELIMINARY DATA

## QUAD BUS TRANSCEIVER

### DESCRIPTION

T54LS/T74LS242/243 are high speed Quad Bus Transmitters/Receivers, intended for 4-line asynchronous 2-way data communications between data buses. Each device has one active high enable (E2) and one active low enable (E1). E2 enables the A outputs and E1 enables the B outputs.

- 2-WAY ASYNCHRONOUS DATA BUS COMMUNICATION
- HYSTERESIS AT INPUTS TO IMPROVE NOISE IMMUNITY
- INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS

**B1**  
Plastic Package

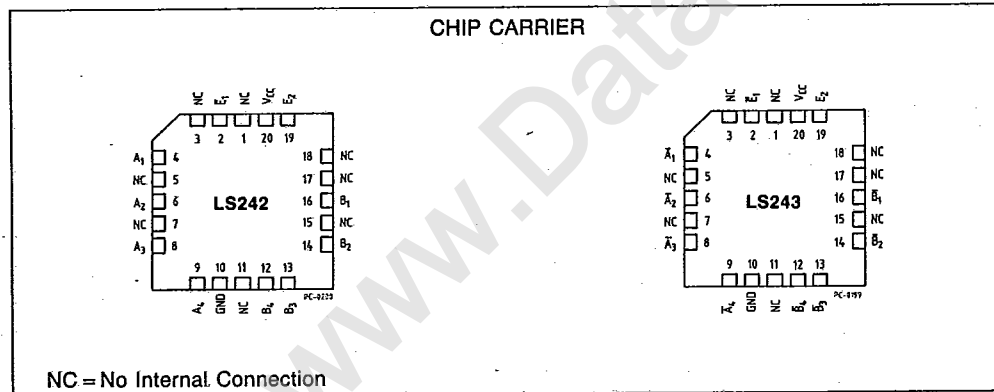
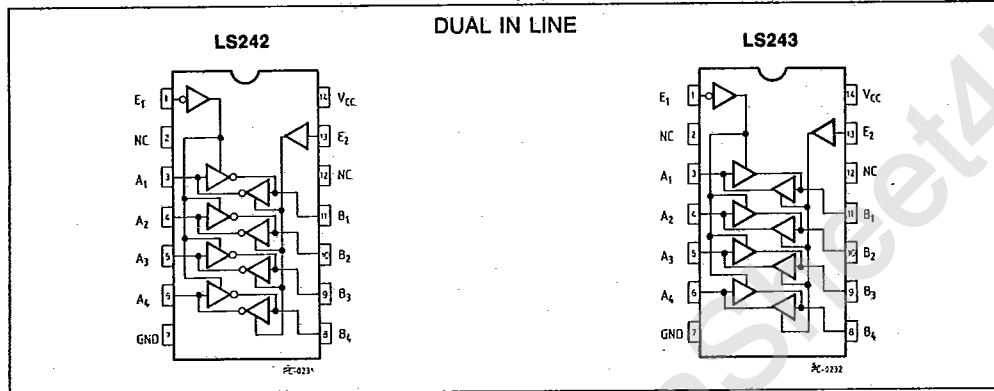
**D1/D2**  
Ceramic Package

**M1**  
Micro Package

**C1**  
Plastic Chip Carrier

ORDERING NUMBERS:  
T54LSXXX D2      T74LSXXX C1  
T74LSXXX D1      T74LSXXX M1  
T74LSXXX B1

## LOGIC AND CONNECTION DIAGRAMS DIP (top view)



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T54LS242/243  
 T74LS242/243

TRUTH TABLES

T54LS/74LS242						T54LS/74LS243					
INPUTS		OUTPUT	INPUTS		OUTPUT	INPUTS		OUTPUT	INPUTS		OUTPUT
E <sub>1</sub>	D		E <sub>2</sub>	D		E <sub>1</sub>	D		E <sub>2</sub>	D	
L	L	H	L	X	(Z)	L	L	L	L	X	(Z)
L	H	L	L	X	(Z)	L	H	H	L	X	(Z)
H	X	(Z)	H	L	H	H	X	(Z)	H	L	L
H	X	(Z)	H	H	L	H	X	(Z)	H	H	H

H=HIGH Voltage Level, L=LOW Voltage Level, X=Don't Care, Z=HIGH Impedance

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply Voltage	-0.5 to 7	V
V <sub>I</sub>	Input Voltage, Applied to Input	-0.5 to 15	V
V <sub>O</sub>	Output Voltage, Applied to Output	0 to 10	V
I <sub>I</sub>	Input Current, Into Inputs	-30 to 5	mA
I <sub>O</sub>	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS242/243D2	4.5 V	5.0 V	5.5 V	-55°C to +125°C
T74LS242/243XX	4.75 V	5.0 V	5.25 V	0°C to +70°C

XX=package type.



T54LS242/243

T74LS242/243

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

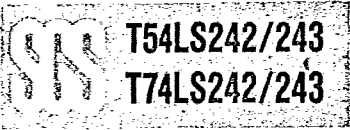
Symbol	Parameter	Limits			Test Conditions (Note 1)	Units	
		Min.	Typ.	Max.			
$V_{IH}$	Input HIGH Voltage	2.0			Guaranteed input HIGH Voltage for all Inputs	V	
$V_{IL}$	Input LOW Voltage	54		0.7	Guaranteed input LOW voltage for all Inputs	V	
		74		0.8			
$V_{T+}-V_{T-}$	Hysteresis	0.2	04		$V_{CC} = \text{MIN}$	V	
$V_{CD}$	Input Clamp Diode Voltage		-0.65	-1.5	$V_{CC} = \text{MIN}, I_{IN} = -18\text{mA}$	V	
$V_{OH}$	Output HIGH Voltage	54,74	2.4	3.4	$V_{CC} = \text{MIN}, I_{OH} = -3.0\text{mA}$	V	
		54	2.0		$I_{OH} = -12\text{mA}$		
		74	2.0		$I_{OH} = -15\text{mA}$		
$V_{OL}$	Output LOW Voltage	54,74	0.25	0.4	$I_{OL} = 4.0\text{mA}$	$V_{CC} = \text{MIN}, V_{IN} = V_{IL}$ or $V_{IH}$ per Truth Table	V
		74	0.35	0.5	$I_{OL} = 8.0\text{mA}$		
$I_{OZH}$	Output Off Current HIGH			40	$V_{CC} = \text{MAX}, V_{OUT} = 2.4\text{V}$	$\mu\text{A}$	
$I_{OZL}$	Output Off Current LOW			-200	$V_{CC} = \text{MAX}, V_{OUT} = 0.4\text{V}$	$\mu\text{A}$	
$I_{IH}$	Input HIGH Current D, E <sub>1</sub> , E <sub>2</sub> E <sub>1</sub> , E <sub>2</sub> D Input			40	$V_{CC} = \text{MAX}, V_{IN} = 2.7\text{V}$	$\mu\text{A}$ mA mA	
				0.1	$V_{CC} = \text{MAX}, V_{IN} = 7.0\text{V}$		
				0.1	$V_{CC} = \text{MAX}, V_{IN} = 5.5\text{V}$		
$I_{IL}$	Input LOW Current			-0.2	$V_{CC} = \text{MAX}, V_{IN} = 0.4\text{V}$	mA	
$I_{OS}$	Output Short Circuit Current (Note 2)	-40		-225	$V_{CC} = \text{MAX}$	mA	
$I_{CC}$	Power Supply Current Total, Output HIGH Total, Output LOW Total at HIGH Z			38	$V_{CC} = \text{MAX}$	mA	
				50			
		LS242 LS243		50 54			

AC CHARACTERISTICS: ( $T_A = 25^\circ\text{C}$ )

Symbol	Parameter	Limits						Test Conditions (Note 1)	Units
		LS242			LS243				
		Min.	Typ.	Max.	Min.	Typ.	Max.		
$t_{PLH}$	Propagation Delay, Data to Output		9	14		12	18	$C_L = 45\text{pF}$ $R_L = 667\Omega$	ns
$t_{PHL}$			12	18		12	18		
$t_{PZH}$	Output Enable Time to HIGH Level		15	23		15	23		ns
$t_{PZL}$	Output Enable Time to LOW Level		20	30		20	30		
$t_{PLZ}$	Output Disable Time From LOW Level		15	25		15	25		
$t_{PHZ}$	Output Disable Time from HIGH Level		10	18		10	18		

## Notes:

- 1) For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- 2) Not more than one output should be shorted at a time.
- 3) Typical Values are at  $V_{CC} = 5.0\text{V}, T_A = 25^\circ\text{C}$



AC WAVEFORMS

Fig. 1

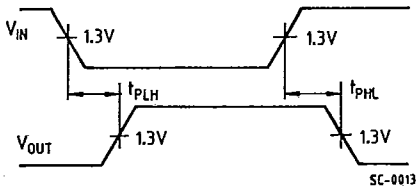


Fig. 2

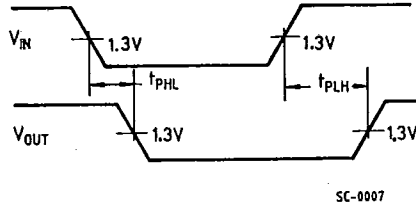


Fig. 3

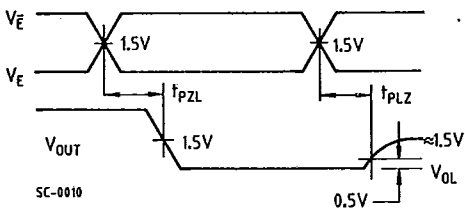


Fig. 4

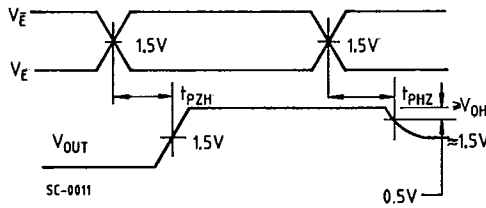
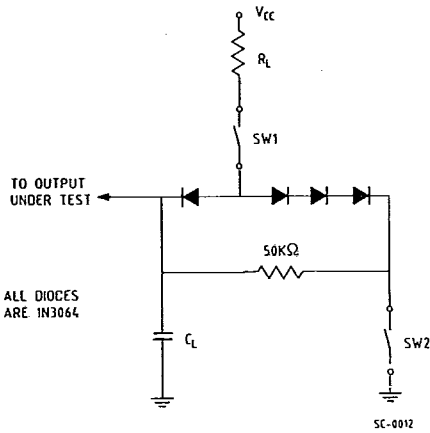


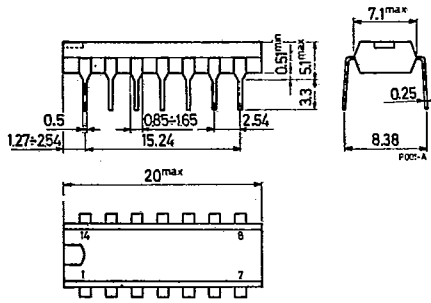
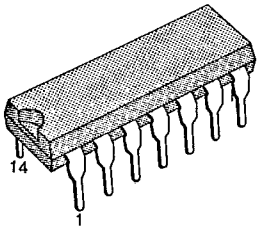
Fig. 5



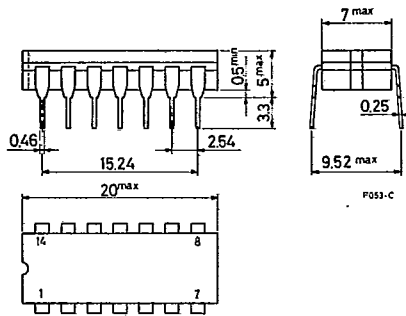
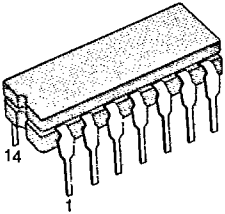
SWITCHING POSITIONS

Symbol	SW1	SW2
$t_{PZH}$	Open	Closed
$t_{PZL}$	Closed	Open
$t_{PLZ}$	Closed	Closed
$t_{PHZ}$	Closed	Closed

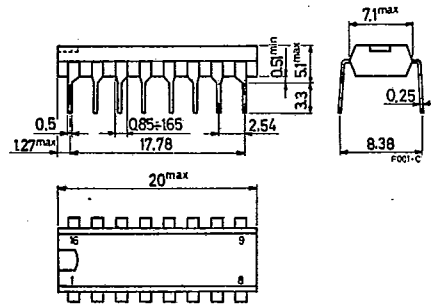
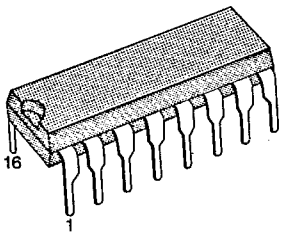
### 14-LEAD PLASTIC DIP



### 14-LEAD CERAMIC DIP



### 16-LEAD PLASTIC DIP



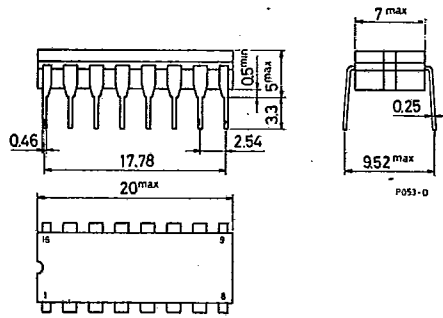
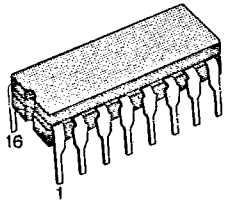
# Packages

67C 16545

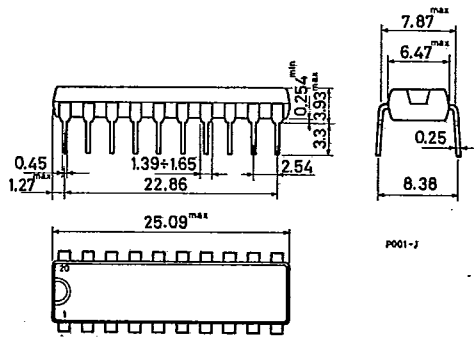
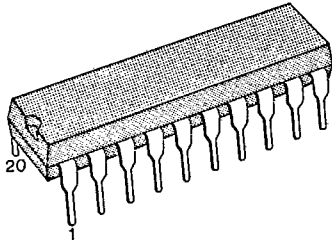
D

T-90-20

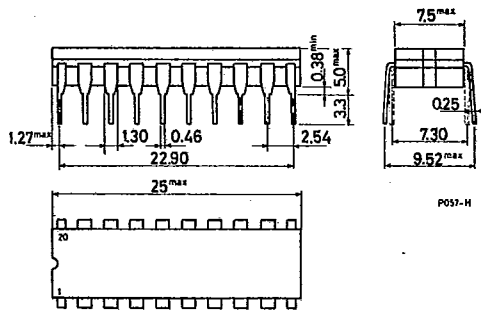
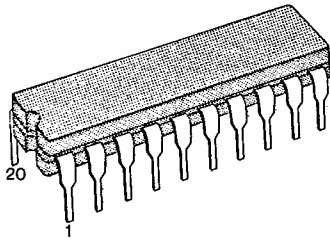
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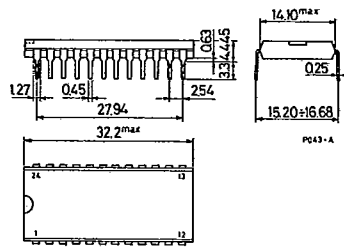
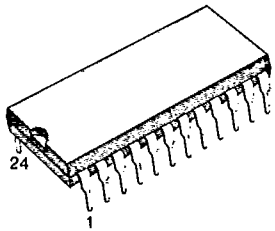
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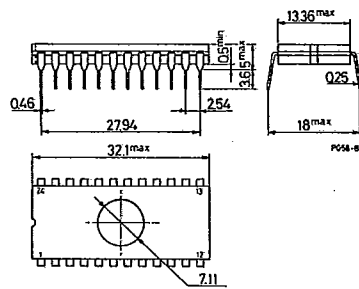
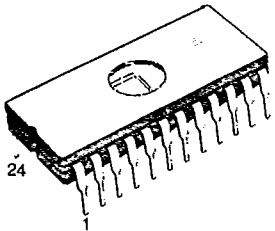
## 20-LEAD CERAMIC DIP



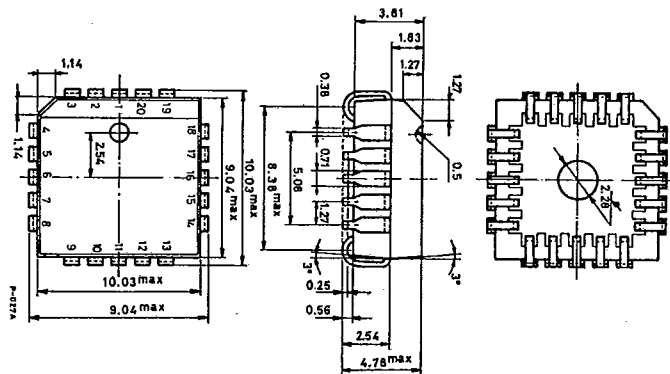
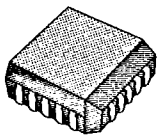
24-LEAD PLASTIC DIP



24-LEAD CERAMIC DIP



CHIP CARRIER 20 LEAD PLASTIC



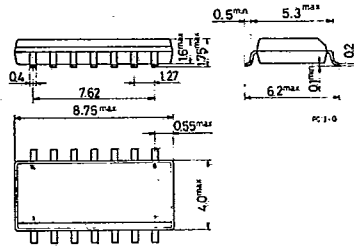
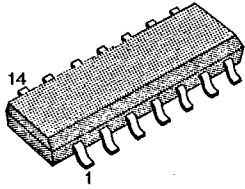
# Packages

67C 16547

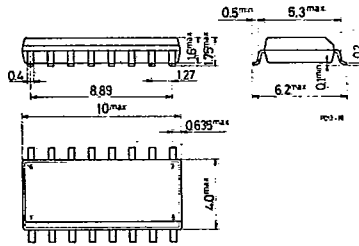
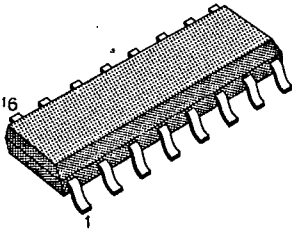
D

T-90-20

## 14-LEAD PLASTIC DIP MICROPACKAGE



## 16-LEAD PLASTIC DIP MICROPACKAGE



NOTE: FOR 20-LEAD PLASTIC DIP MICROPACKAGE CONTACT SGS



# Surface Mounted

67C 16548

D

T-90-20

One possible solution to the important problem of PWB minimization, is that of using surface mounted components. Integrated circuits in SO (Small Outline) packages are made up of standard chips mounted in very small plastic packages. The advantages given by using these devices are:

## PWB Reduction

This is by far the most important advantage since the reduction of PWB size varies from 40 to 60% in comparison with standard board types. (See page 584 for package dimensions.)

## Assembly Cost Reduction

SO Devices require no preliminary operation prior to mounting and can therefore be easily utilized in fully automatic equipment.

## Increasing Reliability

The following characteristics lead to a higher level of reliability with respect to their standard packaged counter parts:

- The mounting system is fully automatic
- PWB number and the interconnections between them are reduced when the same number of devices are used.
- The high density of components on the board makes it thermally much more stable.

## Noise Reduction and Improved Frequency Response

The reduction of the length of the connecting wires between the leads and the silicon guarantees a more homogeneous propagation delay between the external pins, with respect to the standard type.

## Assembly Without Board Holes

The devices are placed on the board and soldered. This technology permits a higher level of tolerance in the positioning (automatic) of the device. For the standard DIP types this must be done with great accuracy due to the insertion of the leads into their holes.

