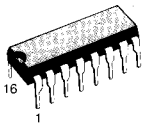
T54LS378
T74LS378

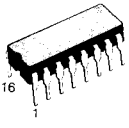
HEX PARALLEL D REGISTER WITH ENABLE

DESCRIPTION

The T54LS378/T74LS378 is an 6-Bit Register with a buffered common enable. This device is similar to the T54LS174/T74LS174, but with common Enable rather than common Master Reset.



B1
Plastic Package



D1/D2
Ceramic Package

M1
Micro Package

C1
Plastic Chip Carrier

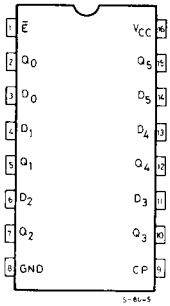
ORDERING NUMBERS:

T54LS378 D2	T74LS378 C1
T74LS378 D1	T74LS378 M1
T74LS378 B1	

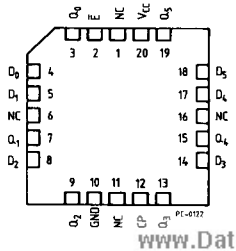
- 8-BIT HIGH SPEED PARALLEL REGISTER
- POSITIVE EDGE-TRIGGERED D-TYPE FLIP-FLOPS
- FULLY BUFFERED COMMON CLOCK AND ENABLE INPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

PIN CONNECTION
(top view)

DUAL IN LINE



CHIP CARRIER

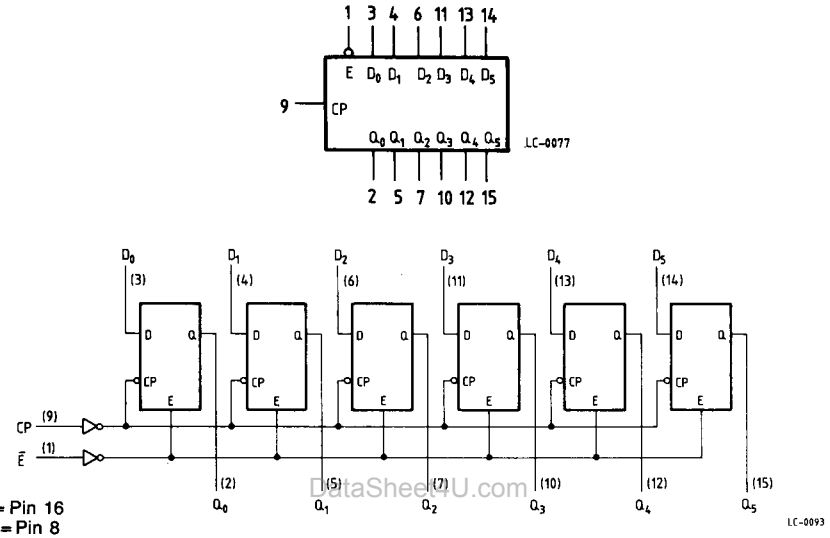


NC = No Internal Connection

PIN NAMES

$\overline{E}$	Enable (Active LOW) Input
D_0-D_5	Data Inputs
CP	Clock (Active HIGH Going Edge) Input
Q_0-Q_5	True Outputs

LOGIC SYMBOL AND LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	Input Voltage, Applied to Input	−0.5 to 15	V
V_O	Output Voltage, Applied to Output	−0.5 to 10	V
I_I	Input Current, Into Inputs	−30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS378D2	4.5 V	5.0 V	5.5 V	−55°C to +125°C
T74LS8378XX	4.75 V	5.0 V	5.25 V	0°C to +70°C

XX = package type.

FUNCTIONAL DESCRIPTION

The LS378 consists of eight edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable ($\overline{E}$) input are common to all flip-flops.

When $\overline{E}$ input is LOW, new data is entered into the register on the LOW-to-HIGH transition of CP input. When the $\overline{E}$ input is HIGH the register will retain the present data independent of the CP input.

TRUTH TABLE

$\overline{E}$	CP	D_n	Q_n
H	⌐	X	No Charge
L	⌐	H	H
L	⌐	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Test Conditions (Note 1)	Units
V_{IH}	Input HIGH Voltage		2.0			Guaranteed input HIGH Voltage for all Inputs	V
V_{IL}	Input LOW Voltage	54			0.7	Guaranteed input LOW Voltage for all Inputs	V
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V_{CC} = MIN, I_{IN} = −18mA	V
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V_{CC} = MIN, I_{OH} = −400μA, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	I_{OL} = 4.0mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74		0.35	0.5	I_{OL} = 8.0mA	
I_{IH}	Input HIGH Current				20 0.1	V_{CC} = MAX, V_{IN} = 2.7V V_{CC} = MAX, V_{IN} = 7.0V	μA mA
I_{IL}	Input LOW Current				−0.4	V_{CC} = MAX, V_{IN} = 0.4V	mA
I_{OS}	Output Short Circuit Current (Note 2)		−20		−100	V_{CC} = MAX, V_{OUT} = 0V	mA
I_{CC}	Power Supply Current			16	27	V_{CC} = MAX	mA

Notes:
1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2) Not more than one output should be shorted at a time.
3) Typical values are at V_{CC} = 5.0V, T_A = 25°C

AC CHARACTERISTICS: $T_A = 25°C$

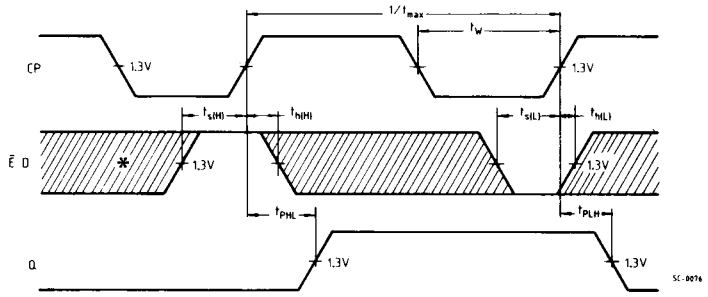
Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
f_{MAX}	Minimum Input Clock Frequency	30	40		Fig. 1	$V_{CC} = 5.0V$	MHz
t_{PLH}	CP to Q Output		17	27	Fig. 1		ns
t_{PHL}	CP to Q Output		18	27	Fig. 1		ns

AC SET-UP REQUIREMENTS: $T_A = 25°C$

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
t_s	Set-up Time, Data to Clock (HIGH or LOW)	20			Fig. 1	$V_{CC} = 5.0V$	ns
t_h	Hold Time, Data to Clock (HIGH or LOW)	5			Fig. 1		ns
t_s	Set-up Time, Enable to Clock (HIGH or LOW)	30			Fig. 1		ns
t_h	Hold Time, Enable to Clock (HIGH or LOW)	5			Fig. 1		ns
t_{wCP}	Minimum Clock Pulse Width	20					ns

AC WAVEFORMS

Fig. 1 - Clock to Output Delays, Clock Pulse Width, Frequency, Set-up and Hold Times Data, Enable to Clock



* The shaded areas indicate when the input is permitted to change for predictable output performance

DEFINITION OF TERMS:

SET-UP TIME (t_s) - is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) - is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.