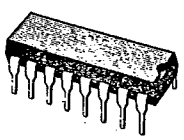
SGS-THOMSON MICROELECTRONICS

T74LS490

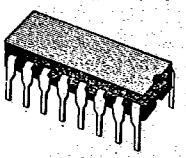
T-45-23-13

DUAL DECADE COUNTER

- DUAL VERSION OF 74LS90
- INDIVIDUAL ASYNCHRONOUS CLEAR AND PRESET TO 9 FOR EACH COUNTER
- COUNT FREQUENCY - TYPICALLY 35 MHz
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- TTL AND CMOS COMPATIBLE



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

T74LS490 D1
T74LS490 B1
T74LS490 C1
T74LS490 M1

DESCRIPTION

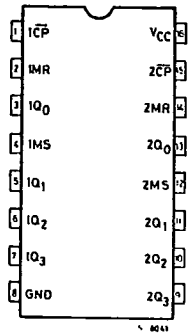
The T74LS490 contains a pair of high-speed 4-stage ripple counters. Each half of the T74LS490 has individual Clock, Master Reset and Master Set (Preset 9) inputs. Each section counts in 8, 4, 2, 1 BCD code.

PIN NAMES

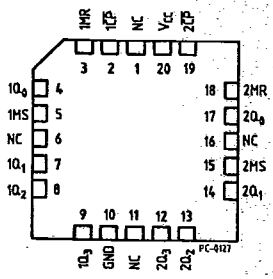
MS	MASTER SET (set to 9) INPUT
MR	MASTER RESET
CP	CLOCK INPUT (active HIGH going edge)
Q_0-Q_3	COUNTER OUTPUTS

PIN CONNECTION (top view)

DUAL IN LINE

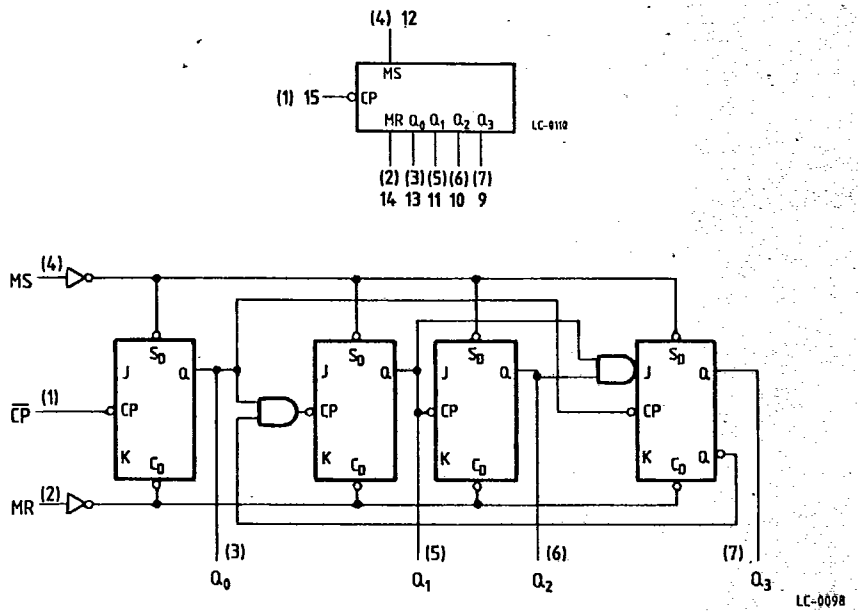


CHIP CARRIER



NC = No Internal Connection

LOGIC SYMBOL AND LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	− 0.5 to 7	V
V_I	Input Voltage, Applied to Input	− 0.5 to 5.5	V
V_O	Output Voltage, Applied to Output	− 0.5 to 10	V
I_I	Input Current, into Inputs	− 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only oand functional operation to the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS490XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = Package type.

TRUTH TABLE

Count	Outputs			
	Q3	Q2	Q1	Q0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits			Test Condition (note 1)		Unit
			Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage		2.0			Guaranteed Input HIGH Voltage for All Inputs		V
V_{IL}	Input LOW Voltage				0.8	Guaranteed Input LOW Voltage for All Inputs		V
V_{CD}	Input Clamp Diode Voltage			- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage		2.7			V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage			0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
				0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current	MR, MS			20	V_{CC} = MAX, V_{IN} = 2.7 V		µA
		$\overline{CP}$			60			
		$\overline{CP}$			- 300	V_{CC} = MAX, V_{IN} = 7.0 V V_{IN} = 5.5 V CP Only		µA
		MR, MS			100			
I_{IL}	Input LOW Current	$\overline{CP}$			- 2.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
		MR, MS			- 0.4			
I_{OS}	Output Short Circuit Current (note 2)		- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current			19	30	V_{CC} = MAX		mA

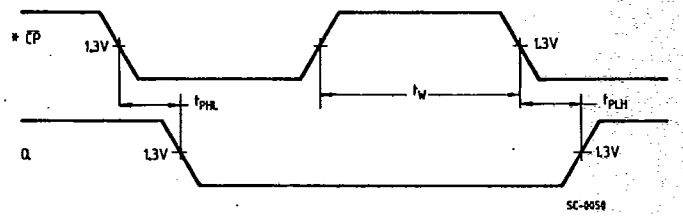
Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating conditions for the device type.
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS : $T_A = 25\ °C$

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Test Conditions		Unit
f_{MAX}	Maximum Input Count Frequency		25	35		Fig. 1	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ $R_L = 2\ k\Omega$	MHz
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}$ to Q_0			12 13	20 20	Fig. 1		ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}$ to Q_1 or Q_3			24 26	39 39	Fig. 3		ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}$ to Q_2			32 36	54 54	Fig. 2		ns
t_{PHL}	Propagation Delay, MR to Output			24	39	Fig. 2		ns
t_{PLH} t_{PHL}	Propagation Delay, MS to Output	Q_0, Q_3		24	39	Fig. 2		ns
		Q_1, Q_2		20	36			

AC WAVEFORMS

Figure 1.



The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the Truth Table.

Figure 2.

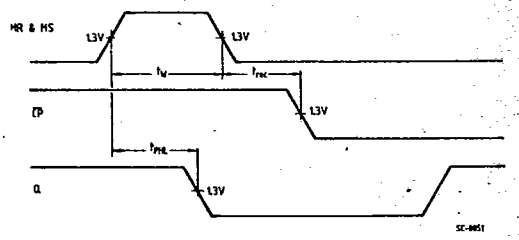


Figure 3.