

## 4-BIT SHIFT REGISTER

### DESCRIPTION

The T54LS95B/T74LS95B is a 4-Bit Shift Register with serial and parallel synchronous operating modes. The serial shift right and parallel load are activated by separate clock inputs which are selected by a mode control input. The data is transferred from the serial or parallel D inputs to the Q outputs synchronous with the HIGH to LOW transition of the appropriate clock input.

The LS95B is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all SGS TTL families.

- SYNCHRONOUS, EXPANDABLE SHIFT RIGHT
- SYNCHRONOUS, SHIFT LEFT CAPABILITY
- SYNCHRONOUS, PARALLEL LOAD
- SEPARATE SHIFT AND LOAD CLOCK INPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

### PIN NAMES

S	Mode Control Input
D <sub>S</sub>	Serial Data Input
P <sub>0</sub> -P <sub>3</sub>	Parallel Data Inputs
$\overline{CP}_1$	Serial Clock (Active LOW Going Edge) Input
$\overline{CP}_2$	Parallel Clock (Active LOW Going Edge) Input
Q <sub>0</sub> -Q <sub>3</sub>	Parallel Outputs

**B1**  
Plastic Package

**D1/D2**  
Ceramic Package

**M1**  
Micro Package

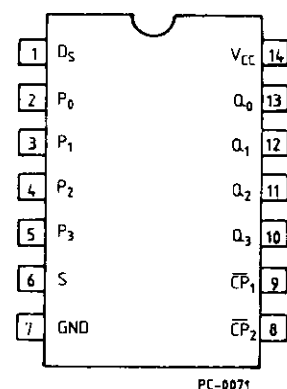
**C1**  
Plastic Chip Carrier

**ORDERING NUMBERS:**

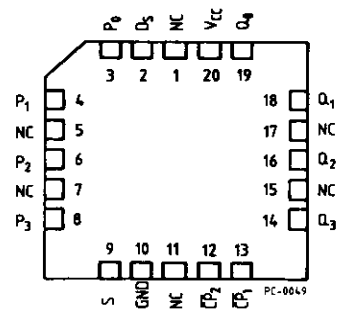
T54LS95B D2	T74LS95B C1
T74LS95B D1	T74LS95B M1
T74LS95B B1	

### PIN CONNECTION (top view)

#### DUAL IN LINE

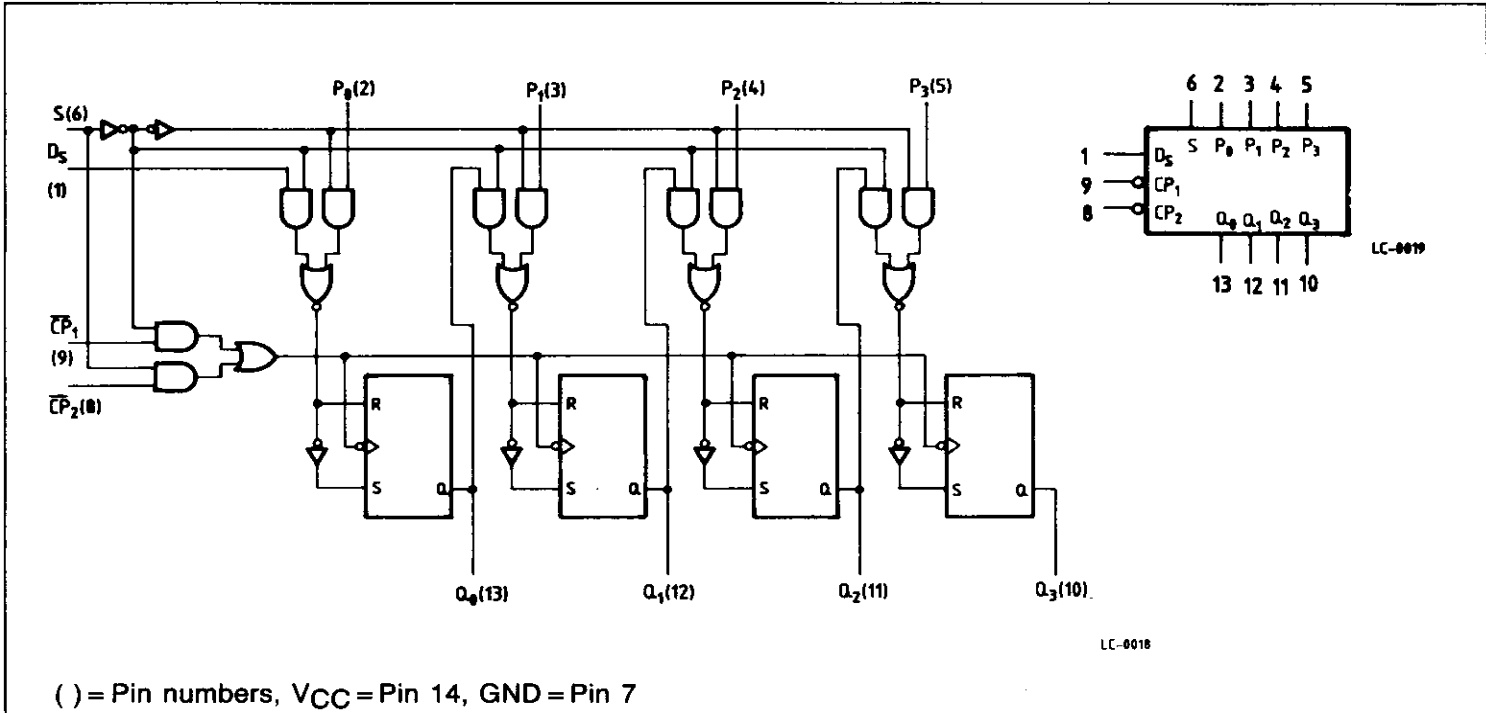


#### CHIP CARRIER



NC = No Internal Connection

### LOGIC DIAGRAM AND LOGIC SIMBOL



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	-0.5 to 7	V
$V_I$	Input Voltage, Applied to Input	-0.5 to 15	V
$V_O$	Output Voltage, Applied to Output	-0.5 to 10	V
$I_I$	Input Current, Into Inputs	-30 to 5	mA
$I_O$	Output Current, Into Outputs	60	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS95BD2	4.5 V	5.0 V	5.5 V	-55°C to +125°C
T74LS95BXX	4.75 V	5.0 V	5.25 V	0°C to +70°C

XX = package type.

**T54LS95B**  
**T74LS95B**

**TRUTH TABLE**

OPERATING MODE	INPUTS					OUTPUTS			
	S	$\overline{CP}_1$	$\overline{CP}_2$	D <sub>S</sub>	P <sub>n</sub>	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>
Shift	L		X	l	X	L	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>
	L		X	h	X	H	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>
Parallel Load	H	X		X	P <sub>n</sub>	P <sub>0</sub>	P <sub>1</sub>	P <sub>2</sub>	P <sub>3</sub>
Mode Change		L	L	X	X	No Change			
		L	L	X	X	No Change			
		H	L	X	X	No Change			
		H	L	X	X	Undetermined			
		L	H	X	X	Undetermined			
		L	H	X	X	No Change			
		H	H	X	X	Undetermined			
		H	H	X	X	No Change			

L = LOW Voltage Level

H = HIGH Voltage Level

X = Don't Care

l = LOW Voltage Level one set-up time prior to the HIGH to LOW clock transition.

h = HIGH Voltage Level one set-up time prior to the HIGH to LOW clock transition.

P<sub>n</sub> = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock Transition

**FUNCTIONAL DESCRIPTION**

The LS95B is a 4-Bit Shift Register with serial and parallel synchronous operating modes. It has a Serial (D<sub>S</sub>) and four Parallel (P<sub>0</sub>-P<sub>3</sub>) Data inputs and four Parallel Data outputs (Q<sub>0</sub>-Q<sub>3</sub>). The serial or parallel mode of operation is controlled by a Mode Control input (S) and two Clock inputs ( $\overline{CP}_1$ ) and ( $\overline{CP}_2$ ). The serial (right-shift) or parallel data transfers occur synchronous with the HIGH to LOW transition of the selected clock input.

When the Mode Control input (S) is HIGH,  $\overline{CP}_2$  is enabled. A HIGH to LOW transition on enabled  $\overline{CP}_2$  transfers parallel data from the P<sub>0</sub>-P<sub>3</sub> inputs to the Q<sub>0</sub>-Q<sub>3</sub> outputs.

When the Mode Control input (S) is LOW,  $\overline{CP}_1$  is

enable. A HIGH to LOW transition on enabled  $\overline{CP}_1$  transfers the data from serial input (D<sub>S</sub>) to Q<sub>0</sub> and shifts the data in Q<sub>0</sub> to Q<sub>1</sub>, Q<sub>1</sub> to Q<sub>2</sub>, and Q<sub>2</sub> to Q<sub>3</sub> respectively (right-shift). A left-shift is accomplished by externally connecting Q<sub>3</sub> to P<sub>2</sub>, Q<sub>2</sub> to P<sub>1</sub>, and Q<sub>1</sub> to P<sub>0</sub>, and operating the LS95B in the parallel mode (S = HIGH).

For normal operation, S should only change states when both Clock inputs are LOW. However, changing S from LOW to HIGH while  $\overline{CP}_2$  is HIGH, or changing S from HIGH to LOW while  $\overline{CP}_1$  is HIGH and  $\overline{CP}_2$  is LOW will not cause any changes on the register outputs.

### DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits			Test Conditions (Note 1)	Units	
			Min.	Typ.	Max.			
$V_{IH}$	Input HIGH Voltage		2.0			Guaranteed input HIGH Threshold Voltage for all Inputs	V	
$V_{IL}$	Input LOW Voltage	54			0.7	Guaranteed input LOW Threshold Voltage for all Inputs	V	
		74			0.8			
$V_{CD}$	Input Clamp Diode Voltage			-0.65	-1.5	$V_{CC} = \text{MIN}, I_{IN} = -18\text{mA}$	V	
$V_{OH}$	Output HIGH Voltage	54	2.5	3.4		$V_{CC} = \text{MIN}, I_{OH} = -400\mu\text{A}, V_{IN} = V_{IH}$ or $V_{IL}$ per Truth Table	V	
		74	2.7	3.4				
$V_{OL}$	Output LOW Voltage	54,74		0.25	0.4	$I_{OL} = 4.0\text{mA}$	$V_{CC} = \text{MIN}, V_{IN} = V_{IH}$ or $V_{IL}$ per Truth Table	V
		74		0.35	0.5	$I_{OL} = 8.0\text{mA}$		
$I_{IH}$	Input HIGH Current $D_S, P_0, P_1, P_2, P_3, \overline{CP}_1, \overline{CP}_2$ S				20 40	$V_{CC} = \text{MAX}, V_{IN} = 2.7\text{V}$	$\mu\text{A}$	
	$D_S, P_0, P_1, P_2, P_3, \overline{CP}_1, \overline{CP}_2$ S				0.1 0.2	$V_{CC} = \text{MAX}, V_{IN} = 7.0\text{V}$	mA	
$I_{IL}$	Input LOW Current $D_S, P_0, P_1, P_2, P_3, \overline{CP}_1, \overline{CP}_2$ S				-0.4 -0.8	$V_{CC} = \text{MAX}, V_{IN} = 0.4\text{V}$	mA	
$I_{OS}$	Output Short Circuit Current (Note 2)		-20		-100	$V_{CC} = \text{MAX}, V_{OUT} = 0\text{V}$	mA	
$I_{CC}$	Power Supply Current			13	21	$V_{CC} = \text{MAX}$	mA	

### AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$

Symbol	Parameter		Limits			Test Conditions	Units
			Min.	Typ.	Max.		
$f_{MAX}$	Shift Frequency		25	36		Fig. 1	MHz ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay, Clock to Output			18 21	27 32	Fig. 2	
						$V_{CC} = 5.0\text{V}$ $C_L = 15\text{pF}$	

#### Notes:

- 1) For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- 2) Not more than one output should be shorted at a time.
- 3) Typical values are at  $V_{CC} = 5.0\text{V}, T_A = 25^\circ\text{C}$

**AC SET-UP REQUIREMENTS:  $T_A = 25^\circ\text{C}$** 

Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
$t_w(\text{CP})$	Clock Pulse Width	25			Fig. 1	ns
$t_s(\text{Data})$	Set-up Time, Data to Clock	20			Fig. 1	ns
$t_h(\text{Data})$	Hold Time, Data to Clock	20				ns
$t_{sL}$	Set-up Time LOW Mode Control to Clock	20			Fig. 1	ns
$t_{hL}$	Hold Time, LOW Mode Control to Clock	0				ns
$t_{sH}$	Set-up Time, HIGH Mode Control to Clock	20			Fig. 1	ns
$t_{hH}$	Hold Time, HIGH Mode Control to Clock	0				ns

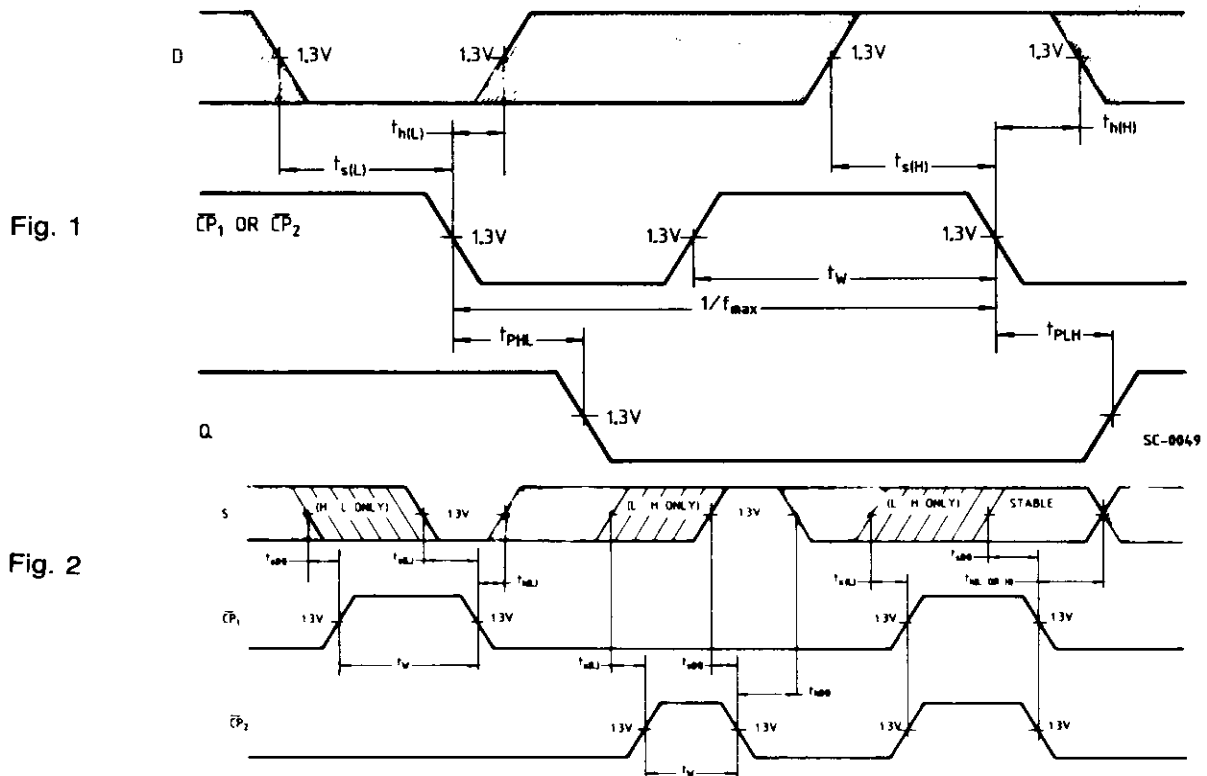
$V_{CC} = 5.0\text{V}$   
 $C_L = 15\text{pF}$

**SET-UP TIME ( $t_s$ )** - is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the output.

**HOLD TIME ( $t_h$ )** - is defined as the minimum time following the clock transition from HIGH to LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be relaxed prior to the clock transition from HIGH to LOW and still be recognized.

**AC WAVEFORMS**

The shaded areas indicate when the input is permitted to change for predictable output performance.



\* The Data Input is ( $D_S$  for  $\overline{CP}_1$ ) or ( $P_n$  for  $\overline{CP}_2$ ).