agere systems

Product Brief
June 2001

Ambassador ® T8105
H.100/H.110 Interface and Time-Slot Interchanger

Introduction

The Agere Systems Inc. *Ambassador* T8105 device provides a complete solution for time-slot switching and interconnect for the H.100/H.110 time-division multiplexed (TDM) buses. It is fully backwards compatible to the T8100A and T8102 devices. The T8105 device provides hierarchical switching as well as a capacity of up to 512 local to H.100/H.110 connections. The hierarchical switching allows up to 1024 local connections without using H.100/H.110 bus bandwidth. Local interfaces include sixteen serial inputs and sixteen serial outputs and the H-bus interface includes 32 bidirectional H.100/H.110 streams. The T8105 bus interface is compatible with the *MVIP**-90, H-*MVIP*, SC-Bus, and ECTF H.100/H.110 bus standards. The *Ambassador* T8105 is configured via a microprocessor interface which can also read and write time-slot and device data. Packaged in both a 208-pin SQFP and a 217-ball BGA, the *Ambassador* T8105 TSI device can provide an economic solution for the computer telephony market.

Features

- Fully compatible to the T8100, T8100A, and T8102.
- H.100/H.110 compliant interface; all mandatory signals.
- Programmable connections to any of the 4096 time slots on the H.100/H.110 bus.
- Programmable switching between local time slots and H.100/H.110 bus, up to 512 connections.
- Programmable switching between local time slots, up to 1024 connections.
- Up to 16 local serial inputs and 16 local serial outputs, (2, 4, and 8 Mbits/s).
- Microprocessor interface: *Intel*†/*Motorola*‡ modes.
- Choice of frame integrity or minimum latency switching on a per-time-slot basis:
  — Frame integrity to ensure proper switching of wideband data.
  — Minimum latency switching to reduce delay in voice channels.
- Subrate switching of 1 bit, 2 bits, and 4 bits.
- Two independently programmable groups of up to 12 framing signals each.
- Programmable GPIO.
- On-chip phase-locked loop (PLL) for H.100/H.110, *MVIP*, or *Dialogic's*§ SC-bus clock operation in master or slave clock modes.
- Serial TDM bus rate and format conversion between most standard buses.
- Optional 8-bit parallel input and/or 8-bit parallel output for local TDM interfaces.
- Includes 2 CT_NETREF pins.
- Stratum 4/4E and AT&T 62411 MTIE compliant.
- 3.3 V supply with 5 V tolerant inputs and TTL-compatible outputs.
- JTAG/boundary-scan testing support.
- 208-pin, plastic SQFP package and 217-ball PBGA package (industrial temperature range).
- Evaluation boards available—PCI and *CompactPCI*** hot swap.

Applications

- Computer telephony integrated solutions
- Enhanced service platforms
- WAN access devices
- Telephony servers
- PBXs
- Wireless base station controllers

Refer to website www.agere.com/ambassador for additional information.

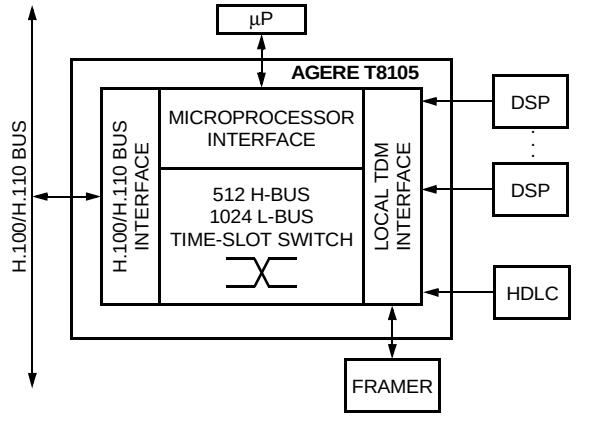

Figure 1. Basic Application of the T8105 as an H.100/H.110 to Local TDM CT Switch

* *MVIP* is a trademark of Natural MicroSystems Corporation.
† *Intel* is a registered trademark of Intel Corporation.
‡ *Motorola* is a registered trademark of Motorola Inc.
§ *Dialogic* is a registered trademark of Dialogic Corporation.
** *CompactPCI* is a registered trademark of the PCI Industrial Computer Manufacturers Group.

T8105 Block Diagram

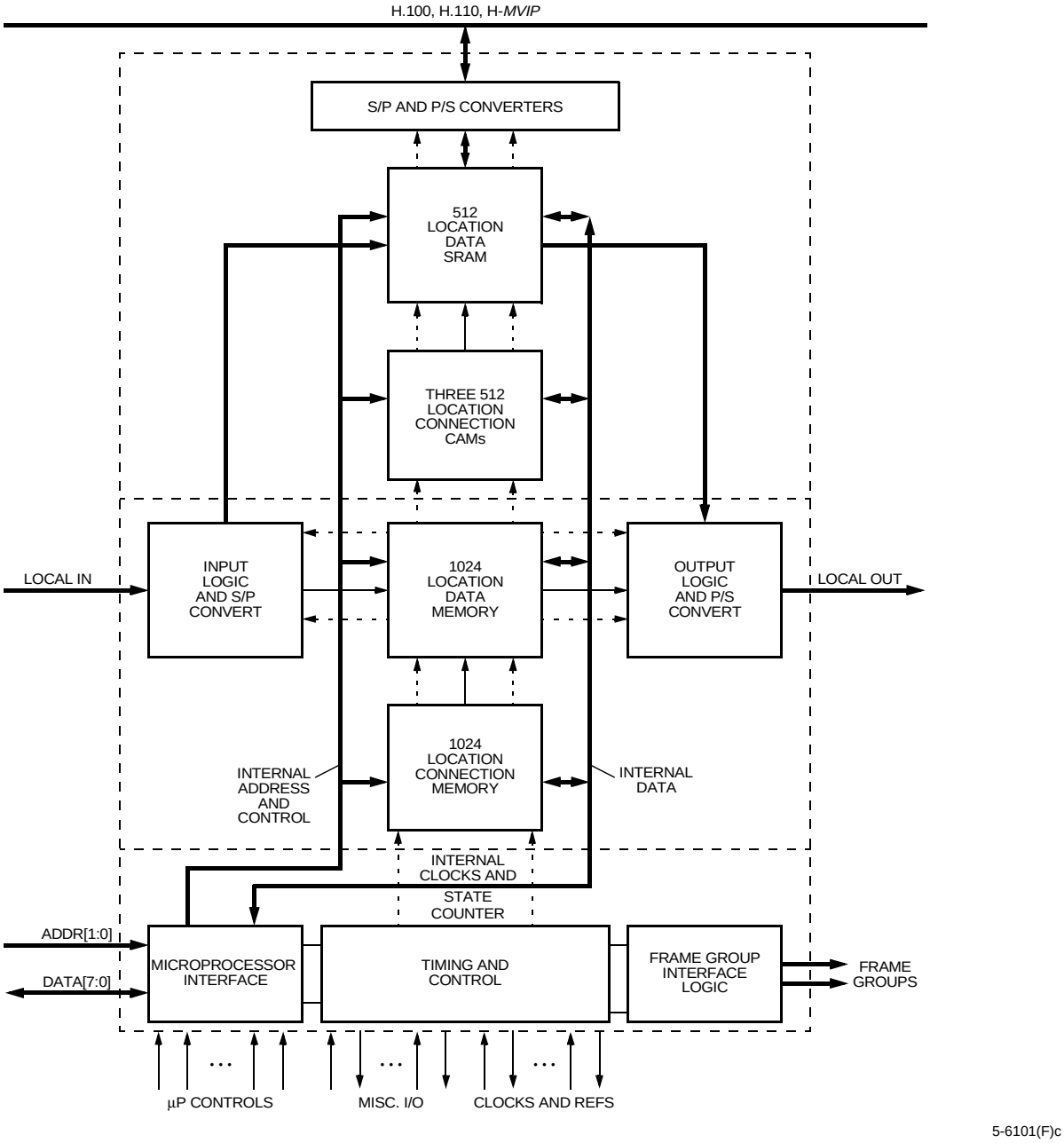

Figure 2. Block Diagram of the *Ambassador*

Subrate switching is the ability to switch part(s) of one byte from one stream/time slot to another stream/time slot. The parts are the following:

- Nibbles (4 bits)—representing a 32 kbits/s subrate
- Dibits (2 bits)—representing a 16 kbits/s subrate
- Bits—representing an 8 kbits/s subrate

H.100/H.110 data transfers are always bytes. If subrate switching is used, the T8105 constructs a byte consisting of the subrate samples. The constructed byte may contain any combination of nibbles, dibits, or bits. In addition, individual data bits can be placed within a byte along with don't care bits.

Onboard clock circuitry, including a digital phase-locked loop, supports all H.100/H.110 clock modes including *MVIP* and SC-bus compatibility clocks. The local CHI supports PCM rates of 2.048 Mbits/s, 4.096 Mbits/s, and 8.192 Mbits/s. The *Ambassador* T8105 has internal circuitry to support either minimum latency or multi-time-slot frame integrity. Frame integrity is a requisite feature for applications that switch wideband data (ISDN H-channels). Minimum latency is advantageous in voice applications.

Application Overview

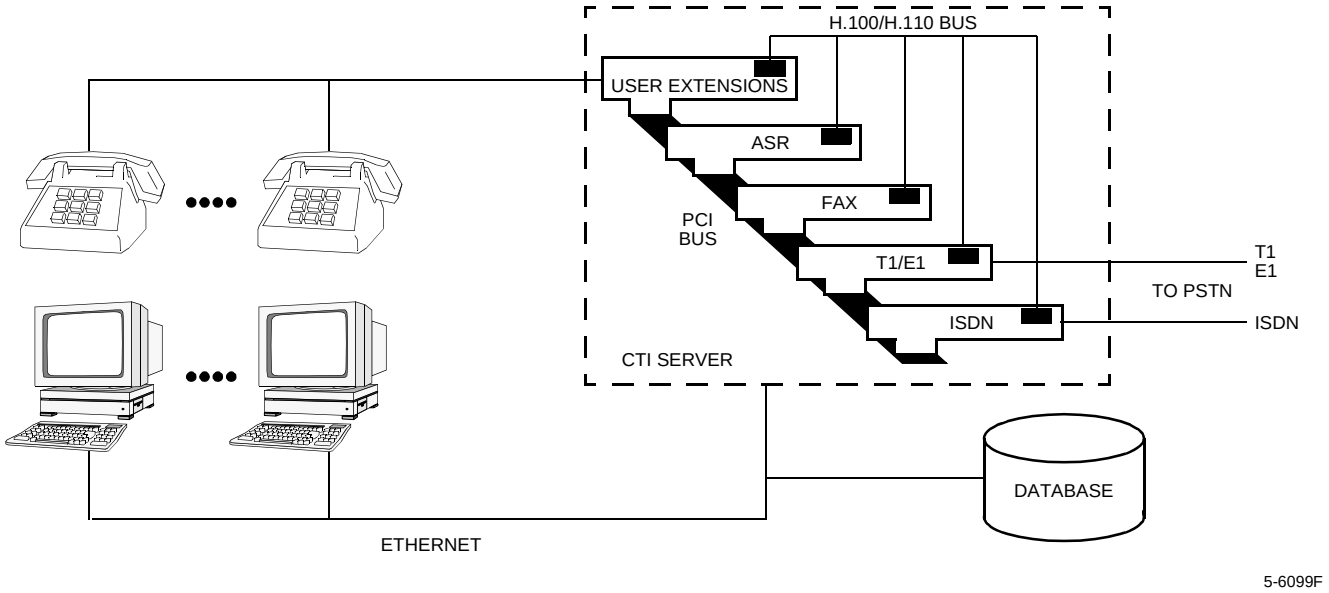

Figure 3. CTI Call Center Application

The integration of computers and telecommunications has enabled a wide range of new communications applications and has fueled an enormous growth in communications markets. A key element in the development of computer-based communications equipment has been the addition of an auxiliary telecom bus to existing computer systems. Most manufacturers of high-capacity, computer-based telecommunications equipment have incorporated some such telecom bus in their systems. Typically, these buses and bus interfaces are designed to transport and switch Nx64 kbits/s low-latency telecom traffic between boards within the computer, independent of the computer's I/O and memory buses. At least a half dozen of these PC-based telecom buses emerged in the early 1990s for use within equipment based on ISA/EISA and MCA computers.

With the advent of the H.100/H.110 bus specification by the Enterprise Computer Telephony Forum (www.ectf.org), the computer-telephony industry has agreed on a single telecom bus for use with PCI and compact PCI computers. H.100/H.110 facilitates interoperation of components, thus providing maximum flexibility to equipment manufacturers, value-added resellers, system integrators, and others building computer-based telecommunications applications.

Ambassador Selection Guide

	Ambassador **Products**				
Features	**T8100A**	**T8102**	**T8105**	**T8110**	**T8150**
Number of Connections:					
Local to local	1024	*	1024	4096	4096
Local to H-bus	256	512	512		
Number of Local Data I/O	16I/16O	16I/16O	16I/16O	32 I/O	32 I/O
Local Data Rates Supported	2, 4, & 8 Mbits/s	2, 4, & 8 Mbits/s	2, 4, & 8 Mbits/s	2, 4, 8, & 16 Mbits/s	2, 4, 8, & 16 Mbits/s
Subrate Switching	1-, 2-, 4-bit	1-, 2-, 4-bit	1-, 2-, 4-bit	1-, 2-, 4-bit	1-, 2-, 4-bit
Intel/*Motorola* Microprocessor Interface	Yes	Yes	Yes	Yes	Yes
32-bit PCI Interface	—	—	—	Yes	—
PCI Minibridge	—	—	—	Yes	—
H-bus/L-bus to PCI Packet Switching	—	—	—	Yes	—
StarFabric Interface	—	—	—	—	Yes
Package Type	208 SQFP 217 PBGA	208 SQFP 217 PBGA	208 SQFP 217 PBGA	272 PBGA	272 PBGA
Power Supply Voltage	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V 1.5 V

* For the T8102, local-to-local connections are achieved through L-H-L bus switching.

Below is a subset of Agere products that could complement the *Ambassador* family in your application.

Product Family	Description	Web Site
Analog Line Card Solutions	Complete integrated circuit line card solution. Products included are protection, switches, SLIC, codec, and ringing.	www.agere.com/alc
CelXpres™ ATM Interconnect	Portfolio of backplane interface devices that interconnect UTOPIA Level 1 or 2 to an ATM cell bus.	www.agere.com/ATM
Phone-On-A-Chip™ VoIP Solutions	Product family targeted at the enterprise IP phone market, but well suited for small office gateways and consumer IP phones.	www.agere.com/phone_chip

For additional information, contact your Agere Systems Account Manager or the following:
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ITALY: **(39) 02 6608131** (Milan), SPAIN: **(34) 1 807 1441** (Madrid)

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