TRIPATH

TA0103A

Stereo 250W (4Ω) Class-T Digital Audio Amplifier Driver using Digital Power Processing (DPP^{TM}) Technology

Technical Information Revision 3.3 - June 2000

GENERAL DESCRIPTION

The TA0103A is a 250W continuous average (4Ω), two channel Amplifier Driver Module which uses Tripath's proprietary Digital Power Processing (DPP^{TM}) technology. Class-T amplifiers offer both the audio fidelity of Class-AB and the power efficiency of Class-D amplifiers.

Applications

- Audio/Video
- Amplifiers/Receivers
- Pro-audio Amplifiers
- Automobile Power Amplifiers
- Subwoofer Amplifiers
- Home/PC Speaker Systems

Benefits

- Reduced system cost with smaller/less expensive power supply and heat sink
- Signal fidelity equal to high quality Class-AB amplifiers
- High dynamic range compatible with digital media such as CD and DVD

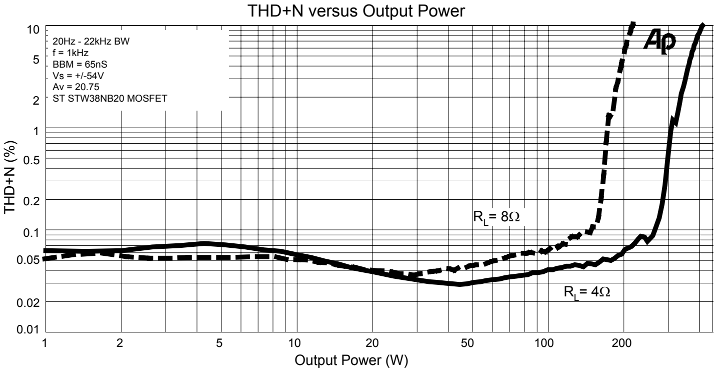
Features

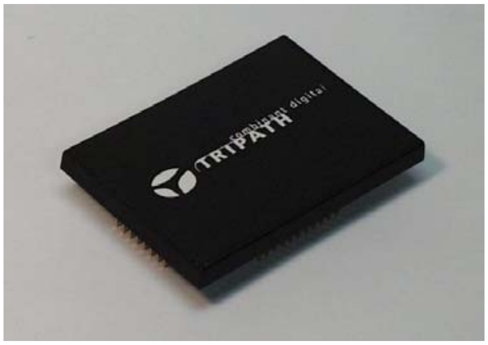
- Class-T architecture
- Proprietary Digital Power Processing technology

  Supports wide range of output power levels
- "Audiophile" Sound Quality
  - 0.04% THD+N @ 55W, 8Ω
  - 0.03% IHF-IM @ 36W, 8Ω
  - 140W @ 8Ω, 0.1% THD+N, $V_S = \underline{+}54V$
  - 250W @ 4Ω, 0.1% THD+N, $V_S = \underline{+}54V$
- High Power
  - 150W @ 8Ω, 1% THD+N, $V_S = \underline{+}54V$
  - 300W @ 4Ω, 1% THD+N, $V_S = \underline{+}54V$
- High Efficiency
  - 92% @ 155W @ 8Ω, $V_S = \underline{+}45V$
  - 90% @ 275W @ 4Ω, $V_S = \underline{+}45V$
- Dynamic Range = 106 dB
- Requires only N-Channel MOSFET output transistors
- High power supply rejection ratio
- Mute input
- Outputs short-circuit protected
- Over- and under-voltage protection
- Bridgeable, single-ended outputs
- 38-pin quad package

  Supports 100kHz BW of Super Audio CD and DVD-Audio (refer to Application Note for specifics)

TYPICAL PERFORMANCE





Absolute Maximum Ratings

SYMBOL	PARAMETER	Value	UNITS
Vs	Supply Voltage (Vspos & Vsneg)	+/-85	V
V5	Positive 5 V Bias Supply	6	V
VN12	Reference Voltage: Nominal +12V referenced to Vsneg	18	V
T_{STORE}	Storage Temperature Range	-40 to 150	ºC
T_A	Operating Free-air Temperature Range	-20 to +80	ºC

Notes: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Damage will occur to the device if VN12 is not supplied or falls below the recommended operating voltage when V_S is within its recommended operating range.

Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
Vs	Supply Voltage (Vspos & Vsneg)	+/- 35		+/- 60	V
V5	Positive 5 V Bias Supply	4.5	5	5.5	V
VN12	Reference Voltage: Nominal +12V referenced to Vsneg	10.8	12	13.2	V

Note: Recommended Operating Conditions indicate conditions for which the device is functional. See Electrical Characteristics for guaranteed specific performance limits.

Electrical Characteristics

T_A = 25°C. See Notes 1 & 2 for Operating Conditions and Test/Application Circuit Setup.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
I_q	Quiescent Current +45V		30	80	mA
	(no load, BBM0=BBM1=0) -45V		36	60	mA
	+5V		43	65	mA
	VN12		210	250	mA
I_S	Source Current @ P_{OUT} = 275W, R_L = 4Ω V_{SPOS} = +45V		7	7.8	A
	@ 10% THD+N V_{SNEG} = -45V		7	7.8	A
I5	Source Current for 5V Bias Supply @ P_{OUT} = 275W, R_L = 4Ω		50	60	mA
IVN12	Source Current for VN12 Supply @ P_{OUT} = 275W, R_L = 4Ω		80	100	mA
Vu	Under Voltage (Vspos & Vsneg)			+/-35	V
Vo	Over Voltage (Vspos & Vsneg)	+/-60			V
V_{IH}	High-level Input Voltage (MUTE)	3.5			V
V_{IL}	Low-level Input Voltage (MUTE)			1	V
I_{DD}MUTE	Mute Supply Current +45V		0.375	2	mA
	(no load, BBM0=BBM1=0) -45V		3.7	5	mA
	+5V		17	25	mA
	VN12		0.5	2	mA
V_{OH}	High-level Output Voltage (HMUTE & OVERLOADB)	3.5			V
V_{OL}	Low-level Output Voltage (HMUTE & OVERLOADB)			1	V
V_{TOC}	Over Current Sense Voltage Threshold	0.67	0.75	0.82	V
A_V	Gain Ratio V_{OUT}/V_{IN}, R_{IN} = 0Ω		108		V/V
Voffset	Offset Voltage, no load, MUTE = Logic low (before nulling)		300	500	mV

Minimum and maximum limits are guaranteed but may not be 100% tested.

Performance Characteristics – Single Ended, Vs = ±54V

Unless otherwise specified, f = 1kHz, Measurement Bandwidth = 22kHz. T_A = 25°C.
See Notes 1 & 2 for Operating Conditions and Test/Application Circuit Setup.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
P_{OUT}	Output Power (Continuous Average/Channel)	THD+N = 0.1%, R_L = 8Ω R_L = 4Ω THD+N = 1%, R_L = 8Ω R_L = 4Ω		140 250 150 300		W W W W
THD + N	Total Harmonic Distortion Plus Noise	P_{OUT} = 55W/Channel, R_L = 8Ω		0.04		%
IHF-IM	IHF Intermodulation Distortion	19kHz, 20kHz, 1:1 (IHF), R_L = 4Ω P_{OUT} = 36W/Channel		0.02		%
SNR	Signal-to-Noise Ratio	A Weighted, R_L = 8Ω, P_{OUT}=140W/Ch		101		dB
CS	Channel Separation	0dBr = 60W, R_L = 4Ω, f = 1kHz		82		dB
PSRR	Power Supply Rejection Ratio	Input Referenced, 30kHz Bandwidth		67		dB
η	Power Efficiency	P_{OUT} = 200W/Channel, R_L = 8Ω		92		%
e_{NOUT}	Output Noise Voltage	A Weighted, no signal, input shorted, DC offset nulled to zero, BBM = 145nS		295		μV

Performance Characteristics – Single Ended, Vs = ±45V

Unless otherwise specified, f = 1kHz, Measurement Bandwidth = 22kHz. T_A = 25°C.
See Notes 1 & 2 for Operating Conditions and Test/Application Circuit Setup.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
P_{OUT}	Output Power (Continuous Average/Channel)	THD+N = 0.1%, R_L = 8Ω R_L = 4Ω THD+N = 1%, R_L = 8Ω R_L = 4Ω		85 150 100 200		W W W W
THD + N	Total Harmonic Distortion Plus Noise	P_{OUT} = 55W/Channel, R_L = 8Ω		0.04		%
IHF-IM	IHF Intermodulation Distortion	19kHz, 20kHz, 1:1 (IHF), R_L = 4Ω P_{OUT} = 36W/Channel		0.03		%
SNR	Signal-to-Noise Ratio	A Weighted, R_L = 8Ω, P_{OUT} = 85W/Ch		100		dB
CS	Channel Separation	0dBr = 60W, R_L = 4Ω, f = 1kHz		82		dB
PSRR	Power Supply Rejection Ratio	Input Referenced, 30kHz Bandwidth		67		dB
η	Power Efficiency	P_{OUT} = 155W/Channel, R_L = 8Ω		92		%
e_{NOUT}	Output Noise Voltage	A Weighted, no signal, input shorted, DC offset nulled to zero, BBM = 145nS		250		μV

Minimum and maximum limits are guaranteed but may not be 100% tested.

Notes:

1) V5 = +5V, VN12 = +12V referenced to V_{SNEG}
2) Test/Application Circuit Values: D = MUR120T3 diodes, R_{IN} = 22.1KΩ
R_D = 33Ω, R_S = 0.025Ω,R_G = 10Ω
R_{OCR1} = R_{OCR2} = 0Ω, L_F = 18uH (Amidon core T200-2)
C_F = 0.22uF, C_D = 0.1uF, C_{IN} = 1uF, C_{BY} = 0.1uF
Power Output MOSFETs, M = ST STW38NB20
BBMO=0, BBM1=1

Pin Description

Pin	Function	Description
1	AGND	Analog Ground
2	OVERLOADB	Logic output. When low, indicates that the level of the input signal has overloaded the amplifier.
3	V5	Positive 5 Volts
4	MUTE	Logic input. When high, both amplifiers are muted. When low (grounded), both amplifiers are fully operational.
5, 6	IN2, IN1	Single-ended input (Channel 1 & 2)
7, 8	BBM0, BBM1	Break-before-make timing control
9, 12	GNDKELVIN1, GNDKELVIN2	Kelvin connection to speaker ground (Channel 1 & 2)
10, 11	OCR2, OCR1	Over-current threshold adjustment (Channel 1 & 2)
13, 14	OCS1L+, OCS1L-	Over Current Sense resistor, Channel 1 low-side
15, 16	OCS1H-, OCS1H+	Over Current Sense resistor, Channel 1 high-side
17, 30	LO1COM, LO2COM	Kelvin connection to source of low-side transistor (Channel 1 & 2)
18, 29	FDBKN1;FDBKN2	Feedback (Channel 1 & 2)
19	VN12	Voltage: +12 V from V_{SNEG}. Refer to Application Information section.
20, 27	LO1, LO2	Low side gate drive output (Channel 1 & 2)
21, 26	HO1COM, HO2COM	Kelvin connection to source of high-side transistor (Channel 1 & 2)
22, 25	HO1, HO2	High side gate drive output (Channel 1 & 2)
23	V_{SPOS}	Positive supply voltage
24	V_{SNEG}	Negative supply voltage
28	PGND	Power Ground
31, 32	OCS2L-, OCS2L+	Over Current Sense resistor, Channel 2 low-side
33, 34	OCS2H-, OCS2H+	Over Current Sense resistor, Channel 2 high-side
35	HMUTE	Logic output. When high, indicates that the output stages of both amplifiers are shut off and muted.
36, 37, 38	NC	Not Connected - Must Be Left Floating

38 Pin Quad Package Pin-out

(Top View)

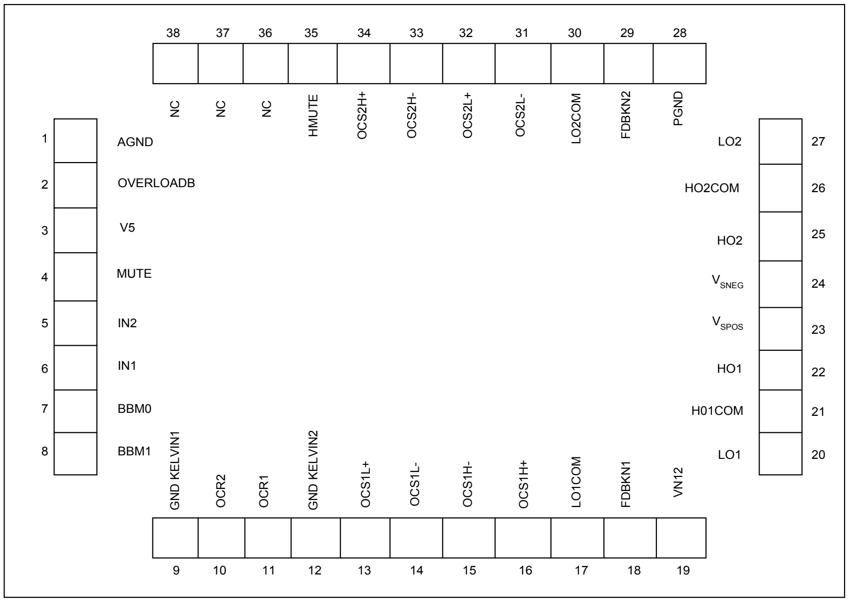
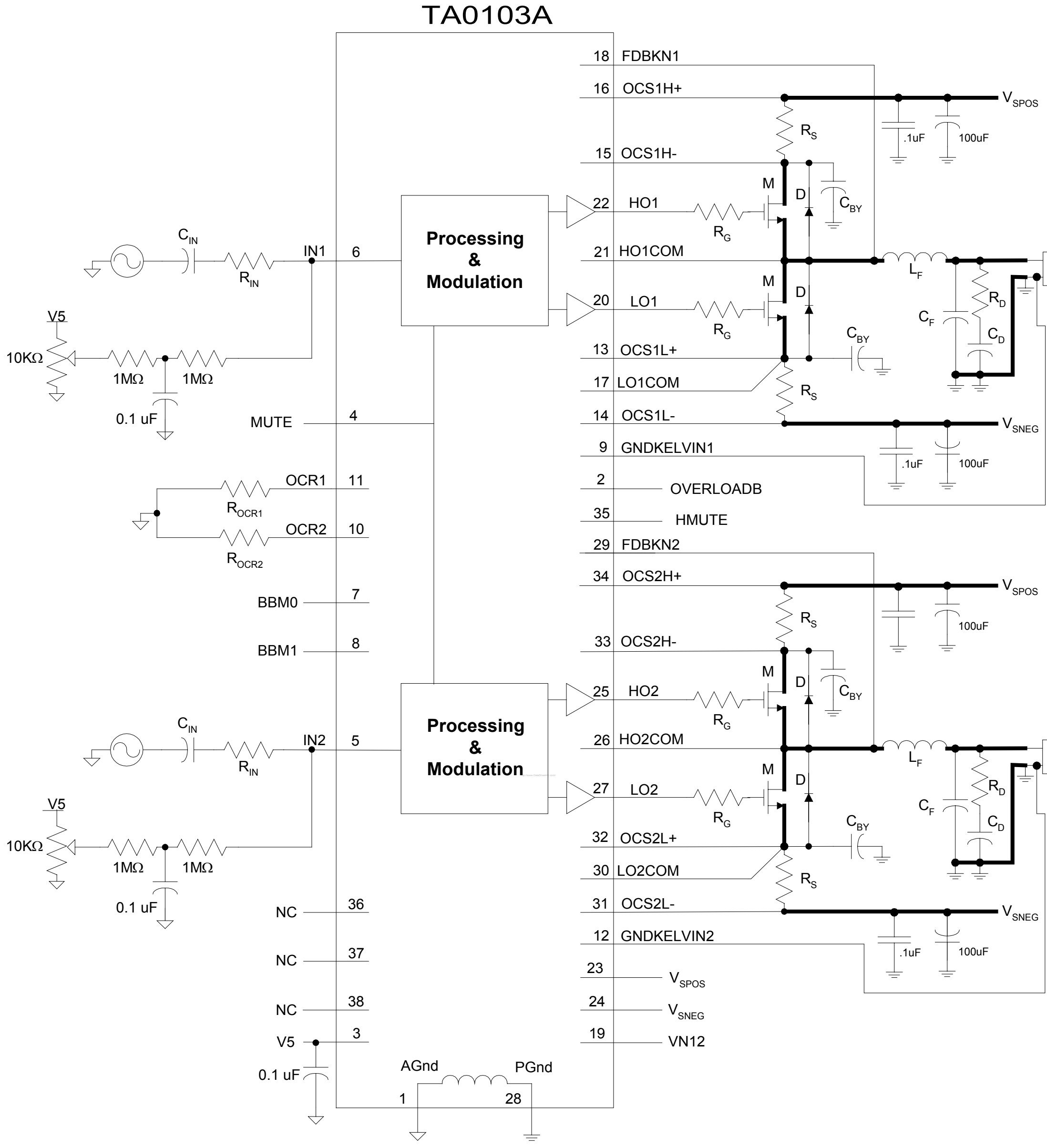


Figure 1

Test/Application Circuit

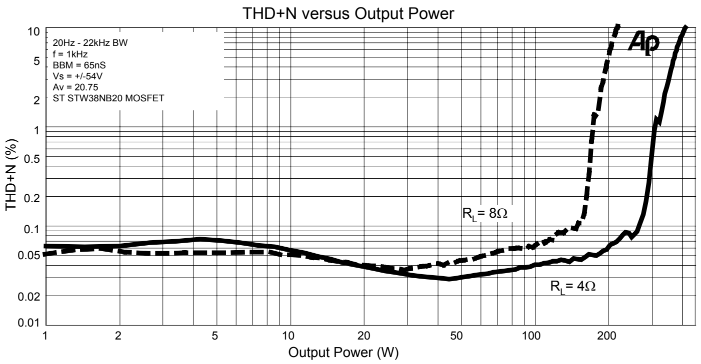


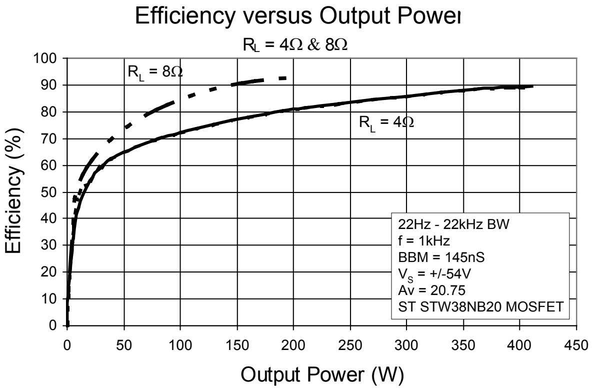
NC - Not Connected (Must Be Left Floating)

Note - Heavy Lines Indicate High-Current Paths

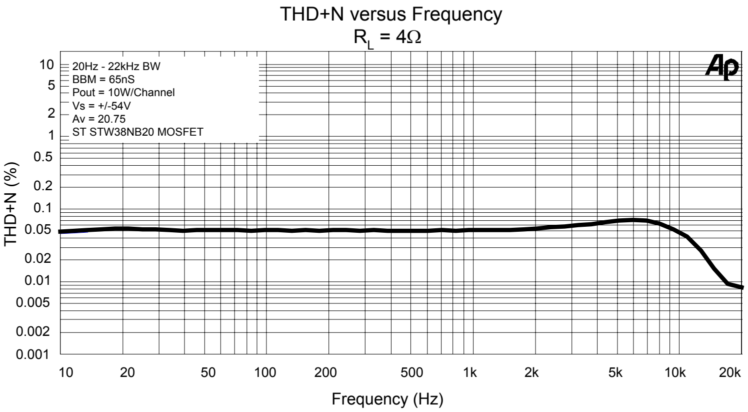
Figure 2

Typical Performance at Vs = +54V

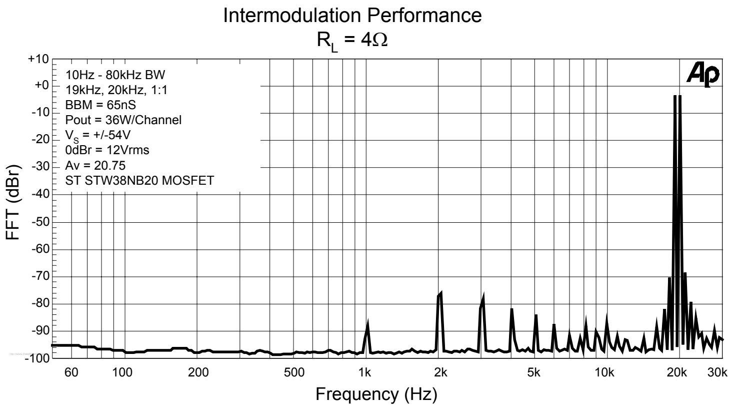

THD+N versus Output Power


Efficiency versus Output Power

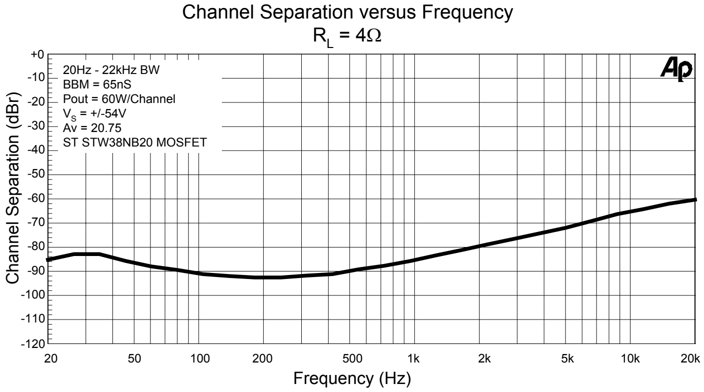
R_L = 4Ω & 8Ω


THD+N versus Frequency

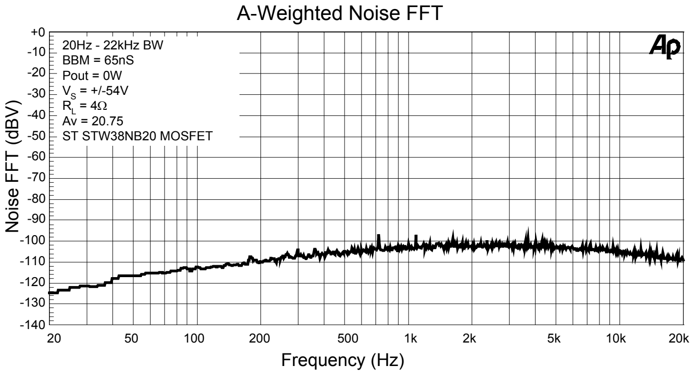
R_L = 4Ω


Intermodulation Performance

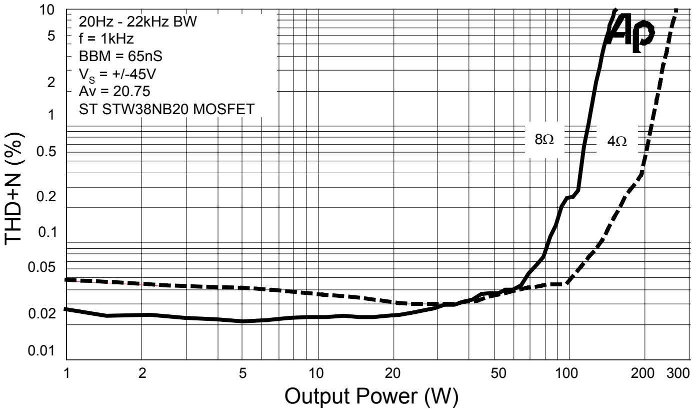
R_L = 4Ω


Channel Separation versus Frequency

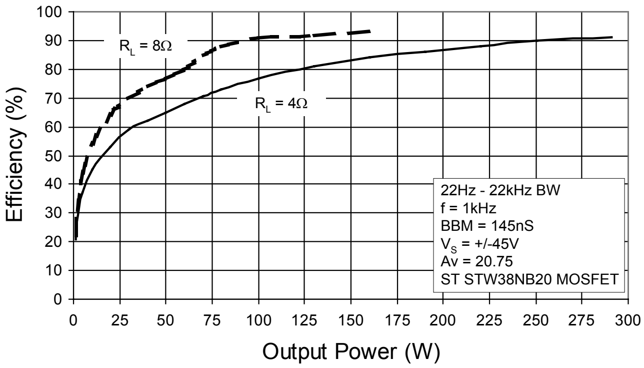
R_L = 4Ω


A-Weighted Noise FFT

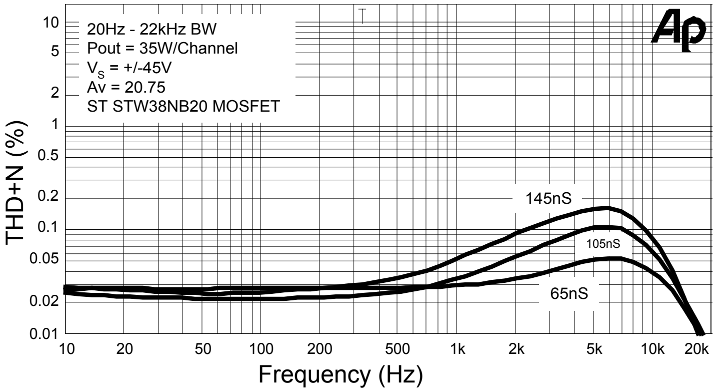
Typical Performance at Vs = ±45V



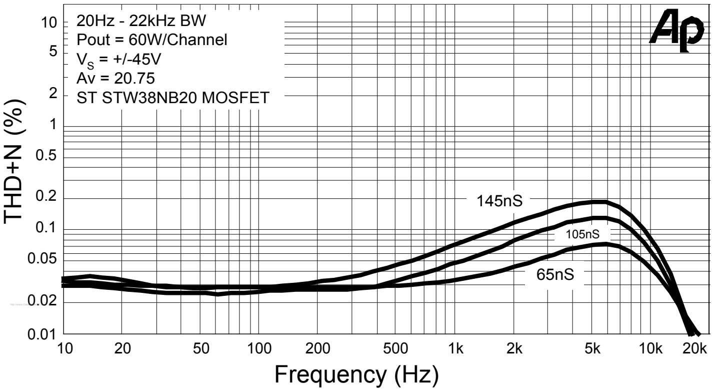
THD+N vs Output Power



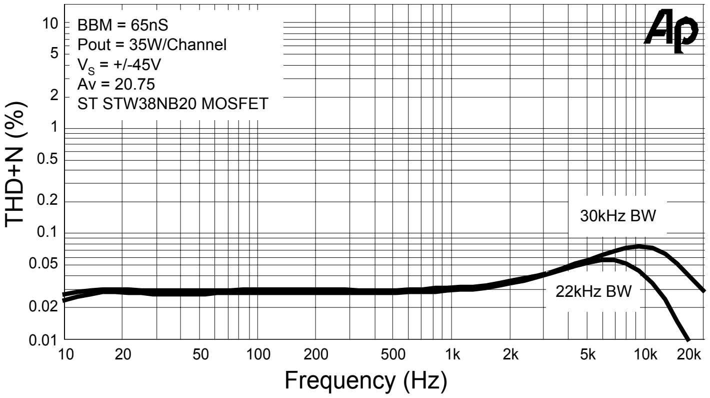
Efficiency versus Output Power



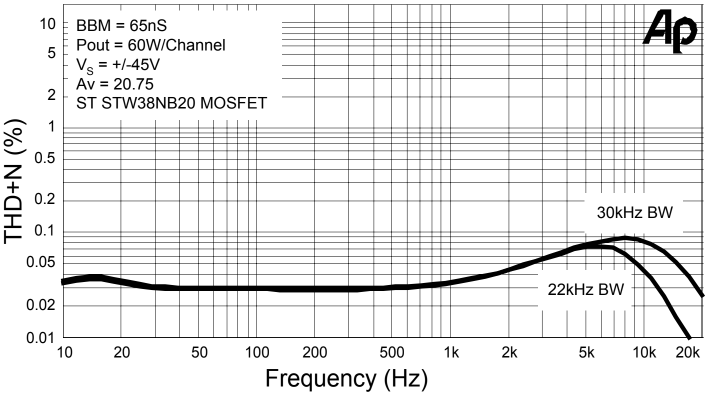
THD+N versus Frequency versus Break Before Make, R_L = 8Ω



THD+N versus Frequency versus Break Before Make, R_L = 4Ω



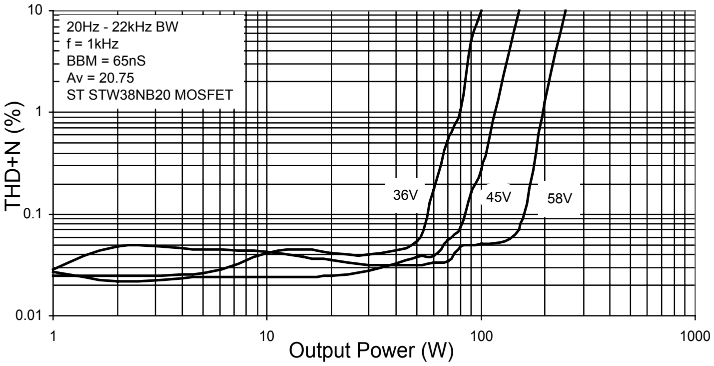
THD+N versus Frequency versus Bandwidth, R_L = 8Ω



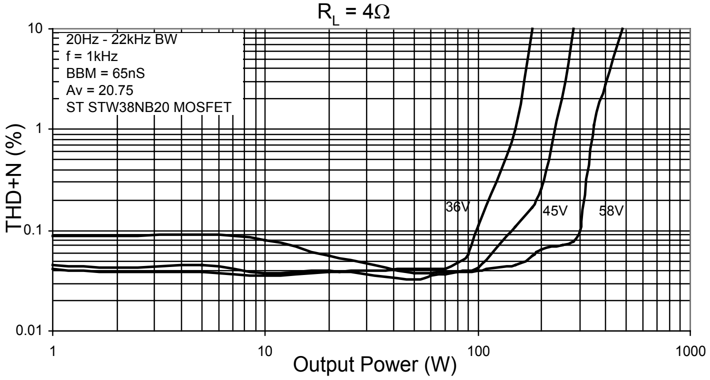
THD+N versus Frequency versus Bandwidth, R_L = 4Ω

Typical Performance

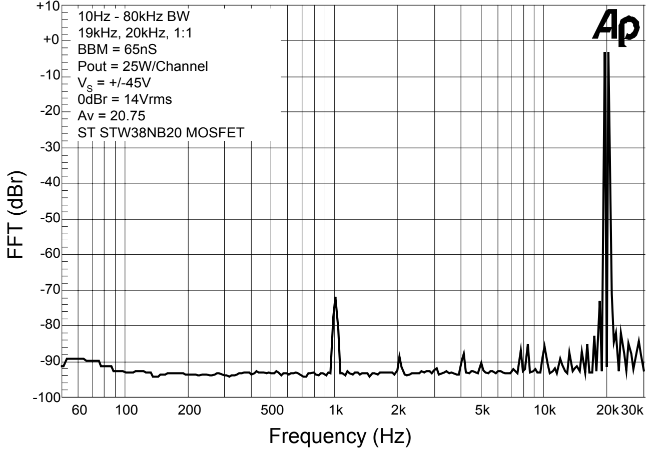
THD+N versus Output Power versus Supply Voltage
$R_L = 8\Omega$



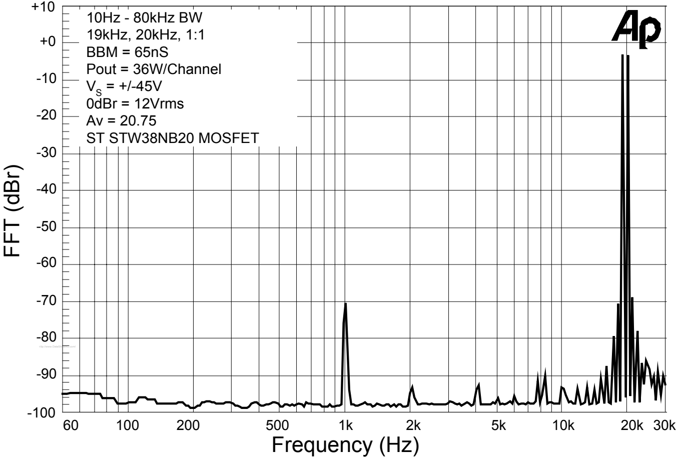
THD+N versus Output Power versus Supply Voltage
$R_L = 4\Omega$



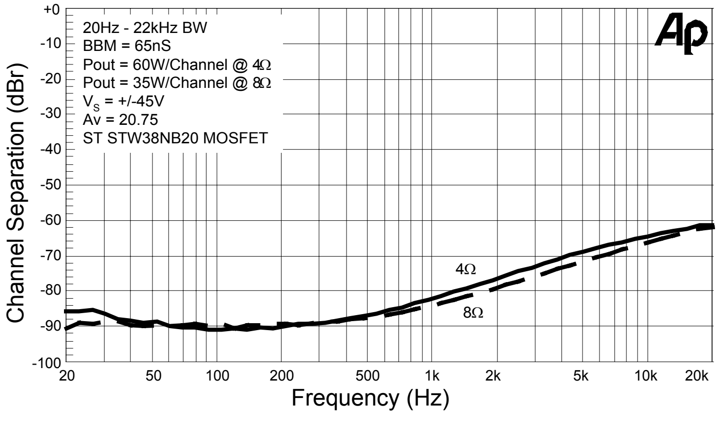
Intermodulation Performance
$R_L = 8\Omega$



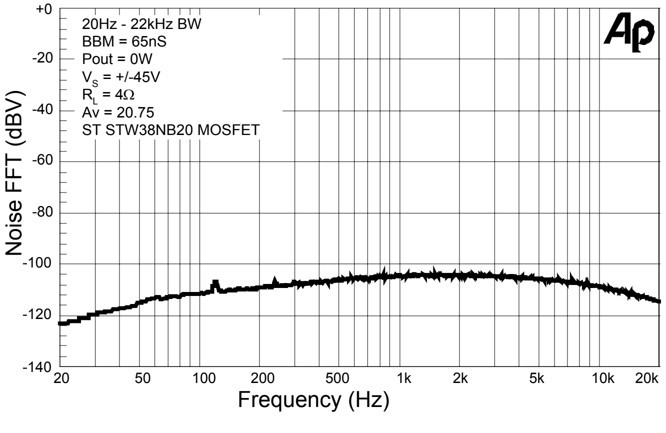
Intermodulation Performance
$R_L = 4\Omega$



Channel Separation versus Frequency



A-Weighted Noise FFT



Functional Description

TA0103A Amplifier Operation

Figure 3 is a simplified diagram of one channel (channel 1) of a TA0103A amplifier to assist in understanding its operation.

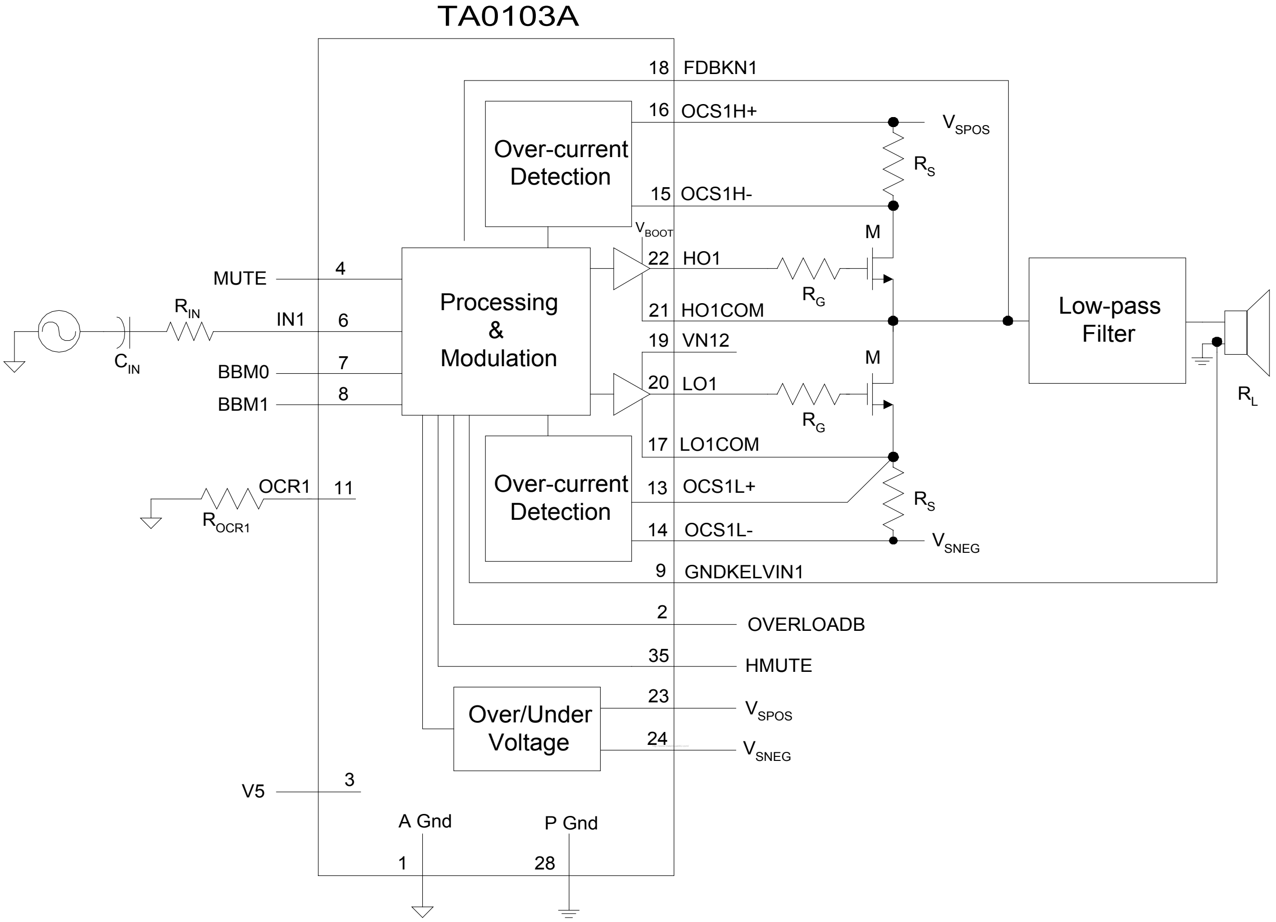


Figure 3: Simplified TA0103A Amplifier

The audio input signal (IN1) is fed to the processor internal to the TA0103A, where a modulation pattern is generated. This pattern is spread spectrum and varies between approximately 200kHz and 1.5MHz. Complementary copies of the switching pattern are level-shifted by the MOSFET drivers and output from the TA0103A where they drive the gates (HO1 and LO1) of external power MOSFETs that are connected as a half bridge. The output of the half bridge is a power-amplified version of the switching pattern that switches between V_{SPOS} and V_{SNEG}. This signal is then low-pass filtered to obtain amplified audio.

The processor portion of the TA0103A is operated from a 5-volt supply (between V5 and AGND). In the generation of the complementary modulation pattern for the output MOSFETs, the processor inserts a “break-before-make” dead time between when it turns one transistor off and it turns the other one on in order to minimize shoot-through currents in the MOSFETs. The dead time can be programmed by setting the break-before-make control bits, BBM0 and BBM1. Feedback information from the output of the half-bridge is supplied to the processor via FDBKN1. Additional feedback information to account for ground bounce is supplied via GNDKELVIN1.

The MOSFET drivers in the TA0103A are operated from voltages obtained from VN12 and LO1COM for the low-side driver, and V_{BOOT} (generated internal to the TA0103A) and HO1COM for the high-side. Only N-Channel MOSFETs are required for both the top and bottom of the half bridge. VN12 must be a stable 12V above V_{SNEG}. The gate resistors, R_G, are used to control MOSFET slew rate and thereby minimize voltage overshoots.

Over- and Under-Voltage Protection

The TA0103A senses the power rails through V_{SPOS} and V_{SNEG} for over- and under-voltage conditions. The over- and under-voltage limits are Vo and Vu respectively as specified in the Electrical Characteristics table. If the supply voltage exceeds Vo or drops below Vu, the TA0103A shuts off the output stages of the amplifiers and asserts a logic level high on HMUTE. The removal of the over-voltage or under-voltage condition returns the TA0103A to normal operation and returns HMUTE to a logic level low. Please note that the limits specified in the Electrical Characteristics table are at 25°C and these limits may change over temperature.

Over-current Protection

The TA0103A has over-current protection circuitry to protect itself and the output transistors from short-circuit conditions. The TA0103A uses the voltage across a resistor, R_S (measured via OCS1H+, OCS1H-, OCS1L+ and OCS1L-), that is in series with each output MOSFET to detect an over-current condition. R_S and R_{OCR} are used to set the over-current threshold. The OCS pins must be Kelvin connected for proper operation. See “Circuit Board Layout” in Application Information for details. An over-current condition will cause the TA0103A to shut off the output stages of the amplifiers and supply a logic level high on HMUTE. The occurrence of an over-current condition is latched in the TA0103A and can be cleared by toggling the MUTE input or cycling power.

Overload

When logic low, the OVERLOADB pin indicates that the level of the input signal has overloaded the amplifier and that the audio output signal is starting to distort. The OVERLOADB signal is active only while an overload is present. The OVERLOADB signal can be used to control a distortion indicator light or LED through a simple buffer circuit.

Mute

When a logic high signal is supplied to MUTE, both amplifier channels are muted (both high- and low-side transistors are turned off) and a logic level high is output on the HMUTE pin. When a logic level low is supplied to MUTE, both amplifiers are fully operational and a logic level low is supplied on HMUTE. There is a delay of approximately 200 milliseconds between the de-assertion of MUTE and the un-muting of the TA0103A.

Application Information

Amplifier Gain and Input Resistor Selection

The value of the input resistor, R_{IN}, is based on the required voltage gain, A_V, of the amplifier according to:

$A_V = 538 \times 10^3/(R_{IN} + 5000)$
where R_{IN} = Input resistor value in ohms.

Input Capacitor Selection

C_{IN} can be calculated once a value for R_{IN} has been determined. C_{IN} and R_{IN} determine the input low-frequency pole. Typically this pole is set at 10 Hz. C_{IN} is calculated according to:

$C_{IN} = 1/((2\pi \times F_P)(R_{IN} + 5000))$

where:
R_{IN} = Input resistor value in ohms.
F_P = Input low frequency pole (typically 10Hz).

DC Offset Adjust

While the DC offset voltages that appear at the speaker terminals of a TA0103A amplifier are typically small, Tripath recommends that any offsets during operation be nulled out of the amplifier with a circuit like the one shown connected to IN1 and IN2 in the Test/Application Circuit.

It should be noted that the DC voltage on the output of a TA0103A amplifier with no load in mute mode is approximately 2.5V. This offset does not need to be nulled. The output impedance of the amplifier in mute mode is approximately 10 KOhms. This means that the 2.5V drops to essentially zero when a typical load is connected.

Supply Voltage and Output Power

The relationship between the bipolar power supply voltage needed, V_S, for a given RMS output power, P_{OUT}, into a given load, R_L, at a given level of THD (total harmonic distortion) is approximated by:

$V_S = (2 \times R_L \times P_{OUT})^{0.5}/(K \times R_L/(R_L + R_{ON} + R_S + R_{COIL}))$

where:
R_{ON} = The at-temperature R_{DSON} of the output transistors, M.
R_{COIL} = Resistance of the output filter inductor.
R_S = Sense Resistor
K = THD Factor, a number fixed by the algorithms in the TA0103A's signal processor that provides the relationship between THD *at full output power* of the amplifier and V_S. K corresponds to THD at full output power as follows:

THD	K
0.1%	0.83
1%	0.95
10%	1.09

Typical measurement graphs of P_{OUT} versus supply voltage for various levels of THD are also included in this data sheet to help determine the supply voltage.

Bridged Operation

Note that the two channels of a TA0103A amplifier can be used to provide a single, bridged amplifier of almost four times the output power of one of the single-ended amplifier channels. To configure a bridged amplifier, the input to one TA0103A channel must be the inverted signal of the input to the other channel.

Low-frequency Power Supply Pumping

A potentially troublesome phenomenon in single-ended switching amplifiers is power supply pumping. This is caused by current from the output filter inductor flowing into the power supply output filter capacitors in the opposite direction as a DC load would drain current from them. Under certain conditions (usually low-frequency input signals), this current can cause the supply voltage to "pump" (increase in magnitude) and eventually cause over-voltage/under-voltage shut down. Moreover, since over/under-voltage are not "latched" shutdowns, the effect would be an amplifier that oscillates between on and off states. If a DC offset on the order of 0.3V is allowed to develop on the output of the amplifier (see "DC Offset Adjust"), the supplies can be boosted to the point where the amplifier's over-voltage protection triggers.

One solution to the pumping issue is to use large power supply capacitors to absorb the pumped supply current without significant voltage boost. The low frequency pole used at the input to the driver determines the value of the supply capacitor required. This works for AC signals only.

Another solution to the supply pumping problem uses the fact that music has low frequency information that is correlated in both channels (it is in phase). This information can be used to eliminate boost by putting the two channels of a TA0103A amplifier out of phase with each other. This works because each channel is pumping out of phase with the other, and the net effect is a cancellation of pumping currents. The phase of the audio signals needs to be corrected by connecting one of the speakers in the opposite polarity as the other channel.

VN12 Supply

VN12 is an additional supply voltage required by the TA0103A. VN12 must be 12 volts more positive than the nominal V_{SNEG}. VN12 must track V_{SNEG}, so if an unregulated supply is used for V_{SNEG}, the design of the supply for VN12 must behave accordingly. Generating the VN12 supply requires some care.

The proper way to generate the voltage for VN12 is to use a 12V-supply voltage referenced to the V_{SNEG} supply rather than to ground (PGND). Figure 4 shows the correct way to power the TA0103A:

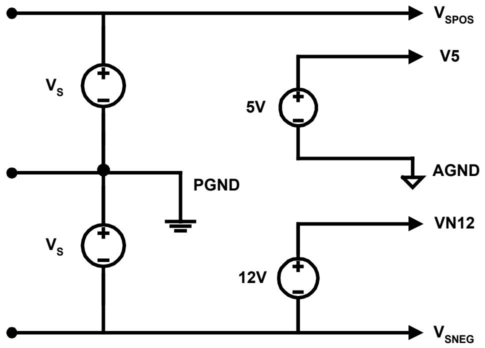


Figure 4

One method to generate the VN12 supply voltage is to use a positive 12V IC regulator to drop PGND down to 12V (relative to V_{SNEG}). Care must be exercised with this method because some IC regulators such as the LM340 series will not function properly with a large voltage drop across the regulator, resulting in damage to the TA0103A.

Generating the VN12 voltage per Figure 5 is NOT recommended. Most power supplies only sink current from the negative terminal and will not be capable of sourcing the current required by VN12. Furthermore, problems can arise since VN12 will not track movements in V_{SNEG}.

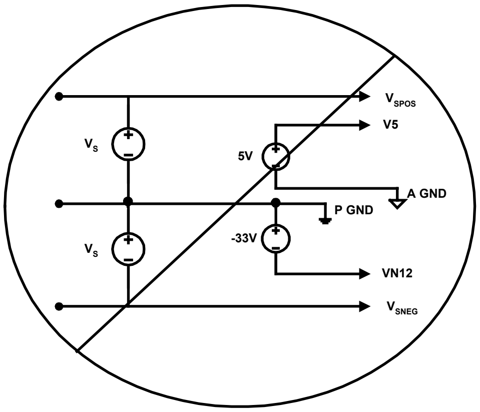


Figure 5

Setting Over-current Threshold

R_S and R_{OCR} determine the value of the over-current threshold, I_{SC}:

$I_{SC} \times R_S = (V_{TOC} \times 9100)/(9100 + R_{OCR})$

where:
R_S and R_{OCR} are in Ω
$I_{SC} = 3 \times I_{RMS} = 3 \times (P_{OUT}/R_L)^{0.5}$ (Over-current is typically set for 3 x RMS current)
V_{TOC} = Over-current sense threshold voltage (See Electrical Characteristics Table)
= 0.75V typically
when $R_{OCR} = 0\Omega$, $R_S = (0.75)/I_{SC}$

Note that R_S will dissipate approximately $(I_{RMS})^2 \times R_S$ of power. To set an I_{SC} of 30A, for example, with $R_{OCR} = 0\Omega$, means that $R_S = 25\text{m}\Omega$ and R_S must dissipate 2.5W on average. If $R_{OCR} = 9.1\text{K}\Omega$, then to set I_{SC} = 30A, R_S will be 12.5mΩ and will only have to dissipate 1.13W on average.

As high-wattage resistors are usually only available in a few low-resistance values (10mΩ, 25mΩ and 50mΩ), R_{OCR} can be used to adjust for a particular over-current threshold using one of these values for R_S.

Output Transistor Selection

The key parameters to consider when selecting a MOSFET to use with the TA0103A are drain-source breakdown voltage (BVdss), gate charge (Qg), and on-resistance ($R_{DS(ON)}$).

The BVdss rating of the MOSFET needs to be selected to accommodate the voltage swing between V_{SPOS} and V_{SNEG} as well as any voltage peaks caused by voltage ringing due to switching transients. With a ‘good’ circuit board layout, a BVdss that is 50% higher than the V_{SPOS} and V_{SNEG} voltage swing is a reasonable starting point. The BVdss rating should be verified by measuring the actual voltages experienced by the MOSFET in the final circuit.

Ideally a low Qg (total gate charge) and low $R_{DS(ON)}$ are desired for the best amplifier performance. Unfortunately, these are conflicting requirements since $R_{DS(ON)}$ is inversely proportional to Qg for a typical MOSFET. The design trade-off is one of cost versus performance. A lower $R_{DS(ON)}$ means lower $I^2R_{DS(ON)}$ losses but the associated higher Qg translates into higher switching losses (losses = Qg x 12 x 1.2MHz). A lower $R_{DS(ON)}$ also means a larger silicon die and higher cost. A higher $R_{DS(ON)}$ means lower cost and lower switching losses but higher I^2R_{DSON} losses.

The following table lists BVdss, Qg and $R_{DS(ON)}$ for MOSFETs that Tripath has used with the TA0103A:

Mfg. Part Number	**BVdss**	**Qg (Max) (nanoCoulombs)**	**$R_{DS(ON)}$ (Max) (Ohms)**
ST STW34NB20	200	80	0.075
ST STW38NB20	200	95	0.065
ST STP19NB20	200	40	0.18
IR IRF640	200	70	0.18

Gate Resistor Selection

The gate resistors, R_G, are used to control MOSFET switching rise/fall times and thereby minimize voltage overshoots. They also dissipate a portion of the power resulting from moving the gate charge each time the MOSFET is switched. If R_G is too small, excessive heat can be generated in the driver. Large gate resistors lead to slower MOSFET switching, which requires a larger break-before-make (BBM) delay. Tripath recommends using an R_G of 10Ω when the Qg of the MOSFET is less than 70nC and 5.6Ω when the Qg is greater than 70nC.

Break-Before-Make (BBM) Timing Control

The half-bridge power MOSFETs require a deadtime between when one transistor is turned off and the other is turned on (break-before-make) in order to minimize shoot through currents. BBM0 and BBM1 are logic inputs (connected to logic high or pulled down to logic low) that control the break-before-make timing of the output transistors according to the following table. Note that if either BBM0 or BBM1 are left floating, they are pulled to a logic low level internal to the TA0103A.

BBM1	**BBM0**	**Delay**
0	0	145nS
0	1	105nS
1	0	65nS
1	1	25nS

The tradeoff involved in making this setting is that as the delay is reduced, distortion levels improve but shoot-through and power dissipation increase. Since the actual amount of BBM required is dependent upon other component values and circuit board layout, the value selected should be verified in the actual application circuit/board. It should also be verified under maximum temperature and power conditions since shoot-through in the output MOSFETs can increase under these conditions, possibly requiring a higher BBM setting than at room temperature.

Clamping Diodes

The purpose of the diode, D, across each of the output MOSFETs is to clamp the voltages the MOSFET experiences to levels within its rating to prevent damage. Tripath recommends that fast-recovery or schottky diodes be used for this purpose (depending on the supply voltage used). The breakdown voltage rating of this diode should be similar to that of the MOSFET. Also, the forward voltage drop of this diode should be less than that of the internal body diode of the MOSFET.

MOSFET Bypass Capacitor

Bypass capacitors, C_{BY}, are necessary for each output MOSFET at the nodes shown in the Test/Application Circuit to damp voltage ringing at these nodes due to the high currents flowing through the parasitic (circuit board trace) inductance. C_{BY} should be 0.1uF and have the appropriate voltage rating. They should be physically located as close to the MOSFET leads as possible.

Turn-on & Turn-off Noise

If turn-on or turn-off noise is present in a TA0103A amplifier, the cause is frequently due to other circuitry external to the TA0103A. While the TA0103A has circuitry to suppress turn-on and turn-off transients, the combination of the power supply and other audio circuitry with the TA0103A in a particular application may exhibit audible transients. One solution that will completely eliminate turn-on and turn-off pops and clicks is to use a relay to connect/disconnect the amplifier from the speakers with the appropriate timing at power on/off. The relay can also be used to protect the speakers from a component failure (e.g. shorted output MOSFET), which is a protection mechanism that some amplifiers have. Circuitry external to the TA0103A would need to be implemented to detect these failures.

Output Filter Design

One advantage of Tripath amplifiers over PWM solutions is the ability to use higher-cutoff-frequency filters. This means any load-dependent peaking/droop in the 20kHz audio band potentially caused by the filter can be made negligible. This is especially important for applications where the user may select a 4-Ohm or 8-Ohm speaker. Furthermore, speakers are not purely resistive loads and the impedance they present changes over frequency and from speaker model to speaker model.

Tripath recommends designing the filter as a 2nd order, 80kHz LC filter. Tripath has obtained good results with L_F = 18uH and C_F = 0.22uF for a nominal impedance of 8Ω.

The core material of the output filter inductor has an effect on the distortion levels produced by a TA0103A amplifier. Tripath recommends low-mu type-2 iron powder cores because of their low loss and high linearity.

Tripath also recommends that an RC damper be used after the LC low-pass filter. No-load operation of a TA0103A amplifier can create significant peaking in the LC filter, which produces strong resonant currents that can overheat the output MOSFETs and/or other components. The RC dampens the peaking and prevents problems. Tripath has obtained good results with R_D = 33Ω and C_D = 0.1uF.

It is highly recommended that the design process for a TA0103A amplifier include an analysis of the interaction of intended speaker(s) with the LC filter and RC damper to ensure the desired frequency response is attained. Component values for the LC filter and RC damper may need to be altered from the Tripath suggestions to achieve the required response.

Grounding

Tripath recommends not connecting analog ground (AGND) to power ground (PGND) externally, as this connection is already made internal to the TA0103A.

Circuit Board Layout

Considerable care needs to be taken in the layout of the circuit board for a TA0103A amplifier. The high currents flowing through PCB traces and the inductive effects due to the switching frequencies involved can cause large overshoot and undershoot voltages if care is not taken. A general rule to follow is to keep the PCB trace of each signal path to/from each lead of each output MOSFET as short as physically possible.

Certain circuit functions in a TA0103A amplifier cannot share PCB return paths with other functions because of the resistive and inductive effects of the switching currents and frequencies used. These so-called ‘Kelvin’ paths must each have a dedicated PCB trace from the TA0103A to their destination. The following signals should be treated as Kelvin paths: OCS1H+, OCS1H-, OCS1L+, OCS1L-, OCS2H+, OCS2H-, OCS2L+, OCS2L-, FDBKN1, FDBKN2, GNDKELVIN1 and GNDKELVIN2.

Performance Measurements of a TA0103A Amplifier

Tripath amplifiers operate by modulating the input signal with a high-frequency switching pattern. This signal is sent through a low-pass filter (external to the Tripath amplifier) that demodulates it to recover an amplified version of the audio input. The frequency of the switching pattern is spread spectrum and typically varies between 200kHz and 1.5MHz, which is well above the 20Hz – 22kHz audio band. The pattern itself does not alter or distort the audio input signal but it does introduce some inaudible noise components.

The measurements of certain performance parameters, particularly those that have anything to do with noise, like THD+N, are significantly affected by the design of the low-pass filter used on the output of the TA0103A and also the bandwidth setting of the measurement instrument used. Unless the filter has a very sharp roll-off just past the audio band or the bandwidth of the measurement instrument ends there, some of the inaudible noise components introduced by the Tripath amplifier switching pattern will get integrated into the measurement, degrading it.

One advantage of Tripath amplifiers is that they do not require large multi-pole filters to achieve excellent performance in listening tests, usually a more critical factor than performance measurements. Though using a multi-pole filter may remove high-frequency noise and improve THD+N type measurements (when they are made with wide-bandwidth measuring equipment), these same filters can increase distortion due to inductor non-linearity. Multi-pole filters require relatively large inductors, and inductor non-linearity increases with inductor value.

Efficiency Of A TA0103A Amplifier

The efficiency, η, of an amplifier is:

$$\eta = P_{OUT}/P_{IN}$$

The power dissipation of a TA0103A amplifier is primarily determined by the on resistance, R_{ON}, of the output transistors used, and the switching losses of these transistors, P_{SW}. For a TA0103A amplifier, P_{IN} (per channel) is approximated by:

$$P_{IN} = P_{DRIVER} + P_{SW} + P_{OUT}\,((R_S + R_{ON} + R_{COIL} + R_L)/R_L)^2$$

where:

P_{DRIVER} = Power dissipated in the TA0103A = 1.6W/channel
$P_{SW} = 2 \times (0.015) \times Q_g$ (Q_g is the gate charge of M, in nano-coulombs)
R_{COIL} = Resistance of the output filter inductor (typically around 50mΩ)

For an 155W RMS per channel, 8Ω load amplifier using STW38NB20 MOSFETs, and an R_S of 50mΩ,

$$\begin{aligned} P_{IN} &= P_{DRIVER} + P_{SW} + P_{OUT}\,((R_S + R_{ON} + R_{COIL} + R_L)/R_L)^2 \\ &= 1.6 + 2 \times (0.015) \times (95) + 155 \times ((0.025 + 0.11 + 0.05 + 8)/8)^2 \\ &= 1.6 + 2.85 + 162 \\ &= 166.7\text{W} \end{aligned}$$

In the above calculation the $R_{DS\,(ON)}$ of 0.065Ω was multiplied by a factor of 1.7 to obtain R_{ON} in order to account for some temperature rise of the MOSFETs. ($R_{DS\,(ON)}$ typically increases by a factor of 1.7 as for a typical MOSFET as temperature increases from 25ºC to 170ºC.)

So,

$$\eta = P_{OUT}/P_{IN} = 155/166.7 = 93\%$$

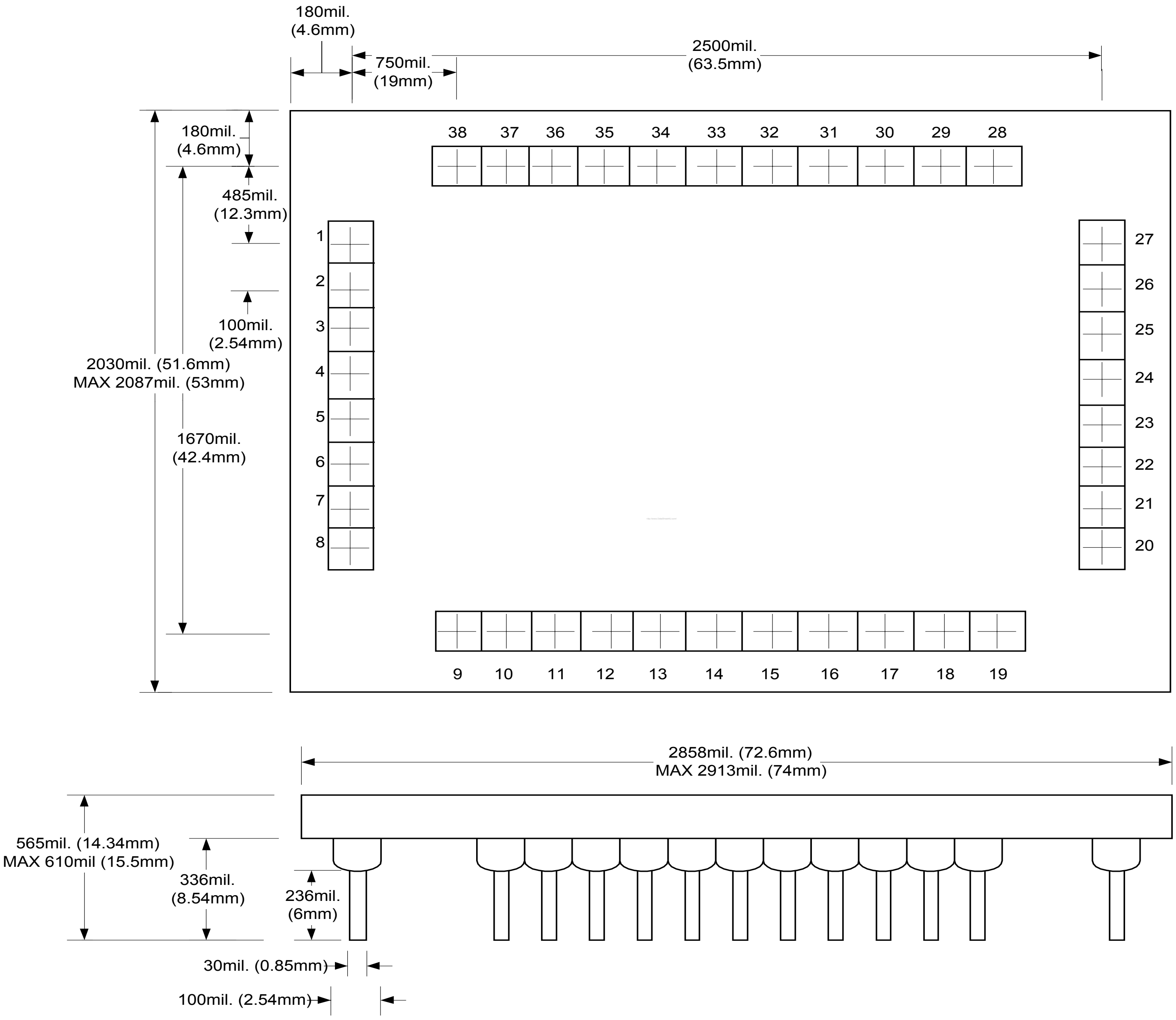
This compares to the 90% measured efficiency (see Typical Performance graphs).

Technical Documentation

Please refer to the Tripath “Application Notes” section on our web page (http://www.tripath.com/html/tech.htm#appnotes) for more information regarding evaluation, test and design of Class-T amplifiers.

Package Information

38 Pin Quad Module



Phyco Socket: 4150-1 x 8SF1 8 position header female
4150-1 x 1SF1 11 position header female

Figure 6

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