TOSHIBA Bipolar Linear Integrated Circuit Silicon Monolithic

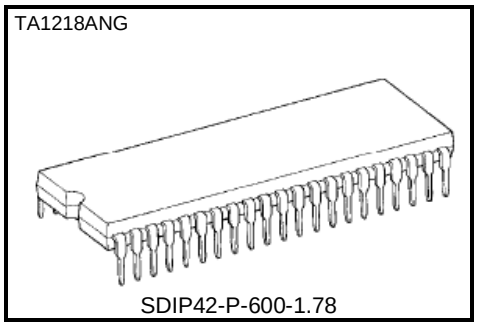
TA1218ANG

Audio/Video Switching IC for TVs

The TA1218ANG is an audio/video switching IC for TV sets.

Conforming to I^2C bus standards, it allows you to perform various switching operations through the bus lines by using a microcomputer. Thanks to its 2-channel outputs, the TA1218ANG can also be used for the PIP systems. Furthermore, since the presence of a signal on its sync signal output pin can be determined by a microcomputer, it is possible to check each input/output channel (self-diagnosis).

This IC has the same pin assignments as the TA1219ANG (SDIP36), a 1-channel output version of the TA1218ANG, so these chips are pin compatible on pins 3 to 20 and 23 to 40.



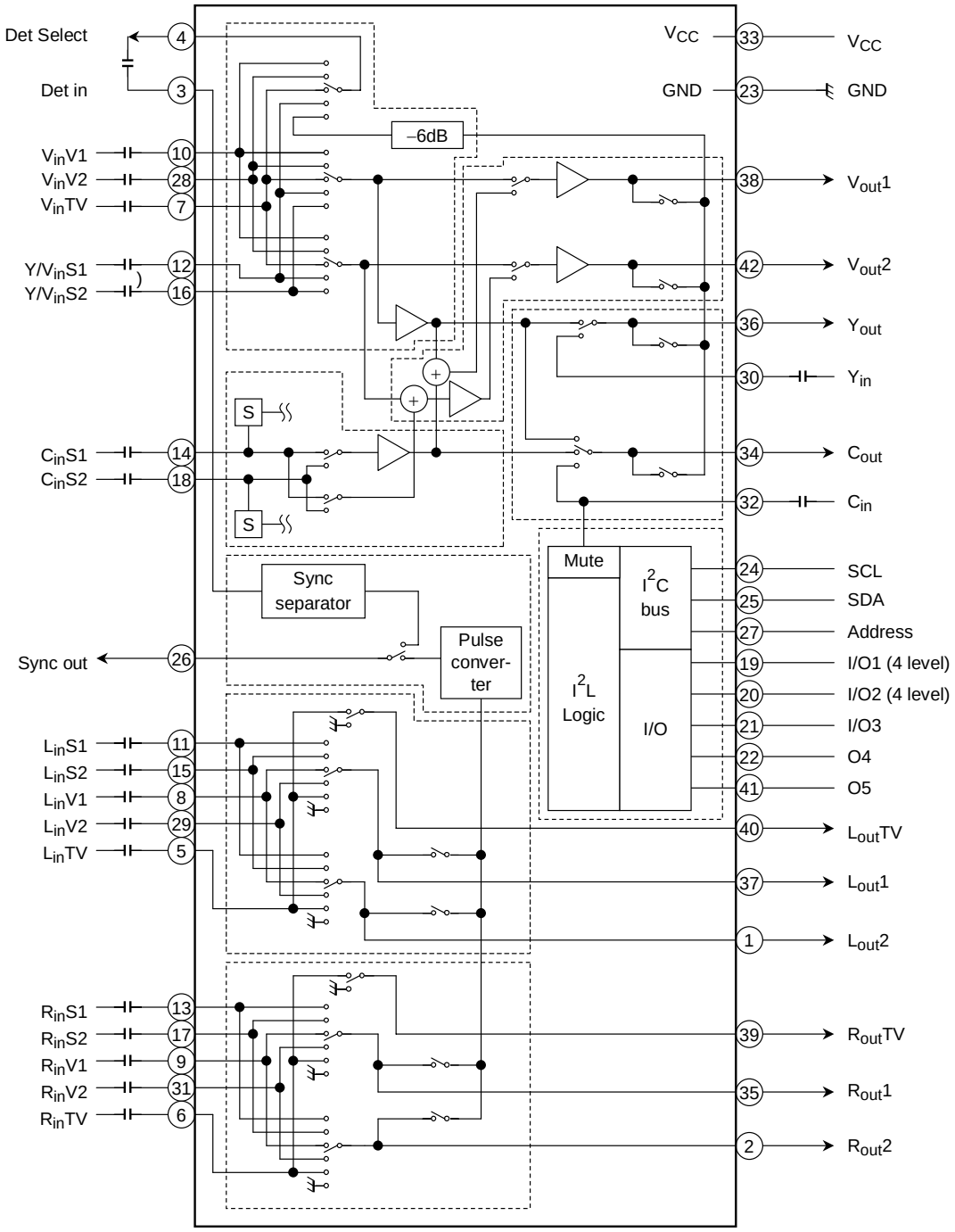
SDIP42-P-600-1.78

Weight: 4.13 g (typ.)

Features

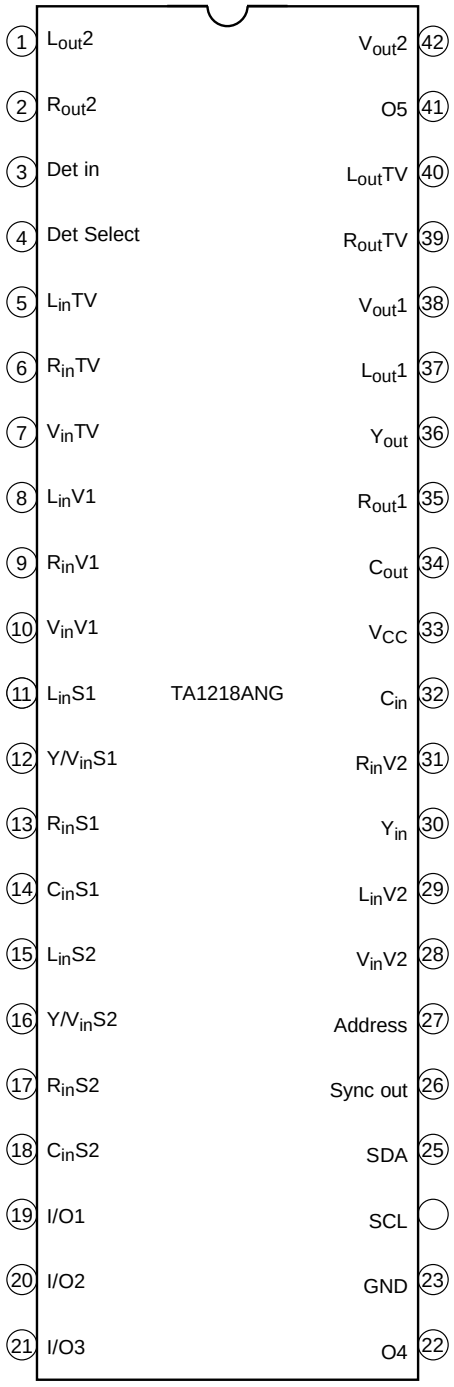
- I^2C bus control
- Video : 5-channel inputs and 2-channel outputs (2 channels conforming to S system)
- Audio : 5-channel inputs and 3-channel outputs
- Self-diagnostic function
- ADC inputs based on European 21-pin standards
- ADC inputs based on S1/S2 terminal standards
- Switchable subaddress

Block Diagram

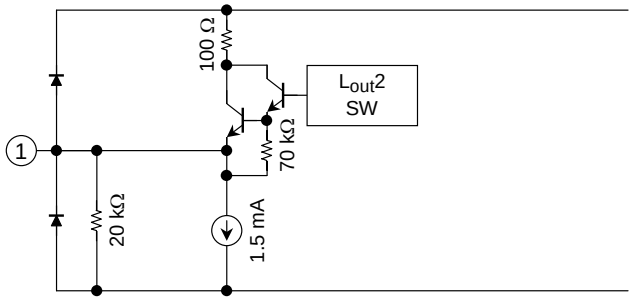
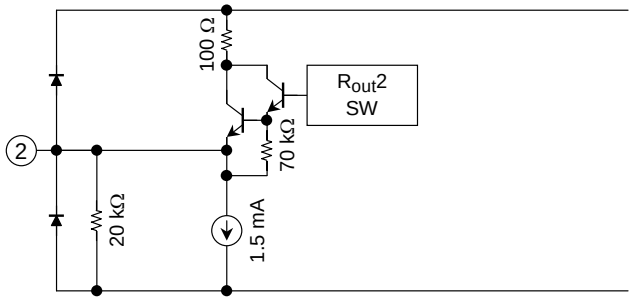
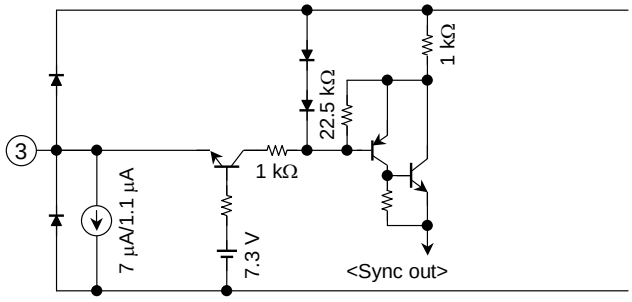
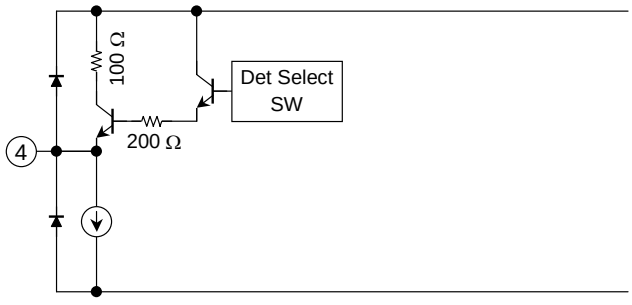


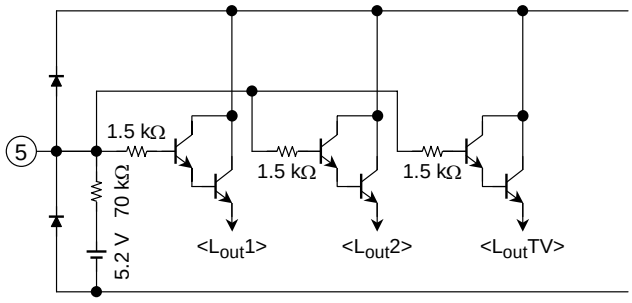
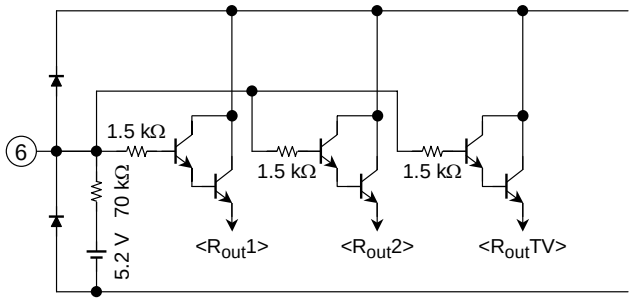
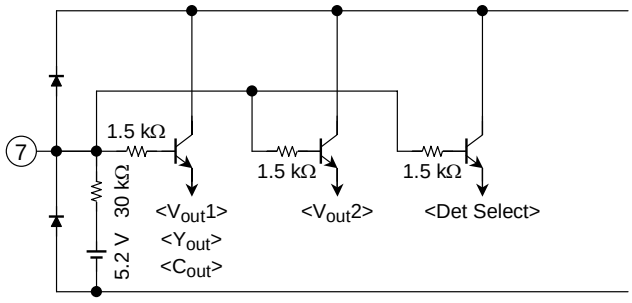
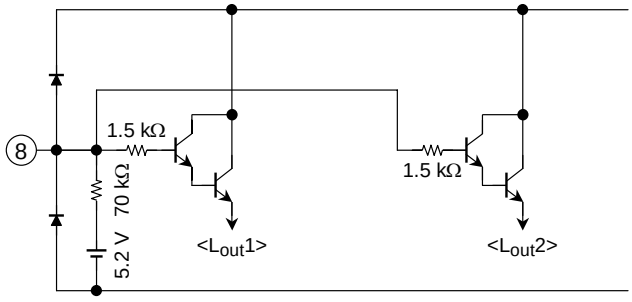
Pin Assignment

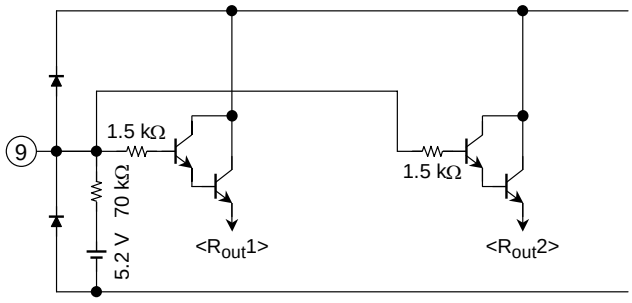
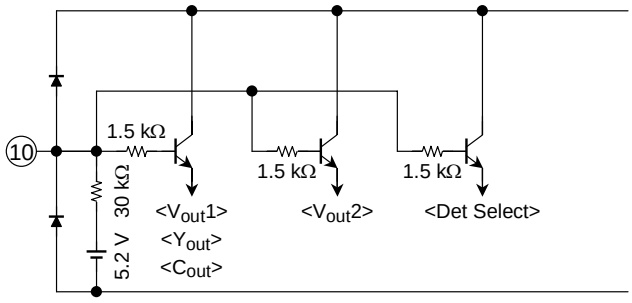
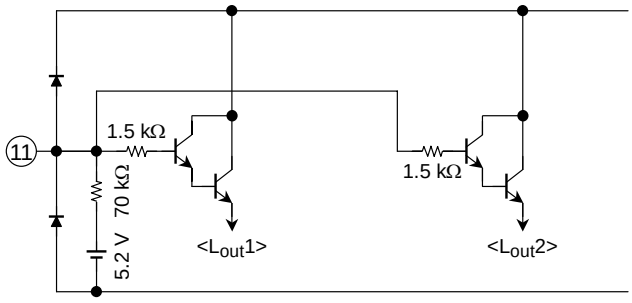
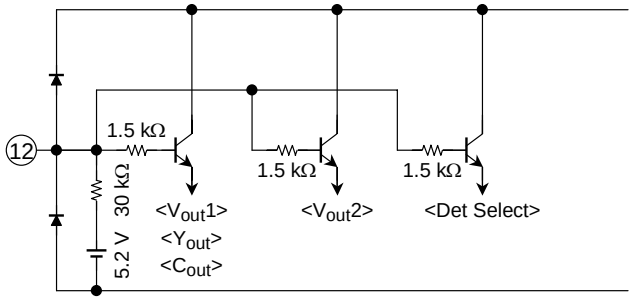
TA1218ANG

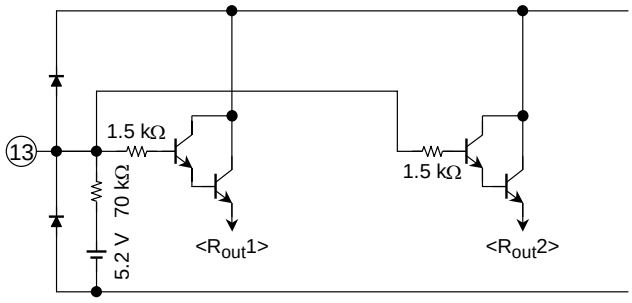
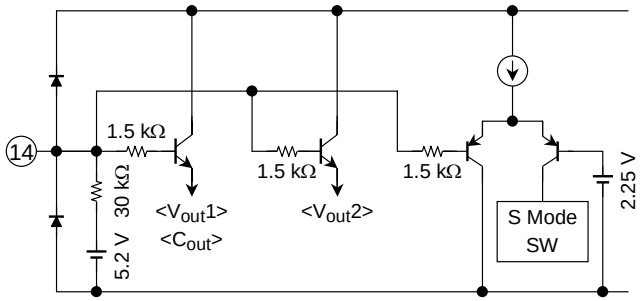
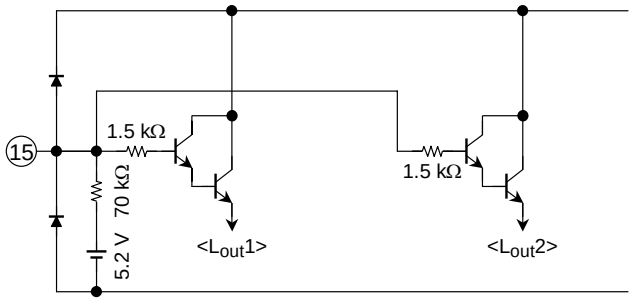
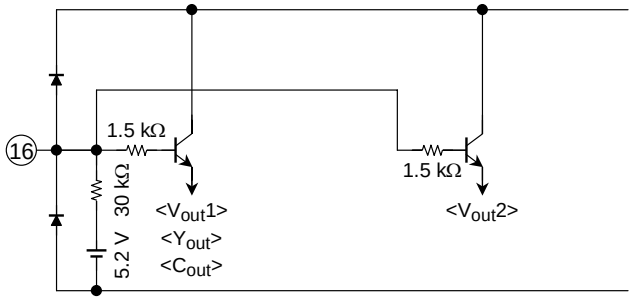


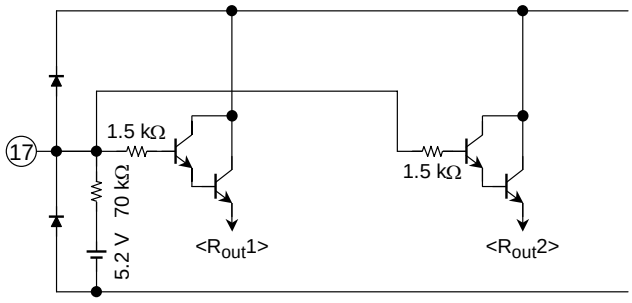
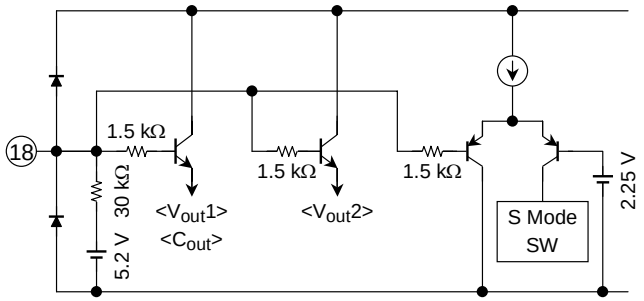
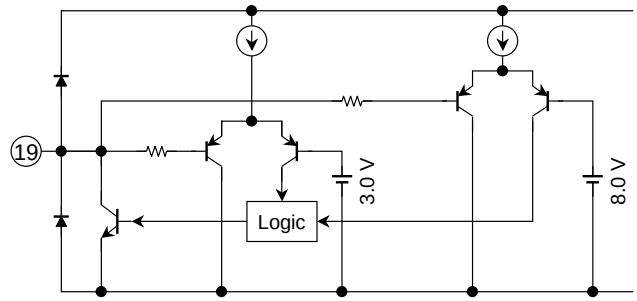
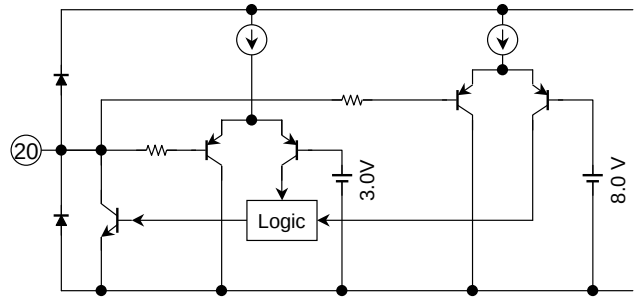
Pin Description

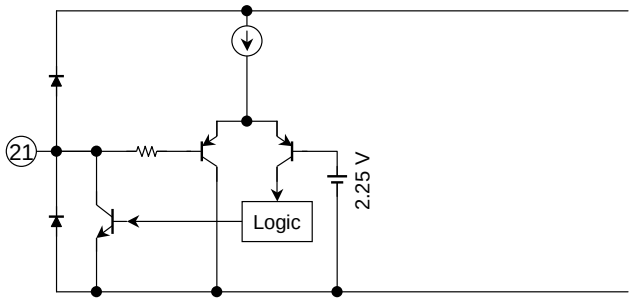
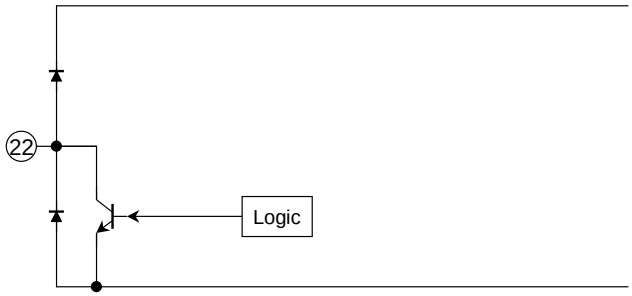
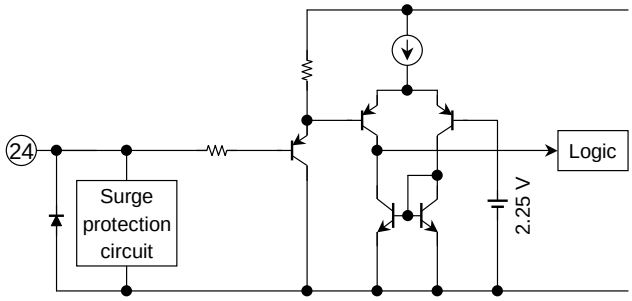
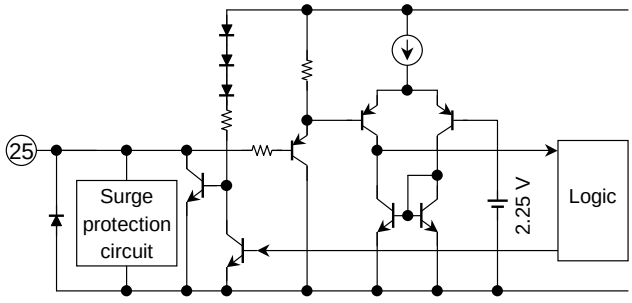
Pin No.	Name	Function	Interface
1	$L_{out}2$	This pin is for output a sub-channel left audio signal. The signals fed into the chip via $L_{in}V1$, $L_{in}V2$, $L_{in}S1$, $L_{in}S2$, or $L_{in}TV$ is output from this pin. The output resistance of this pin is 45 Ω. Furthermore, the signal output from this pin is pulse-converted for use in self-diagnosis. The converted signal is output from Sync Out. This output can be muted in combination with $R_{out}2$ by bus control.	
2	$R_{out}2$	This pin is for output a sub-channel right audio signal. The signals fed into the chip via $R_{in}V1$, $R_{in}V2$, $R_{in}S1$, $R_{in}S2$, or $R_{in}TV$ is output from this pin. The output resistance of this pin is 45 Ω. Furthermore, the signal output from this pin is pulse-converted for use in self-diagnosis. The converted signal is output from Sync Out. This output can be muted in combination with $L_{out}2$ by bus control.	
3	Det in	This pin is for input a sync separation signal. Input the signal from Det Select to this pin with capacitance coupling. The input resistance of this pin is 18 kΩ. The sync signal separated from Det Select is outputted from Sync Out for use in self-diagnosis.	
4	Det Select	This pin is for output a sync separation signal. Signals $V_{in}V1$, $V_{in}V2$, $V_{in}TV$, $Y/V_{in}S1$, $V_{out}1$, $V_{out}2$, Y_{out}, or C_{out} are outputted from this pin. The output resistance of this pin is 35 Ω. Input the signal from this pin to Det in with capacitance coupling.	

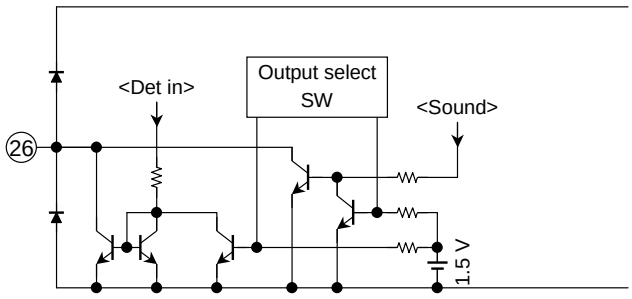
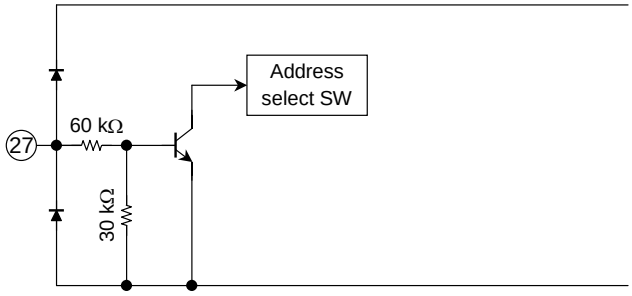
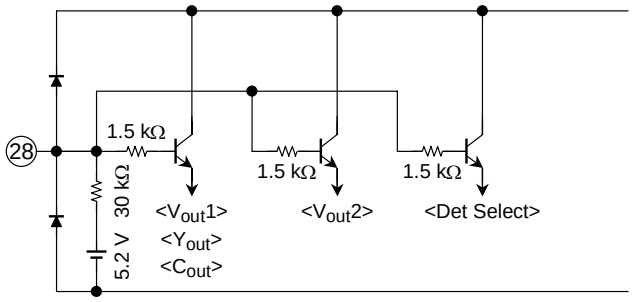
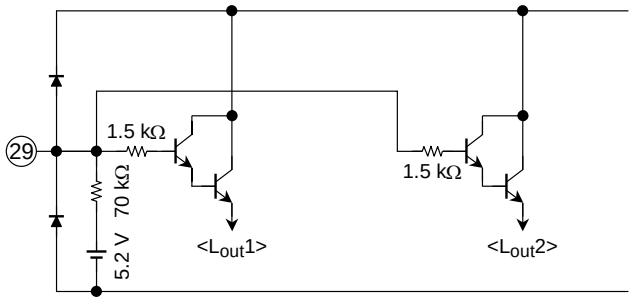
Pin No.	Name	Function	Interface
5	$L_{in}TV$	This pin is for input a left audio signal from the main demodulator in the TV set. The signal fed into this pin is presented to $L_{out}TV$, $L_{out}1$, and $L_{out}2$. The input dynamic range of this pin is 6.5 V_{p-p} and the input resistance is 70 kΩ.	
6	$R_{in}TV$	This pin is for input a right audio signal from the main demodulator in the TV set. The signal fed into this pin is presented to $R_{out}TV$, $R_{out}1$, and $R_{out}2$. The input dynamic range of this pin is 6.5 V_{p-p} and the input resistance is 70 kΩ.	
7	$V_{in}TV$	This pin is for input a composite audio signal from the main demodulator in the TV set. The signal fed into this pin is presented to $V_{out}1$, $V_{out}2$, Y_{out}, and C_{out}. The same signal is also output from Det Select as a sync separation signal. The input dynamic range of this pin is 2.0 V_{p-p} and the input resistance is 30 kΩ.	
8	$L_{in}V1$	This pin is for input a left audio signal from an external source (V1 channel). This pin can also be used for PIP signal input. The signal fed into this pin is presented to $L_{out}1$ and $L_{out}2$. The input dynamic range of this pin is 6.5 V_{p-p} and the input resistance is 70 Ω.	

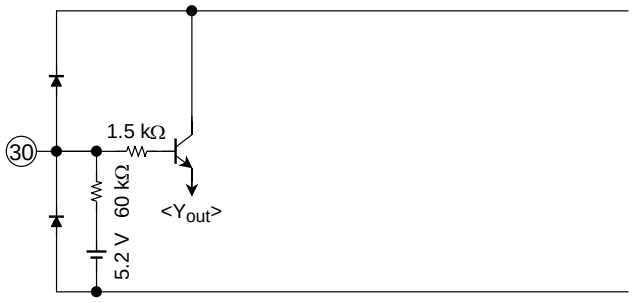
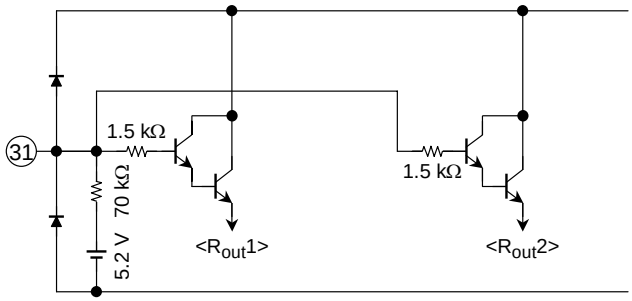
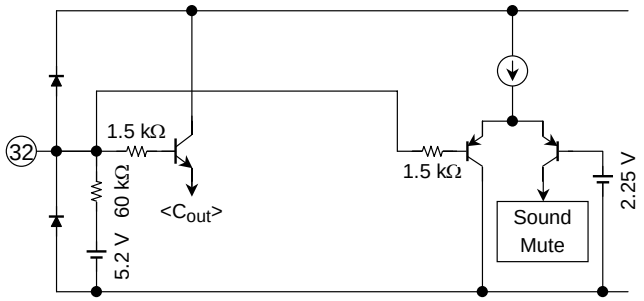
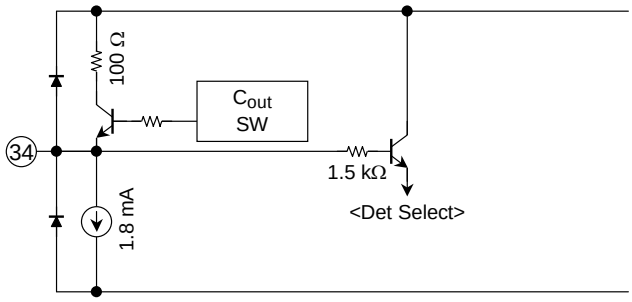
Pin No.	Name	Function	Interface
9	$R_{in}V1$	This pin is for input a right audio signal from an external source (V1 channel). This pin can also be used for PIP signal input. The signal fed into this pin is presented to $R_{out}1$ and $R_{out}2$. The input dynamic range of this pin is 6.5 V_{p-p} and the input resistance is 70 kΩ.	
10	$V_{in}V1$	This pin is for input a composite video signal from an external source (V1 channel). This pin can also be used for PIP signal input. The signal fed into this pin is presented to $V_{out}1$, $V_{out}2$, Y_{out}, and C_{out}. The same signal is also output from Det Select as a sync separation signal. The input dynamic range of this pin is 2.0 V_{p-p} and the input resistance is 30 kΩ.	
11	$L_{in}S1$	This pin is for input a left audio signal from an external source (S1 channel). The signal fed into this pin is presented to $L_{out}1$ and $L_{out}2$. The input dynamic range of this pin is 6.5 V_{p-p} and the input resistance is 70 kΩ.	
12	$Y/V_{in}S1$	This pin is for input a luminance signal or composite video signal from an external source (S1 channel). The signal fed into this pin is presented to $V_{out}1$, $V_{out}2$, Y_{out}, and C_{out}. The same signal is also output from Det Select as a sync separation signal. The input dynamic range of this pin is 2.0 V_{p-p} and the input resistance is 30 kΩ.	

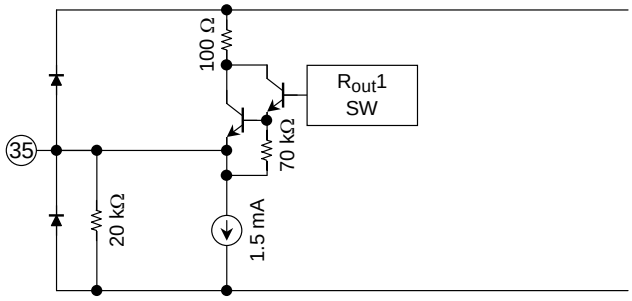
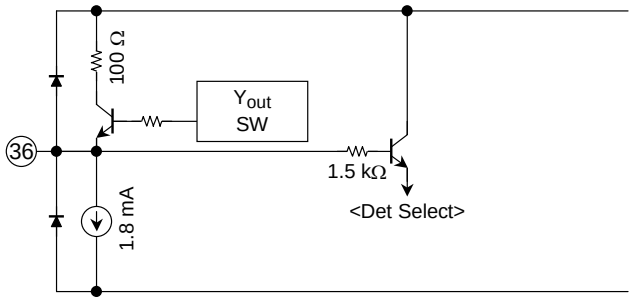
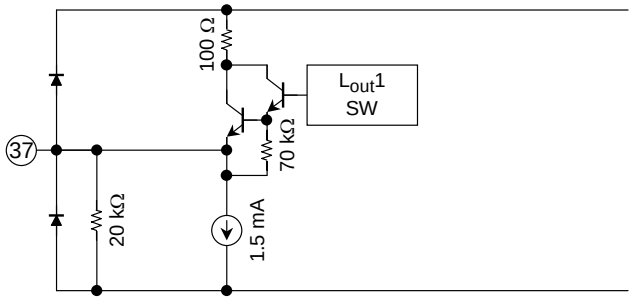
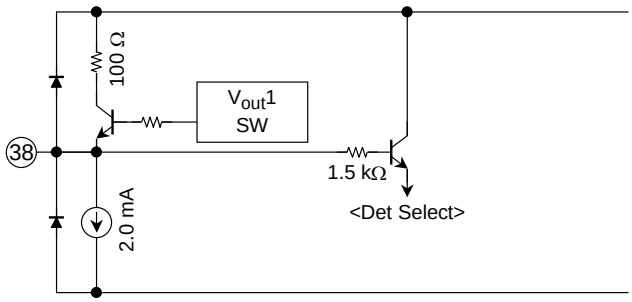
Pin No.	Name	Function	Interface
13	$R_{in}S1$	This pin is for input a right audio signal from an external source (S1 channel). The signal fed into this pin is presented to $R_{out}1$ and $R_{out}2$. The input dynamic range of this pin is 6.5 V_{p-p} and the input resistance is 70 kΩ.	
14	$C_{in}S1$	This pin is for input a chroma signal from an external source (S1 channel). It also functions as an S-mode select switch for the S1 channel. The S mode is selected when the pin voltage is 2.25 V or less. The signal fed into this pin is presented to C_{out} directly and to $V_{out}1$ and $V_{out}2$ after being combined with the $Y_{in}S1$ signal. The input dynamic range of this pin is 2.0 V_{p-p} and the input resistance is 30 kΩ.	
15	$L_{in}S2$	This pin is for input a left audio signal from an external source (S2 channel). The signal fed into this pin is presented to $L_{out}1$ and $L_{out}2$. The input dynamic range of this pin is 6.5 V_{p-p} and the input resistance is 70 kΩ.	
16	$Y/V_{in}S2$	This pin is for input a luminance signal or composite aoudio signal from an external source (S2 channel). The signal fed into this pin is presented to $V_{out}1$, $V_{out}2$, Y_{out}, and C_{out}. The input dynamic range of this pin is 2.0 V_{p-p} and the input resistance is 30 kΩ.	

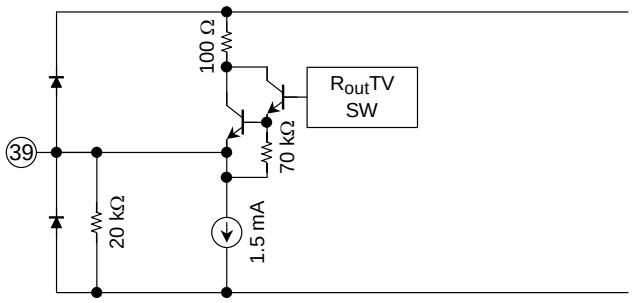
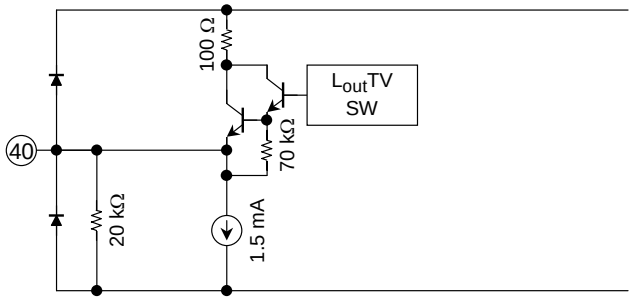
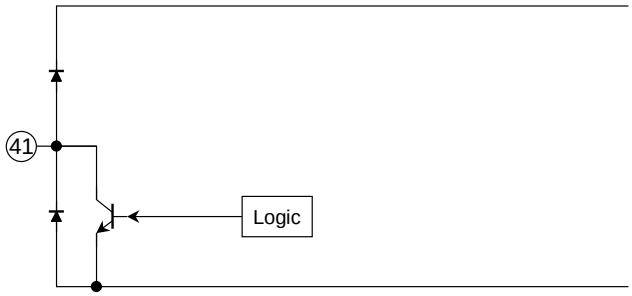
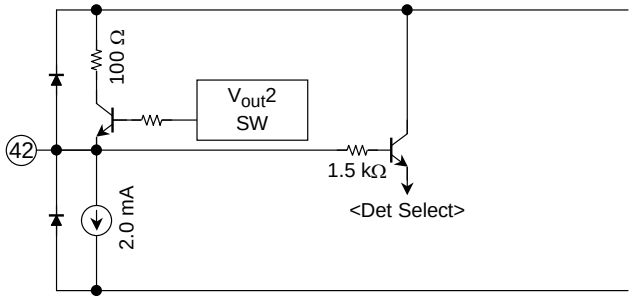
Pin No.	Name	Function	Interface
17	$R_{in}S2$	This pin is for input a right audio signal from an external source (S2 channel). The signal fed into this pin is presented to $R_{out}1$ and $R_{out}2$. The input dynamic range of this pin is 6.5 V_{p-p} and the input resistance is 70 kΩ.	
18	$C_{in}S2$	This pin is for input a chroma signal from an external source (S2 channel). It also functions as an S-mode select switch for the S2 channel. The S mode is selected when the pin voltage is 2.25 V or less. The signal fed into this pin is presented to C_{out} directly and to $V_{out}1$ and $V_{out}2$ after being combined with the $Y_{in}S2$ signal. The input dynamic range of this pin is 2.0 V_{p-p} and the input resistance is 30 kΩ.	
19	I/O1	This is an ADC input/DAC output pin. The ADC is a 4-level detection type (2 bits). The threshold levels are 8.0 V , 3.0 V and 0.75V. The DAC (1 bit) is an open-collector output. Make sure that the current flowing into this pin is 2.0 mA or less.	
20	I/O2	This is an ADC input/DAC output pin. The ADC is a 4-level detection type (2 bits). The threshold levels are 8.0 V, 3.0V and 0.75V. The DAC (1 bit) is an open-collector output. Make sure that the current flowing into this pin is 2.0 mA or less.	

Pin No.	Name	Function	Interface
21	I/O3	This is an ADC input/DAC output pin. The ADC is a 2-level detection type (1 bit). The threshold level is 2.25 V. The DAC (1 bit) is an open-collector output. Make sure that the current flowing into this pin is 2.0 mA or less.	
22	O4	This pin is for a 1 bit DAC output. This is an open-collector output. Make sure that the current flowing into this pin is 2.0 mA or less.	
23	GND	This is the GND pin.	—
24	SCL	This pin is for input an I^2C bus clock. The input threshold level of this pin is 2.25 V.	
25	SDA	This is an I^2C bus data input/output pin. The input threshold level of this pin is 2.25 V. Make sure that the current flowing into this pin is 3.0 mA or less.	

Pin No.	Name	Function	Interface
26	Sync out	This pin is for output a self-diagnostic sync signal. The signal separated from $V_{in}TV$ $V_{in}V1$, $V_{in}V2$, $Y/V_{in}S1$, $V_{out}1$, $V_{out}2$, Y_{out}, or C_{out} is outputted from this pin. In addition, the signal derived from $L_{out}1$, $R_{out}1$, $L_{out}2$, or $R_{out}2$ is also output from this pin for use in audio block diagnosis. This is an open-collector output. Make sure that the current flowing into this pin is 2.0 mA or less.	
27	Address	This is for an I^2C bus slave address select switch. The threshold level of this pin is 2.25 V. The following lists the addresses : High : 92H (write), 93H (read) Low : 90H (write), 91H (read)	
28	$V_{in}V2$	This pin is for input a composite video signal from an external source (V2 channel). This pin can also be used for PIP signal input. The signal fed into this pin is presented to $V_{out}1$, $V_{out}2$, Y_{out}, and C_{out}. The same signal is also output from Det Select as a sync separation signal. The input dynamic range of this pin is 2.0 V_{p-p} and the input resistance is 30 kΩ.	
29	$L_{in}V2$	This pin is for input a left audio signal from an external source (V2 channel). This pin can also be used for PIP signal input. The signal fed into this pin is presented to $L_{out}1$ and $L_{out}2$. The input dynamic range of this pin is 6.5 V_{p-p} and the input resistance is 70 kΩ.	

Pin No.	Name	Function	Interface
30	Y_{in}	This pin is for input a luminance signal from an external comb filter. The signal fed into this pin is presented to Y_{out}. The input dynamic range of this pin is 5.5 V_{p-p} and the input resistance is 60 kΩ.	
31	$R_{in}V2$	This pin is for input a right audio signal from an external source (V2 channel). This pin can also be used for PIP signal input. The signal fed into this pin is presented to $R_{out}1$ and $R_{out}2$. The input dynamic range of this pin is 6.5 V_{p-p} and the input resistance is 70 kΩ.	
32	C_{in}	This pin is for input a chroma signal from an external comb filter. The signal fed into this pin is presented to C_{out}. The input dynamic range of this pin is 5.5 V_{p-p} and the input resistance is 60 kΩ. This pin also functions as a audio mute switch. The entire audio output can be muted by pulling the voltage on this pin below 2.25 V.	
33	V_{CC}	This is the power supply pin. Apply 9 V to this pin. The current consumption of this pin is 47 mA.	—
34	C_{out}	This pin is for output a chroma signal. The signal fed into C_{in}, $C_{in}S1$, $C_{in}S2$, $V_{in}V1$, $V_{in}V2$, $Y/V_{in}S1$, $Y/V_{in}S2$, or $V_{in}TV$ is outputted from this pin. The output resistance of this pin is 25 Ω. The same signal is also outputted from Det Select as a sync separation signal.	

Pin No.	Name	Function	Interface
35	$R_{out}1$	This pin is for output the main channel right audio signal. The signal fed into $R_{in}V1$, $R_{in}V2$, $R_{in}S1$, $R_{in}S2$, or $R_{in}TV$ is outputted from this pin. The output resistance of this pin is 45 Ω. Furthermore, the signal outputted from this pin is pulse-converted for use in self-diagnosis. The converted signal is outputted from Sync Out. This outputted can be muted independently of $L_{out}1$ by bus control.	
36	Y_{out}	This pin is for output a luminance signal. The signal fed into Y_{in}, $Y/V_{in}S1$, $Y/V_{in}S2$, $V_{in}V1$, $V_{in}V2$, or $V_{in}TV$ is outputted from this pin. The output resistance of this pin is 25 Ω. The same signal is also outputted from Det Select as a sync separation signal.	
37	$L_{out}1$	This pin is for output the main channel left audio signal. The signal fed into $L_{in}V1$, $L_{in}V2$, $L_{in}S1$, $L_{in}S2$, or $L_{in}TV$ is outputted from this pin. The output resistance of this pin is 45 Ω. Furthermore, the signal outputted from this pin is pulse-converted for use in self-diagnosis. The converted signal is outputted from Sync Out. This output can be muted independently of $R_{out}1$ by bus control.	
38	$V_{out}1$	This pin is for output the main channel composite video signal. The signal fed into $V_{in}TV$, $V_{in}V1$, $V_{in}V2$, $V_{in}S1$, $V_{in}S2$, $Y_{in}S1 + C_{in}S1$, or $Y_{in}S2 + C_{in}S2$ is outputted from this pin. The output resistance of this pin is 25 Ω The same signal is also outputted from Det Select as a sync separation signal.	

Pin No.	Name	Function	Interface
39	$R_{out}TV$	This pin is for output only the signal that is forwarded from $R_{in}TV$. The output resistance of this pin is 45 Ω. This output can be muted in combination with $L_{out}TV$ by bus control.	
40	$L_{out}TV$	This pin is for output only the signal that is forwarded from $L_{in}TV$. The output resistance of this pin is 45 Ω. This output can be muted in combination with $R_{out}TV$ by bus control.	
41	O5	This is a 1 bit DAC output pin. This is an open-collector output. Make sure that the current flowing into this pin is 2.0 mA or less.	
42	$V_{out}2$	This pin is for output a sub-channel composite video signal. The signal fed into $V_{in}TV$, $V_{in}V1$, $V_{in}V2$, $V_{in}S1$, $V_{in}S2$, $Y_{in}S1 + C_{in}S1$, or $Y_{in}S2 + C_{in}S2$ is outputted from this pin. The output resistance of this pin is 25 Ω. The same signal is also outputted from Det Select as a sync separation signal.	

Bus Data Specifications

Data Structure

(1) Write

S	Slave address (90H or 92H)	W (0)	A	Data 1	A	Data 2	A	Data 3	A	P

(2) Read

S	Slave address (91H or 93H)	R (1)	A	Data 4	A	P

Note2: Slave address is switched by the voltage applied to pin 27 (address). Switched to 90H when low (GND); switched to 92H when high (V_{CC}) during write mode.

Contents of Data

Mode	Data No.	Contents of Data							
Write	Data 1 [F0H]	B07	B06	B05	B04	B03	B02	B01	B00
		Audio mute				Forced TV Audio		YC output switching	
		$L_{out}TV$ $R_{out}TV$	$L_{out}2$ $R_{out}2$	$R_{out}1$	$L_{out}1$			Y_{out}	C_{out}
	Data 2 [1FH]	B17	B16	B15	B14	B13	B12	B11	B10
		Sync detection sensitivity switching	Sync output switching	Sync (diagnosis) detection switching			Input select (main)		
	Data 3 [07H]	B27	B26	B25	B24	B23	B22	B21	B20
		DAC output switching					Input select (sub)		
		O5	O4	I/O3	I/O2	I/O1			
Read	Data 4	B37	B36	B35	B34	B33	B32	B31	B30
		ADC input discrimination					S input discrimination		Power-on reset
		I/O3	I/O2 Hi	I/O2 Low	I/O1 Hi	I/O1 Low	$C_{in}S1$	$C_{in}S2$	

Note3: Shown in [ ] are reset data.

Note4: The data contents marked by a slash (/) are an unused bit (data free).

Main Video Select: Terminal 38 Output Signal

Mode		Output Signal	S Input Discrimination		Bus Data		
					Input Select (main)		
Input	S/V	$V_{out}1$	CS1	CS2	B12	B11	B10
S1	V	$Y/V_{in}S1$	Low	*	0	0	0
	S	$Y/V_{in}S1 + C_{in}S1$	Open				
	FV	$Y/V_{in}S1$					1
S2	V	$Y/V_{in}S2$	*	Low	0	1	0
	S	$Y/V_{in}S2 + C_{in}S2$		Open			
	FV (Note5)	$Y/V_{in}S2$					1
V1	V	$V_{in}V1$	*	*	1	0	1
V2	V	$V_{in}V2$	*	*	1	1	0
TV	V	$V_{in}TV$	*	*	1	1	1

Do not use [100] for the input select data.

Note5: FV: Forced Video Mode.

Main L/R Select: Terminal 37 and 35 Output Signal

Mode	Main L/R Output Signal		Bus Data			
			Forced TV Voice	Input Select (main)		
Input	$L_{out}1$	$R_{out}1$	B03	B12	B11	B10
S1	$L_{in}S1$	$R_{in}S1$	0	0	0	*
S2	$L_{in}S2$	$R_{in}S2$		0	1	*
V1	$L_{in}V1$	$R_{in}V1$		1	0	1
V2	$L_{in}V2$	$R_{in}V2$		1	1	0
TV	$L_{in}TV$	$R_{in}TV$		1	1	1
TV	$L_{in}TV$	$R_{in}TV$	1	*	*	*

Do not use [100] for the input select data.

Sub (PIP) Video Select: Terminal 42 Output Signal

Mode		Output Signal	S Input Discrimination		Bus Data		
					Input Select (sub)		
INPUT	S/V	V_{out2}			B22	B21	B20
S1	V	$Y/V_{in}S1$	Low	*	0	0	0
	S	$Y/V_{in}S1 + C_{in}S1$	Open				
	FV	Y/VinS1					1
S2	V	$Y/V_{in}S2$	*	Low	0	1	0
	S	$Y/V_{in}S2 + C_{in}S2$		Open			
	FV	$Y/V_{in}S2$					1
V1	V	$V_{in}1$	*	*	1	1	1
V2	V	$V_{in}2$	*	*	1	1	0
TV	V	$V_{in}TV$	*	*	1	1	1

Do not use [100] for the input select data.

Sub L/R Select: Terminal 1 and 2 Output Signal

Mode	SUB L/R Output Signal		Bus Data			
			Forced TV Voice	Input Select (sub)		
Input	L_{out2}	R_{out2}	B03	B22	B21	B20
S1	$L_{in}S1$	$R_{in}S1$	0	0	0	*
S2	$L_{in}S2$	$R_{in}S2$		0	1	*
V1	$L_{in}V1$	$R_{in}V1$		1	0	1
V2	$L_{in}V2$	$R_{in}V2$		1	1	0
TV	$L_{in}TV$	$R_{in}TV$		1	1	1
TV	$L_{in}TV$	$R_{in}TV$	1	*	*	*

Do not use [100] for the input select data.

Y Output Select: Terminal 30 Output Signal

Mode		Y Output Signal	Main V Select Mode (see table 2-2.)		Bus Data
					Y Output Switching
Input	Through	Y_{out}			B01
S1	Y_{in}	Y_{in}	S1	V or FV	0
	V through	$Y/V_{in}S1$			1
	Y through	$Y/V_{in}S1$		S	*
S2	Y_{in}	Y_{in}	S2	V or FV	0
	V through	$Y/V_{in}S2$			1
	Y through	$Y/V_{in}S2$		S	*
V1	Y_{in}	Y_{in}	V1	V	0
	V through	$V_{in}V1$			1
V2	Y_{in}	Y_{in}	V2	V	0
	V through	$V_{in}V2$			1
TV	Y_{in}	Y_{in}	TV	V	0
	V through	$V_{in}TV$			1

C Output Select: Terminal 34 Output Signal

Mode		Y Output Signal	Main V Select Mode (see table 2-2.)		Bus Data
					C Output Switching
Input	Through	C_{out}			B00
S1	C_{in}	C_{in}	S1	V or FV	0
	V through	$Y/V_{in}S1$			1
	C through	$C_{in}S1$		S	*
S2	C_{in}	C_{in}	S2	V or FV	0
	V through	$Y/V_{in}S2$			1
	C through	$C_{in}S2$		S	*
V1	C_{in}	C_{in}	V1	V	0
	V through	$V_{in}V1$			1
V2	C_{in}	C_{in}	V2	V	0
	V through	$V_{in}V2$			1
TV	C_{in}	C_{in}	TV	V	0
	V through	$V_{in}TV$			1

Sync Detection Select: Terminal 4 Output Signal

Mode		Detection Select	Sync Output	Bus Data			
				Sync Switching	Sync Detection Switching		
		Det Select	Sync Out	B16	B15	B14	B13
Video Input	TV	V_{in}TV	Sync	0	0	1	1
	V1	V_{in}V1				0	1
	V2	V_{in}V2				1	0
	S1	Y/V_{in}S1				0	0
Video Output	V_{out}1	V_{out}1	Sync	0	1	1	1
	V_{out}2	V_{out}2				0	1
	Y_{out}	Y_{out}				1	0
	C_{out}	C_{out}				0	0
Audio Output	R_{out}1	★	R_{out}1	1	*	1	1
	L_{out}1	★	L_{out}1			0	1
	R_{out}2	★	R_{out}2			1	0
	L_{out}2	★	L_{out}2			0	0

For Det Select marked by ★, the video input or video output corresponding to data B15, B14, and B13 is selected.

Sync Detection Sensitivity Switching

Mode		Bus Data
		Detection Sensitivity Switching
		B17
Sensitivity	High	1
	Low	0

Audio Mute

Mode		Bus Data			
		Audio Mute			
Output	Mute	B07	B06	B05	B04
$L_{out}1$	off	*	*	*	0
	on				1
$R_{out}1$	off	*	*	0	*
	on			1	
$L_{out}2$	off	*	0	*	*
$R_{out}2$	on		1		
$L_{out}TV$	off	0	*	*	*
$R_{out}TV$	on	1			

DAC Output Switching

Mode		Bus Data				
		DAC Output Switching				
Output	State	B27	B26	B25	B24	B23
I/O1	Open	*	*	*	*	0
	Low					1
I/O2	Open	*	*	*	0	*
	Low				1	
I/O3	Open	*	*	0	*	*
	Low			1		
O4	Open	*	0	*	*	*
	Low		1			
O5	Open	0	*	*	*	*
	Low	1				

Read Mode

Power-On Reset Discrimination

Mode		Bus Data
		Power-On Reset
		B30
Reset	on	1
	off	0

S Input Discrimination

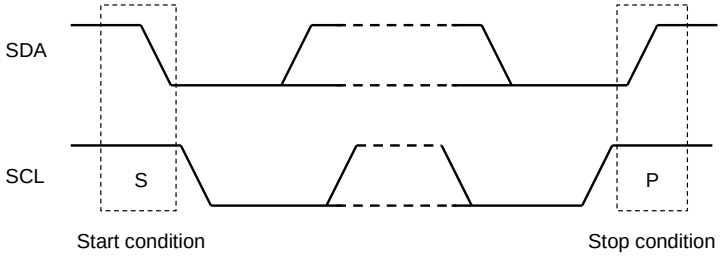
Mode		Bus Data	
		S Input Discrimination	
Input	Voltage	B32	B31
$C_{in}S2$	High (open)	*	1
	Low		0
$C_{in}S1$	High (open)	1	*
	Low	0	

ADC Input Discrimination

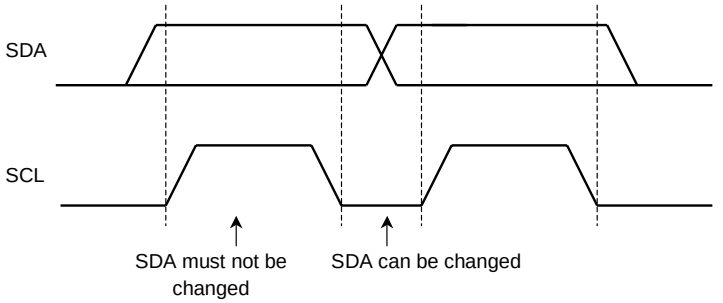
Mode		Bus Data				
		ADC Input Discrimination				
Input	Voltage	B37	B36	B35	B34	B33
I/O1	High	*	*	*	0	0
	Mid				1	0
	Low				0	1
	bottom				1	1
I/O2	High	*	0	0	*	*
	Mid		1	0		
	Low		0	1		
	bottom		1	1		
I/O3	High	0	*	*	*	*
	Low	1				

Outline of I^2C Bus Control Format

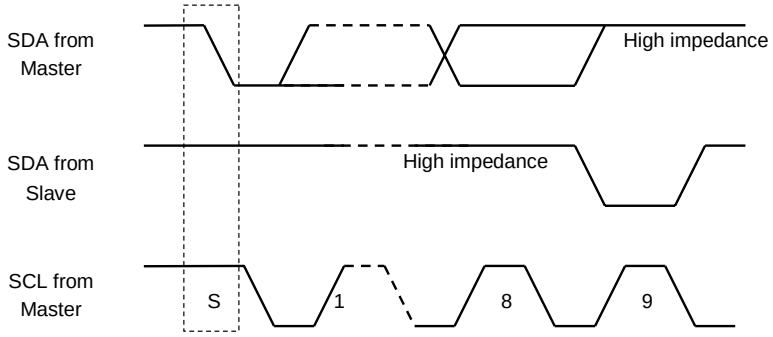
(1) Start and stop conditions



(2) Bit transfer



(3) Acknowledgement



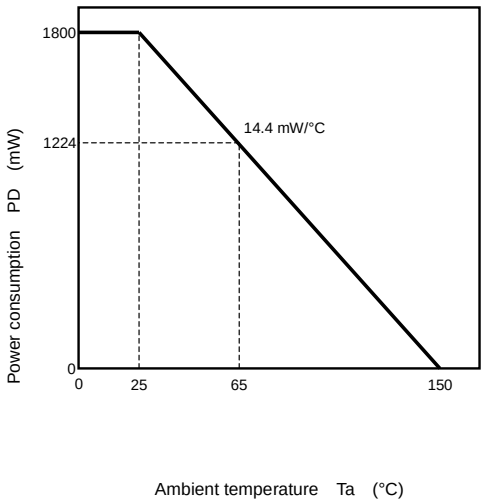
I^2C BUS Conditions

Characteristics	Symbol	Min	Typ.	Max	Unit
Low level input voltage	V_{IL}	0	–	1.5	V
High level input voltage	V_{IH}	3.0	–	Vcc	V
Low level output voltage at 3 mA sink current	V_{OL1}	0	–	0.4	V
Input current each I/O pin with an input voltage between 0.1 VDD and 0.9 VDD	I_i	-10	–	10	μA
Capacitance for each I/O pin	C_i	–	–	10	pF
SCL clock frequency	f_{SCL}	0	–	100	kHz
Hold time START condition	$t_{HD;STA}$	4.0	–	–	μs
Low period of SCL clock	t_{LOW}	4.7	–	–	μs
High period of SCL clock	t_{HIGH}	4.0	–	–	μs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	–	–	μs
Data hold time	$t_{HD;DAT}$	500	–	–	ns
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	–	–	μs
Bus free time between a STOP and START condition	t_{BUF}	4.7	–	–	μs

Maximum Ratings

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	14	V
Power dissipation	P_{DMAX} (Note6)	1800	mW
Input pin voltage	V_{in}	GND – 0.3 to Vcc + 0.3	V
Operating temperature	T_{opr}	−20 to 65	°C
Storage temperature	T_{stg}	−55 to 150	°C

Note6: When using the device at temperatures above Ta = 25°C, reduce the rated power dissipation by 14.4 mW per degree of centigrade. (see the diagram below.)



Operating Conditions

Characteristics	Test Condition	Min	Typ.	Max	Unit	Remark
Supply voltage	33	8.1	9.0	9.9	V	—
Composite signal input amplitude	7, 10, 12, 16, 28	—	1.0	—	V_{p-p}	100IRE
Y input amplitude	12, 16	—	1.0	—	V_{p-p}	100IRE
Comb Y input amplitude	30	—	2.0	—	V_{p-p}	—
Chroma input amplitude	14, 18	—	286	—	mV_{p-p}	Burst
Comb chroma input amplitude	32	—	572	—	mV_{p-p}	Burst
Audio input amplitude	5, 6, 8, 9, 11, 13, 15, 17, 29, 31	—	—	6.0	V_{p-p}	—

Electrical Characteristics
(referenced to V_{CC} = 9 V at Ta = 25°C unless otherwise specified)

Current Consumption

Pin No.	Pin Name	Symbol	Test Circuit	Min	Typ.	Max	Unit
33	V_{CC}	I_{CC}	—	30	47	64	mA

Pin Voltage

Pin No.		Pin Name	Symbol	Test Circuit	Min	Typ.	Max	Unit
N	F							
1	43	$L_{out}2$	V1	—	3.7	4.0	4.3	V
2	44	$R_{out}2$	V2	—	3.7	4.0	4.3	V
3	45	Det in	V3	—	6.3	6.6	6.9	V
4	46	Det Select	V4	—	3.4	3.7	4.0	V
5	47	$L_{in}TV$	V5	—	5.0	5.2	5.4	V
6	48	$R_{in}TV$	V6	—	5.0	5.2	5.4	V
7	2	$V_{in}TV$	V7	—	5.0	5.2	5.4	V
8	3	$L_{in}V1$	V8	—	5.0	5.2	5.4	V
9	5	$R_{in}V1$	V9	—	5.0	5.2	5.4	V
10	6	$V_{in}V1$	V10	—	5.0	5.2	5.4	V
11	7	$L_{in}S1$	V11	—	5.0	5.2	5.4	V
12	8	$Y/V_{in}S1$	V12	—	5.0	5.2	5.4	V
13	9	$R_{in}S1$	V13	—	5.0	5.2	5.4	V
14	10	$C_{in}S1$	V14	—	5.0	5.2	5.4	V
15	11	$L_{in}S2$	V15	—	5.0	5.2	5.4	V
16	12	$Y/V_{in}S2$	V16	—	5.0	5.2	5.4	V
17	13	$R_{in}S2$	V17	—	5.0	5.2	5.4	V
18	15	$C_{in}S2$	V18	—	5.0	5.2	5.4	V
23	21	GND	V23	—	—	0	—	V
28	26	$V_{in}V2$	V28	—	5.0	5.2	5.4	V
29	27	$L_{in}V2$	V29	—	5.0	5.2	5.4	V
30	28	Y_{in}	V30	—	5.0	5.2	5.4	V
31	29	$R_{in}V2$	V31	—	5.0	5.2	5.4	V
32	30	C_{in}	V32	—	5.0	5.2	5.4	V
33	33	V_{CC}	V33	—	—	9.0	—	V
34	34	C_{out}	V34	—	3.5	3.8	4.1	V
35	35	$R_{out}1$	V35	—	3.7	4.0	4.3	V
36	36	Y_{out}	V36	—	3.5	3.8	4.1	V
37	37	$L_{out}1$	V37	—	3.7	4.0	4.3	V
38	38	$V_{out}1$	V38	—	4.1	4.4	4.7	V
39	39	$R_{out}TV$	V39	—	3.7	4.0	4.3	V
40	40	$L_{out}TV$	V40	—	3.7	4.0	4.3	V
42	42	$V_{out}2$	V42	—	4.1	4.4	4.7	V

DC Characteristics

Characteristics	Measured Pin	Symbol	Test Circuit	Min.	Typ.	Max.	Unit	Remark
Input pin Input resistance	Det in	R3	—	10	18	30	kΩ	Measure a change ΔI in the current flowing into each pin when the voltage is raised by 0.5V. Then calculate the input resistance value R. R = 0.5 V/ΔI [Ω]
	V_{in}TV	R7	—	20	30	40	kΩ	
	V_{in}V1	R10	—	20	30	40	kΩ	
	V_{in}V2	R28	—	20	30	40	kΩ	
	Y/V_{in}S1	R12	—	20	30	40	kΩ	
	Y/V_{in}S2	R16	—	20	30	40	kΩ	
	C_{in}S1	R14	—	20	30	40	kΩ	
	C_{in}S2	R18	—	20	30	40	kΩ	
	Y_{in}	R30	—	40	60	80	kΩ	
	C_{in}	R32	—	40	60	80	kΩ	
	L_{in}TV	R5	—	49	70	100	kΩ	
	R_{in}TV	R6	—	49	70	100	kΩ	
	L_{in}V1	R8	—	49	70	100	kΩ	
	R_{in}V1	R9	—	49	70	100	kΩ	
	L_{in}V2	R29	—	49	70	100	kΩ	
	R_{in}V2	R31	—	49	70	100	kΩ	
	L_{in}S1	R11	—	49	70	100	kΩ	
	R_{in}S1	R13	—	49	70	100	kΩ	
	L_{in}S2	R15	—	49	70	100	kΩ	
	R_{in}S2	R17	—	49	70	100	kΩ	
Output pin Output resistance	Det Select	R4	—	17	35	53	Ω	Measure a voltage change ΔV on each pin when a current of 100 μA flows into the pin. Then calculate the output resistance value R. R = ΔV/100 μA [Ω]
	V_{out}1	R38	—	13	25	50	Ω	
	V_{out}2	R42	—	13	25	50	Ω	
	Y_{out}	R36	—	13	25	50	Ω	
	C_{out}	R34	—	13	25	50	Ω	
	L_{out}TV	R40	—	20	45	90	Ω	
	R_{out}TV	R39	—	20	45	90	Ω	
	L_{out}1	R37	—	20	45	90	Ω	
	R_{out}1	R35	—	20	45	90	Ω	
	L_{out}2	R1	—	20	45	90	Ω	
	R_{out}2	R2	—	20	45	90	Ω	
S mode discrimination voltage	C_{in}S1	VthC1	—	1.75	2.25	2.75	V	Voltage on pin 14 at which data B31 changes.
	C_{in}S2	VthC2	—	1.75	2.25	2.75	V	Voltage on pin 18 at which data B32 changes.
External mute ON voltage	C_{in}	VthM	—	1.75	2.25	2.75	V	Voltage on pin 32 at which voice is muted.
Address switching voltage	Address	VthA	—	1.75	2.25	2.75	V	Voltage on pin 27 at which the slave address changes.

Characteristics	Measured Pin	Symbol	Test Circuit	Min.	Typ.	Max.	Unit	Remark
ADC input discrimination voltage	I/O1	VthI1L	—	0.55	0.75	0.95	V	Low-bottom threshold level of I/O1 input (pin 19).
	I/O1	VthI1M	—	2.5	3.0	3.5	V	Mid-Low threshold level of I/O1 input (pin 19).
	I/O1	Vthl1H	—	7.5	8.0	8.5	V	High-Mid threshold level of I/O1 input (pin 19)
	I/O2	VthI2L	—	1.75	2.25	2.75	V	Low-bottom threshold level of I/O2 input (pin 20).
	I/O2	Vthl2M	—	2.5	3.0	3.5	V	Mid-Low threshold level of I/O2 input(pin 20)
	I/O2	VthI2H	—	7.5	8.0	8.5	V	High-Mid threshold level of I/O2 input (pin 20).
	I/O3	VthI3	—	1.75	2.25	2.75	V	Hig-Low threshold level of I/O3 input (pin 21).

AC Characteristics

Characteristics	Select Mode	Symbol	Test Circuit	Min.	Typ.	Max.	Unit	Test Method
$V_{out}1$ Input dynamic range	$V_{in}TV$	VDR7V1	—	1.5	2.0	—	V_{p-p}	(1) Apply a 15 kHz sine wave to each input pin. (2) In each select mode, measure an input amplitude at which the output waveform on pin 38 begins to be distorted.
	$V_{in}V1$	VDR10V1	—	1.5	2.0	—	V_{p-p}	
	$V_{in}V2$	VDR28V1	—	1.5	2.0	—	V_{p-p}	
	$Y/V_{in}S1$	VDR12V1	—	1.5	2.0	—	V_{p-p}	
	$C_{in}S1$	VDR14V1	—	1.5	2.0	—	V_{p-p}	
	$Y/V_{in}S2$	VDR16V1	—	1.5	2.0	—	V_{p-p}	
	$C_{in}S2$	VDR18V1	—	1.5	2.0	—	V_{p-p}	
$V_{out}1$ Gain	$V_{in}TV$	G7V1	—	5.5	6.0	6.5	dB	(1) Apply a 15 kHz, 1.0 V_{p-p} sine wave to each input pin. (2) In each select mode, find the gain between input and output.
	$V_{in}V1$	G10V1	—	5.5	6.0	6.5	dB	
	$V_{in}V2$	G28V1	—	5.5	6.0	6.5	dB	
	$Y/V_{in}S1$	G12V1	—	5.5	6.0	6.5	dB	
	$C_{in}S1$	G14V1	—	5.5	6.0	6.5	dB	
	$Y/V_{in}S2$	G16V1	—	5.5	6.0	6.5	dB	
	$C_{in}S2$	G18V1	—	5.5	6.0	6.5	dB	
$V_{out}1$ Frequency response	$V_{in}TV$	F7V1	—	10	—	—	MHz	(1) Apply a 1.0 V_{p-p} sine wave to each input pin. (2) In each select mode, measure a frequency at which the output amplitude on pin 38 is 3dB down from the 15 kHz applied level.
	$V_{in}V1$	F10V1	—	10	—	—	MHz	
	$V_{in}V2$	F28V1	—	10	—	—	MHz	
	$Y/V_{in}S1$	F12V1	—	10	—	—	MHz	
	$C_{in}S1$	F14V1	—	10	—	—	MHz	
	$Y/V_{in}S2$	F16V1	—	10	—	—	MHz	
	$C_{in}S2$	F18V1	—	10	—	—	MHz	
$V_{out}1$ Crosstalk	$V_{in}TV$	CT7V1	—	55	60	—	dB	(1) Apply a 3.58 MHz, 1.0 V_{p-p} sine wave to each input pin. (2) In each select mode, compare signal output from the selected pin with leakage components from nonselected pins to find a crosstalk.
	$V_{in}V1$	CT10V1	—	55	60	—	dB	
	$V_{in}V2$	CT28V1	—	55	60	—	dB	
	$Y/V_{in}S1$	CT12V1	—	55	60	—	dB	
	$C_{in}S1$	CT14V1	—	55	60	—	dB	
	$Y/V_{in}S2$	CT16V1	—	55	60	—	dB	
	$C_{in}S2$	CT18V1	—	55	60	—	dB	
$V_{out}2$ Input dynamic range	$V_{in}TV$	VDR7V2	—	1.5	2.0	—	V_{p-p}	(1) Apply a 15 kHz sine wave to each input pin. (2) In each select mode, measure an input amplitude at which the output waveform on pin 42 begins to be distorted.
	$V_{in}V1$	VDR10V2	—	1.5	2.0	—	V_{p-p}	
	$V_{in}V2$	VDR28V2	—	1.5	2.0	—	V_{p-p}	
	$Y/V_{in}S1$	VDR12V2	—	1.5	2.0	—	V_{p-p}	
	$C_{in}S1$	VDR14V2	—	1.5	2.0	—	V_{p-p}	
	$Y/V_{in}S2$	VDR16V2	—	1.5	2.0	—	V_{p-p}	
	$C_{in}S2$	VDR18V2	—	1.5	2.0	—	V_{p-p}	

Characteristics	Select Mode	Symbol	Test Circuit	Min.	Typ.	Max.	Unit	Test Method
$V_{out}2$ Gain	$V_{in}TV$	G7V2	—	5.5	6.0	6.5	dB	(1) Apply a 15 kHz, 1.0 V_{p-p} sine wave to each input pin. (2) In each select mode, find the gain between input and output.
	$V_{in}V1$	G10V2	—	5.5	6.0	6.5	dB	
	$V_{in}V2$	G28V2	—	5.5	6.0	6.5	dB	
	$Y/V_{in}S1$	G12V2	—	5.5	6.0	6.5	dB	
	$C_{in}S1$	G14V2	—	5.5	6.0	6.5	dB	
	$Y/V_{in}S2$	G16V2	—	5.5	6.0	6.5	dB	
	$C_{in}S2$	G18V2	—	5.5	6.0	6.5	dB	
$V_{out}2$ Frequency response	$V_{in}TV$	F7V2	—	10	—	—	MHz	(1) Apply a 1.0 V_{p-p} sine wave to each input pin. (2) In each select mode, measure a frequency at which the output amplitude on pin 42 is 3dB down from the 15 kHz applied level.
	$V_{in}V1$	F10V2	—	10	—	—	MHz	
	$V_{in}V2$	F28V2	—	10	—	—	MHz	
	$Y/V_{in}S1$	F12V2	—	10	—	—	MHz	
	$C_{in}S1$	F14V2	—	10	—	—	MHz	
	$Y/V_{in}S2$	F16V2	—	10	—	—	MHz	
	$C_{in}S2$	F18V2	—	10	—	—	MHz	
$V_{out}2$ Crosstalk	$V_{in}TV$	CT7V2	—	55	60	—	dB	(1) Apply a 3.58 MHz, 1.0 V_{p-p} sine wave to each input pin. (2) In each select mode, compare signal output from the selected pin with leakage components from nonselected pins to find a crosstalk.
	$V_{in}V1$	CT10V2	—	55	60	—	dB	
	$V_{in}V2$	CT28V2	—	55	60	—	dB	
	$Y/V_{in}S1$	CT12V2	—	55	60	—	dB	
	$C_{in}S1$	CT14V2	—	55	60	—	dB	
	$Y/V_{in}S2$	CT16V2	—	55	60	—	dB	
	$C_{in}S2$	CT18V2	—	55	60	—	dB	
Y_{out} Input dynamic range	$V_{in}TV$	VDR7Y	—	1.5	2.0	—	V_{p-p}	(1) Apply a 15 kHz sine wave to each input pin. (2) In each select mode, measure an input amplitude at which the output waveform on pin 36 begins to be distorted.
	$V_{in}V1$	VDR10Y	—	1.5	2.0	—	V_{p-p}	
	$V_{in}V2$	VDR28Y	—	1.5	2.0	—	V_{p-p}	
	$Y/V_{in}S1$	VDR12Y	—	1.5	2.0	—	V_{p-p}	
	$Y/V_{in}S2$	VDR16Y	—	1.5	2.0	—	V_{p-p}	
	Y_{in}	VDR30Y	—	5.0	5.5	—	V_{p-p}	
Y_{out} Gain	$V_{in}TV$	G7Y	—	5.5	6.0	6.5	dB	(1) Apply a 15 kHz, 1.0 V_{p-p} sine wave to each input pin. (2) In each select mode, find the gain between input and output.
	$V_{in}V1$	G10Y	—	5.5	6.0	6.5	dB	
	$V_{in}V2$	G28Y	—	5.5	6.0	6.5	dB	
	$Y/V_{in}S1$	G12Y	—	5.5	6.0	6.5	dB	
	$Y/V_{in}S2$	G16Y	—	5.5	6.0	6.5	dB	
	Y_{in}	G30Y	—	−0.5	0	0.5	dB	

Characteristics	Select Mode	Symbol	Test Circuit	Min.	Typ.	Max.	Unit	Test Method
Y_{out} Frequency response	$V_{in}TV$	F7Y	—	10	—	—	MHz	(1) Apply a 1.0 V_{p-p} sine wave to each input pin. (2) In each select mode, measure a frequency at which the output amplitude on pin 36 is 3dB down from the 15 kHz applied level.
	$V_{in}V1$	F10Y	—	10	—	—	MHz	
	$V_{in}V2$	F28Y	—	10	—	—	MHz	
	$Y/V_{in}S1$	F12Y	—	10	—	—	MHz	
	$Y/V_{in}S2$	F16Y	—	10	—	—	MHz	
	Y_{in}	F30Y	—	10	—	—	MHz	
Y_{out} Crosstalk	$V_{in}TV$	CT7Y	—	55	60	—	dB	(1) Apply a 3.58 MHz, 1.0 V_{p-p} sine wave to each input pin. (2) In each select mode, compare signal output from the selected pin with leakage components from nonselected pins to find a crosstalk.
	$V_{in}V1$	CT10Y	—	55	60	—	dB	
	$V_{in}V2$	CT28Y	—	55	60	—	dB	
	$Y/V_{in}S1$	CT12Y	—	55	60	—	dB	
	$Y/V_{in}S2$	CT16Y	—	55	60	—	dB	
	Y_{in}	CT30Y	—	55	60	—	dB	
C_{out} Input dynamic range	$V_{in}TV$	VDR7C	—	1.5	2.0	—	V_{p-p}	(1) Apply a 15 kHz sine wave to each input pin. (2) In each select mode, measure an input amplitude at which the output waveform on pin 34 begins to be distorted.
	$V_{in}V1$	VDR10C	—	1.5	2.0	—	V_{p-p}	
	$V_{in}V2$	VDR28C	—	1.5	2.0	—	V_{p-p}	
	$Y/V_{in}S1$	VDR12C	—	1.5	2.0	—	V_{p-p}	
	$C_{in}S1$	VDR14C	—	1.5	2.0	—	V_{p-p}	
	$Y/V_{in}S2$	VDR16C	—	1.5	2.0	—	V_{p-p}	
	$C_{in}S2$	VDR18C	—	1.5	2.0	—	V_{p-p}	
	C_{in}	VDR32C	—	5.0	5.5	—	V_{p-p}	
C_{out} Gain	$V_{in}TV$	G7C	—	5.5	6.0	6.5	dB	(1) Apply a 15 kHz, 1.0 V_{p-p} sine wave to each input pin. (2) In each select mode, find the gain between input and output.
	$V_{in}V1$	G10C	—	5.5	6.0	6.5	dB	
	$V_{in}V2$	G28C	—	5.5	6.0	6.5	dB	
	$Y/V_{in}S1$	G12C	—	5.5	6.0	6.5	dB	
	$C_{in}S1$	G14C	—	5.5	6.0	6.5	dB	
	$Y/V_{in}S2$	G16C	—	5.5	6.0	6.5	dB	
	$C_{in}S2$	G18C	—	5.5	6.0	6.5	dB	
	C_{in}	G32C	—	−0.5	0	0.5	dB	

Characteristics	Select Mode	Symbol	Test Circuit	Min.	Typ.	Max.	Unit	Test Method
C_{out} Frequency response	V_{in}TV	F7C	—	10	—	—	MHz	(1) Apply a 1.0 V_{p-p} sine wave to each input pin. (2) In each select mode, measure a frequency at which the output amplitude on pin 34 is 3dB down from the 15 kHz applied level.
	V_{in}V1	F10C	—	10	—	—	MHz	
	V_{in}V2	F28C	—	10	—	—	MHz	
	Y/V_{in}S1	F12C	—	10	—	—	MHz	
	C_{in}S1	F14C	—	10	—	—	MHz	
	Y/V_{in}S2	F16C	—	10	—	—	MHz	
	C_{in}S2	F18C	—	10	—	—	MHz	
	C_{in}	F32C	—	10	—	—	MHz	
C_{out} Crosstalk	V_{in}TV	CT7C	—	55	60	—	dB	(1) Apply a 3.58 MHz, 1.0 V_{p-p} sine wave to each input pin. (2) In each select mode, compare signal output from the selected pin with leakage components from nonselected pins to find a crosstalk.
	V_{in}V1	CT10C	—	55	60	—	dB	
	V_{in}V2	CT28C	—	55	60	—	dB	
	Y/V_{in}S1	CT12C	—	55	60	—	dB	
	C_{in}S1	CT14C	—	55	60	—	dB	
	Y/V_{in}S2	CT16C	—	55	60	—	dB	
	C_{in}S2	CT18C	—	55	60	—	dB	
	C_{in}	CT32C	—	55	60	—	dB	
Det select Input dynamic range	V_{in}TV	VDR7D	—	5.0	5.5	—	V	(1) Apply a 15 kHz sine wave to each input pin. (2) In each select mode, measure an input amplitude at which the output waveform on pin 4 begins to be distorted.
	V_{in}V1	VDR10D	—	5.0	5.5	—	V	
	V_{in}V2	VDR28D	—	5.0	5.5	—	V	
	Y/V_{in}S1	VDR12D	—	5.0	5.5	—	V	
	V_{out1}	VDR38D	—	1.5	2.0	—	V	
	V_{out2}	VDR42D	—	1.5	2.0	—	V	
	Y_{out}	VDR36D	—	1.2	1.8	—	V	
	C_{out}	VDR34D	—	1.2	1.8	—	V	
Det select Gain	V_{in}TV	G7D	—	−0.5	0	0.5	dB	(1) Apply a 15 kHz, 1.0 V_{p-p} sine wave to each input pin. (2) In each select mode, find the gain between input and output.
	V_{in}V1	G10D	—	−0.5	0	0.5	dB	
	V_{in}V2	G28D	—	−0.5	0	0.5	dB	
	Y/V_{in}S1	G12D	—	−0.5	0	0.5	dB	
	V_{out1}	G38D	—	−0.1	0	0.1	dB	
	V_{out2}	G42D	—	−0.1	0	0.1	dB	
	Y_{out}	G36D	—	−0.1	0	0.1	dB	
	C_{out}	G34D	—	−0.1	0	0.1	dB	

Characteristics	Select Mode	Symbol	Test Circuit	Min.	Typ.	Max.	Unit	Test Method
$L_{out}1$ Input dynamic range	$L_{in}TV$	VDR5L1	—	6.0	6.5	—	V_{p-p}	(1) Apply a 1 kHz sine wave to each input pin. (2) In each select mode, measure an input amplitude at which the output waveform on pin 37 begins to be distorted.
	$L_{in}V1$	VDR8L1	—	6.0	6.5	—	V_{p-p}	
	$L_{in}V2$	VDR29L1	—	6.0	6.5	—	V_{p-p}	
	$L_{in}S1$	VDR11L1	—	6.0	6.5	—	V_{p-p}	
	$L_{in}S2$	VDR15L1	—	6.0	6.5	—	V_{p-p}	
$L_{out}1$ Gain	$L_{in}TV$	G5L1	—	−0.5	0	0.5	dB	(1) Apply a 1 kHz, 1.0 V_{p-p} sine wave to each input pin. (2) In each select mode, find the gain between input and output.
	$L_{in}V1$	G8L1	—	−0.5	0	0.5	dB	
	$L_{in}V2$	G29L1	—	−0.5	0	0.5	dB	
	$L_{in}S1$	G11L1	—	−0.5	0	0.5	dB	
	$L_{in}S2$	G15L1	—	−0.5	0	0.5	dB	
$L_{out}1$ Frequency response	$L_{in}TV$	F5L1	—	0.1	2.0	—	MHz	(1) Apply a 1.0 V_{p-p} sine wave to each input pin. (2) In each select mode, measure a frequency at which the output amplitude on pin 37 is 3dB down from the 1 kHz applied level.
	$L_{in}V1$	F8L1	—	0.1	2.0	—	MHz	
	$L_{in}V2$	F29L1	—	0.1	2.0	—	MHz	
	$L_{in}S1$	F11L1	—	0.1	2.0	—	MHz	
	$L_{in}S2$	F15L1	—	0.1	2.0	—	MHz	
$L_{out}1$ Crosstalk	$L_{in}TV$	CT5L1	—	70	100	—	dB	(1) Apply a 1 kHz, 1.0 V_{p-p} sine wave to each input pin. (2) In each select mode, compare signal output from the selected pin with leakage components from nonselected pins to find a crosstalk.
	$L_{in}V1$	CT8L1	—	70	100	—	dB	
	$L_{in}V2$	CT29L1	—	70	100	—	dB	
	$L_{in}S1$	CT11L1	—	70	100	—	dB	
	$L_{in}S2$	CT15L1	—	70	100	—	dB	
$L_{out}1$ Mute attenuation	$L_{in}TV$	M5L1	—	70	100	—	dB	(1) Apply a 1 kHz, 1.0 V_{p-p} sine wave to each input pin. (2) In each select mode, compare the output amplitudes on pin 37 when mute is turned on and turned off to find mute attenuation.
	$L_{in}V1$	M8L1	—	70	100	—	dB	
	$L_{in}V2$	M29L1	—	70	100	—	dB	
	$L_{in}S1$	M11L1	—	70	100	—	dB	
	$L_{in}S2$	M15L1	—	70	100	—	dB	

Characteristics	Select Mode	Symbol	Test Circuit	Min.	Typ.	Max.	Unit	Test Method
$R_{out}1$ Input dynamic range	$R_{in}TV$	VDR6R1	—	6.0	6.5	—	V_{p-p}	(1) Apply a 1 kHz sine wave to each input pin. (2) In each select mode, measure an input amplitude at which the output waveform on pin 35 begins to be distorted.
	$R_{in}V1$	VDR9R1	—	6.0	6.5	—	V_{p-p}	
	$R_{in}V2$	VDR31R1	—	6.0	6.5	—	V_{p-p}	
	$R_{in}S1$	VDR13R1	—	6.0	6.5	—	V_{p-p}	
	$R_{in}S2$	VDR17R1	—	6.0	6.5	—	V_{p-p}	
$R_{out}1$ Gain	$R_{in}TV$	G6R1	—	−0.5	0	0.5	dB	(1) Apply a 1 kHz, 1.0 V_{p-p} sine wave to each input pin. (2) In each select mode, find the gain between input and output.
	$R_{in}V1$	G9R1	—	−0.5	0	0.5	dB	
	$R_{in}V2$	G31R1	—	−0.5	0	0.5	dB	
	$R_{in}S1$	G13R1	—	−0.5	0	0.5	dB	
	$R_{in}S2$	G17R1	—	−0.5	0	0.5	dB	
$R_{out}1$ Frequency response	$R_{in}TV$	F6R1	—	0.1	2.0	—	MHz	(1) Apply a 1.0 V_{p-p} sine wave to each input pin. (2) In each select mode, measure a frequency at which the output amplitude on pin 35 is 3dB down from the 1 kHz applied level.
	$R_{in}V1$	F9R1	—	0.1	2.0	—	MHz	
	$R_{in}V2$	F31R1	—	0.1	2.0	—	MHz	
	$R_{in}S1$	F13R1	—	0.1	2.0	—	MHz	
	$R_{in}S2$	F17R1	—	0.1	2.0	—	MHz	
$R_{out}1$ Crosstalk	$R_{in}TV$	CT6R1	—	70	100	—	dB	(1) Apply a 1 kHz, 1.0 V_{p-p} sine wave to each input pin. (2) In each select mode, compare signal output from the selected pin with leakage components from nonselected pins to find a crosstalk.
	$R_{in}V1$	CT9R1	—	70	100	—	dB	
	$R_{in}V2$	CT31R1	—	70	100	—	dB	
	$R_{in}S1$	CT13R1	—	70	100	—	dB	
	$R_{in}S2$	CT17R1	—	70	100	—	dB	
$R_{out}1$ Mute attenuation	$R_{in}TV$	M6R1	—	70	100	—	dB	(1) Apply a 1 kHz, 1.0 V_{p-p} sine wave to each input pin. (2) In each select mode, compare the output amplitudes on pin 35 when mute is turned on and turned off to find mute attenuation.
	$R_{in}V1$	M9R1	—	70	100	—	dB	
	$R_{in}V2$	M31R1	—	70	100	—	dB	
	$R_{in}S1$	M13R1	—	70	100	—	dB	
	$R_{in}S2$	M17R1	—	70	100	—	dB	

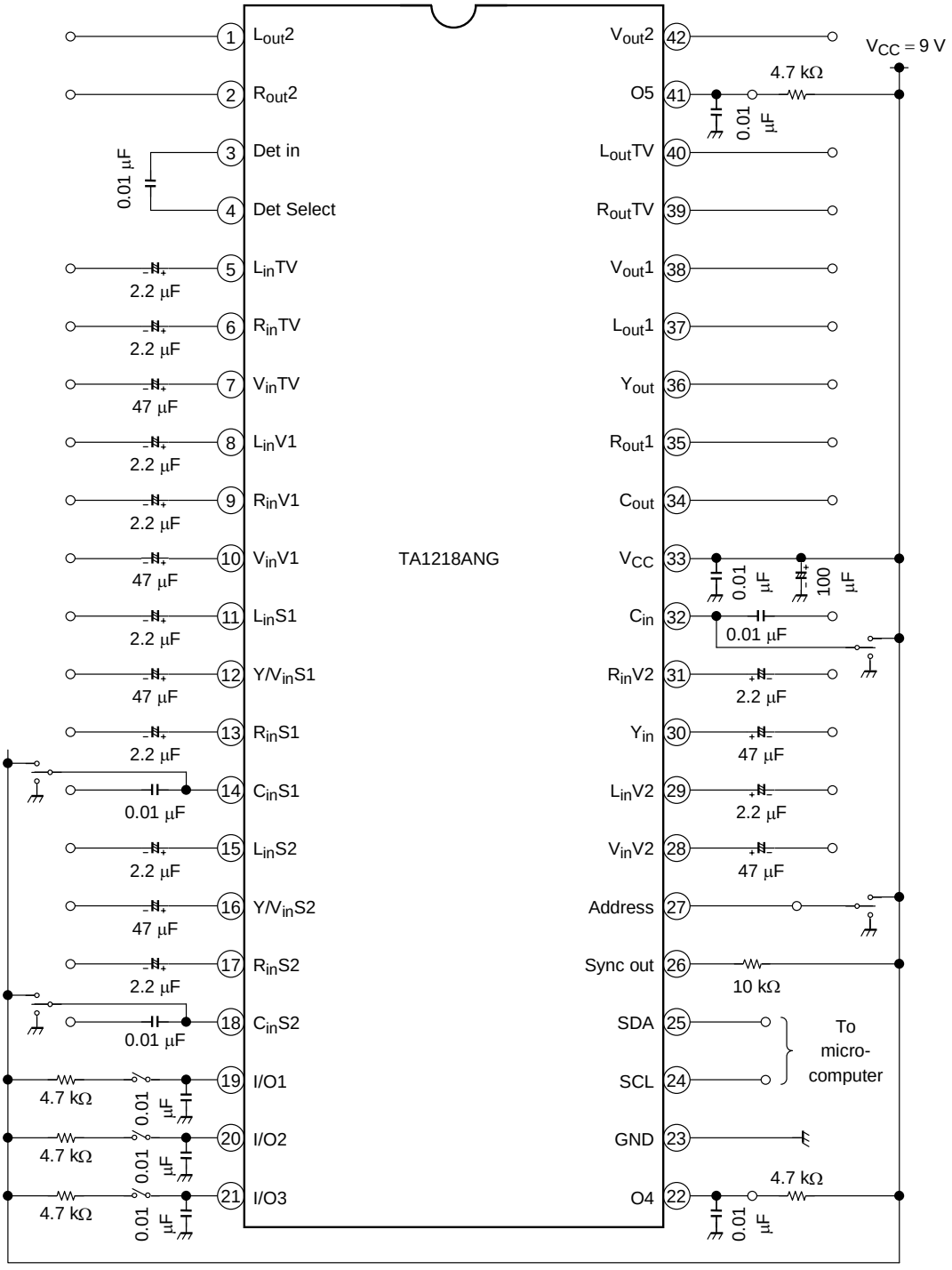
Characteristics	Select Mode	Symbol	Test Circuit	Min.	Typ.	Max.	Unit	Test Method
$L_{out}2$ Input dynamic range	$L_{in}TV$	VDR5L2	—	6.0	6.5	—	V_{p-p}	(1) Apply a 1 kHz sine wave to each input pin. (2) In each select mode, measure an input amplitude at which the output waveform on pin 1 begins to be distorted.
	$L_{in}V1$	VDR8L2	—	6.0	6.5	—	V_{p-p}	
	$L_{in}V2$	VDR29L2	—	6.0	6.5	—	V_{p-p}	
	$L_{in}S1$	VDR11L2	—	6.0	6.5	—	V_{p-p}	
	$L_{in}S2$	VDR15L2	—	6.0	6.5	—	V_{p-p}	
$L_{out}2$ Gain	$L_{in}TV$	G5L2	—	−0.5	0	0.5	dB	(1) Apply a 1 kHz, 1.0 V_{p-p} sine wave to each input pin. (2) In each select mode, find the gain between input and output.
	$L_{in}V1$	G8L2	—	−0.5	0	0.5	dB	
	$L_{in}V2$	G29L2	—	−0.5	0	0.5	dB	
	$L_{in}S1$	G11L2	—	−0.5	0	0.5	dB	
	$L_{in}S2$	G15L2	—	−0.5	0	0.5	dB	
$L_{out}2$ Frequency response	$L_{in}TV$	F5L2	—	0.1	2.0	—	MHz	(1) Apply a 1.0 V_{p-p} sine wave to each input pin. (2) In each select mode, measure a frequency at which the output amplitude on pin 1 is 3dB down from the 1 kHz applied level.
	$L_{in}V1$	F8L2	—	0.1	2.0	—	MHz	
	$L_{in}V2$	F29L2	—	0.1	2.0	—	MHz	
	$L_{in}S1$	F11L2	—	0.1	2.0	—	MHz	
	$L_{in}S2$	F15L2	—	0.1	2.0	—	MHz	
$L_{out}2$ Crosstalk	$L_{in}TV$	CT5L2	—	70	100	—	dB	(1) Apply a 1 kHz, 1.0 V_{p-p} sine wave to each input pin. (2) In each select mode, compare signal output from the selected pin with leakage components from nonselected pins to find a crosstalk.
	$L_{in}V1$	CT8L2	—	70	100	—	dB	
	$L_{in}V2$	CT29L2	—	70	100	—	dB	
	$L_{in}S1$	CT11L2	—	70	100	—	dB	
	$L_{in}S2$	CT15L2	—	70	100	—	dB	
$L_{out}2$ Mute attenuation	$L_{in}TV$	M5L2	—	70	100	—	dB	(1) Apply a 1 kHz, 1.0 V_{p-p} sine wave to each input pin. (2) In each select mode, compare the output amplitudes on pin 1 when mute is turned on and turned off to find mute attenuation.
	$L_{in}V1$	M8L2	—	70	100	—	dB	
	$L_{in}V2$	M29L2	—	70	100	—	dB	
	$L_{in}S1$	M11L2	—	70	100	—	dB	
	$L_{in}S2$	M15L2	—	70	100	—	dB	

Characteristics	Select Mode	Symbol	Test Circuit	Min.	Typ.	Max.	Unit	Test Method
$R_{out}2$ Input dynamic range	$R_{in}TV$	VDR6R2	—	6.0	6.5	—	V_{p-p}	(1) Apply a 1 kHz sine wave to each input pin. (2) In each select mode, measure an input amplitude at which the output waveform on pin 2 begins to be distorted.
	$R_{in}V1$	VDR9R2	—	6.0	6.5	—	V_{p-p}	
	$R_{in}V2$	VDR31R2	—	6.0	6.5	—	V_{p-p}	
	$R_{in}S1$	VDR13R2	—	6.0	6.5	—	V_{p-p}	
	$R_{in}S2$	VDR17R2	—	6.0	6.5	—	V_{p-p}	
$R_{out}2$ Gain	$R_{in}TV$	G6R2	—	−0.5	0	0.5	dB	(1) Apply a 1 kHz, 1.0 V_{p-p} sine wave to each input pin. (2) In each select mode, find the gain between input and output.
	$R_{in}V1$	G9R2	—	−0.5	0	0.5	dB	
	$R_{in}V2$	G31R2	—	−0.5	0	0.5	dB	
	$R_{in}S1$	G13R2	—	−0.5	0	0.5	dB	
	$R_{in}S2$	G17R2	—	−0.5	0	0.5	dB	
$R_{out}2$ Frequency response	$R_{in}TV$	F6R2	—	0.1	2.0	—	MHz	(1) Apply a 1.0 V_{p-p} sine wave to each input pin. (2) In each select mode, measure a frequency at which the output amplitude on pin 2 is 3dB down from the 1 kHz applied level.
	$R_{in}V1$	F9R2	—	0.1	2.0	—	MHz	
	$R_{in}V2$	F31R2	—	0.1	2.0	—	MHz	
	$R_{in}S1$	F13R2	—	0.1	2.0	—	MHz	
	$R_{in}S2$	F17R2	—	0.1	2.0	—	MHz	
$R_{out}2$ Crosstalk	$R_{in}TV$	CT6R2	—	70	100	—	dB	(1) Apply a 1 kHz, 1.0 V_{p-p} sine wave to each input pin. (2) In each select mode, compare signal output from the selected pin with leakage components from nonselected pins to find a crosstalk.
	$R_{in}V1$	CT9R2	—	70	100	—	dB	
	$R_{in}V2$	CT31R2	—	70	100	—	dB	
	$R_{in}S1$	CT13R2	—	70	100	—	dB	
	$R_{in}S2$	CT17R2	—	70	100	—	dB	
$R_{out}2$ Mute attenuation	$R_{in}TV$	M6R2	—	70	100	—	dB	(1) Apply a 1 kHz, 1.0 V_{p-p} sine wave to each input pin. (2) In each select mode, compare the output amplitudes on pin 2 when mute is turned on and turned off to find mute attenuation.
	$R_{in}V1$	M9R2	—	70	100	—	dB	
	$R_{in}V2$	M31R2	—	70	100	—	dB	
	$R_{in}S1$	M13R2	—	70	100	—	dB	
	$R_{in}S2$	M17R2	—	70	100	—	dB	
$L_{out}TV$ Input dynamic range	$L_{in}TV$	VDR5LTV	—	6.0	6.5	—	V_{p-p}	While applying a 1 kHz sine wave to pin 5 , measure an input amplitude at which the output waveform on pin 40 begins to be distorted.

Characteristics	Select Mode	Symbol	Test Circuit	Min.	Typ.	Max.	Unit	Test Method
$L_{out}TV$ Gain	$L_{in}TV$	G5LTV	—	−0.5	0	0.5	dB	While applying a 1 kHz, 1.0 V_{p-p} sine wave to pin 5 , find the gain between pins 5 and 40 .
$L_{out}TV$ Frequency response	$L_{in}TV$	F5LTV	—	0.1	2.0	—	MHz	While applying a 1.0 V_{p-p} sine wave to pin 5, measure a frequency at which the output waveform on pin 40 is 3dB down from the 1 kHz applied level.
$L_{out}TV$ Crosstalk	$L_{in}TV$	CT5LTV	—	70	100	—	dB	(1) Apply a 1 kHz, 1.0 V_{p-p} sine wave to each input pin. (2) Compare the output amplitude when $L_{in}TV$ is selected with leakage components from nonselected pins to find a crosstalk.
	$L_{in}V1$	CT8LTV	—	70	100	—	dB	
	$L_{in}V2$	CT29LTV	—	70	100	—	dB	
	$L_{in}S1$	CT11LTV	—	70	100	—	dB	
	$L_{in}S2$	CT15LTV	—	70	100	—	dB	
$L_{out}TV$ Mute attenuation	$L_{in}TV$	M5LTV	—	70	100	—	dB	While applying a 1 kHz, 1.0 V_{p-p} sine wave to pin 5, compare the output amplitudes on pin 40 when mute is turned on and turned off to find mute attenuation.
$R_{out}TV$ Input dynamic range	$R_{in}TV$	VDR6RTV	—	6.0	6.5	—	V_{p-p}	While applying a 1 kHz sine wave to pin 6 , measure an input amplitude at which the output waveform on pin 39 begins to be distorted.
$R_{out}TV$ Gain	$R_{in}TV$	G6RTV	—	−0.5	0	0.5	dB	While applying a 1 kHz, 1.0 V_{p-p} sine wave to pin 6 , find the gain between pins 6 and 39.
$R_{out}TV$ Frequency response	$R_{in}TV$	F6RTV	—	0.1	2.0	—	MHz	While applying a 1.0 V_{p-p} sine wave to pin 6, measure a frequency at which the output waveform on pin 39 is 3dB down from the 1 kHz applied level.

Characteristics	Select Mode	Symbol	Test Circuit	Min.	Typ.	Max.	Unit	Test Method
R_{out}TV Crosstalk	R_{in}TV	CT6RTV	—	70	100	—	dB	(1) Apply a 1 kHz, 1.0 V_{p-p} sine wave to each input pin. (2) Compare the output amplitude when R_{in}TV is selected with leakage components from nonselected pins
	R_{in}V1	CT9RTV	—	70	100	—	dB	
	R_{in}V2	CT31RTV	—	70	100	—	dB	
	R_{in}S1	CT13RTV	—	70	100	—	dB	
	R_{in}S2	CT17RTV	—	70	100	—	dB	
R_{out}TV Mute attenuation	R_{in}TV	M6RTV	—	70	100	—	dB	While applying a 1 kHz, 1.0 V_{p-p} sine wave to pin 6, compare the output amplitudes on pin 39 when mute is turned on and turned off to find mute attenuation.

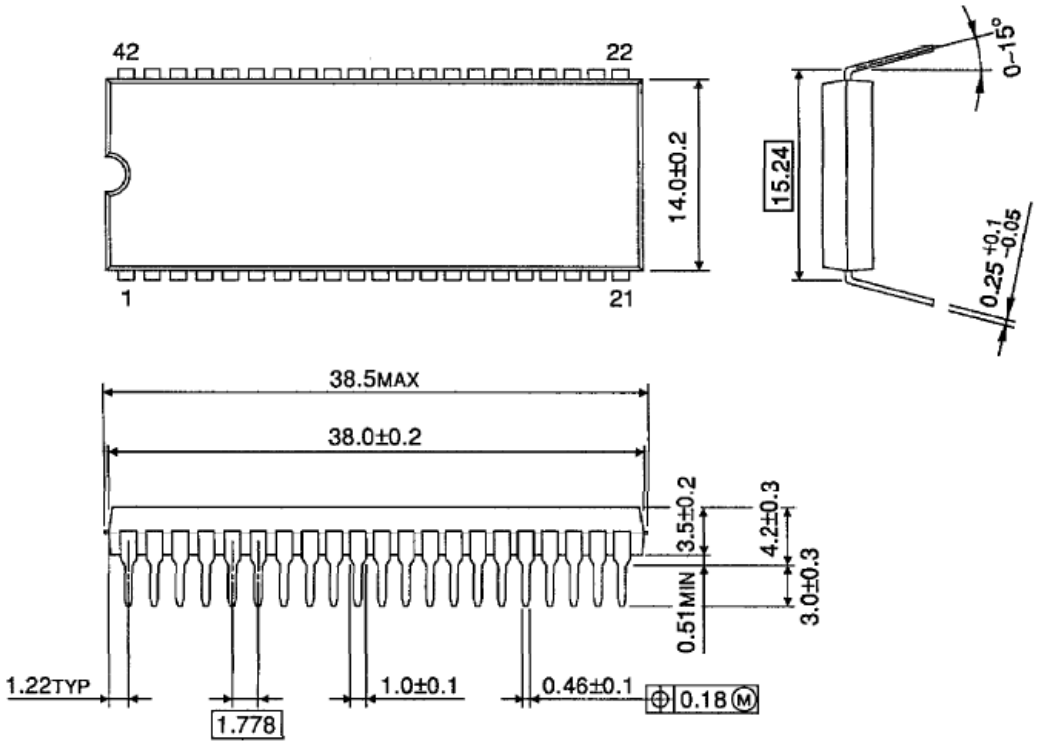
Application Circuit



Package Dimensions

OUTLINE DRAWING
SDIP42-P-600-1.78

Unit : mm



Weight: 4.13 g (typ.)

About solderability, following conditions were confirmed

- Solderability

  (1) Use of Sn-63Pb solder Bath
  - solder bath temperature = 230°C
  - dipping time = 5 seconds
  - the number of times = once
  - use of R-type flux

  (2) Use of Sn-3.0Ag-0.5Cu solder Bath
  - solder bath temperature = 245°C
  - dipping time = 5 seconds
  - the number of times = once
  - use of R-type flux

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