SMCT TA65N14A10

Advanced Pulse Power Device

N-MOS VCS, ThinPak^{TM}

Description

This voltage controlled Solidtron (VCS) discharge switch utilizes an n-type MOS-Controlled Thyristor mounted on a ThinPakTM, ceramic "chip-scale" hybrid.

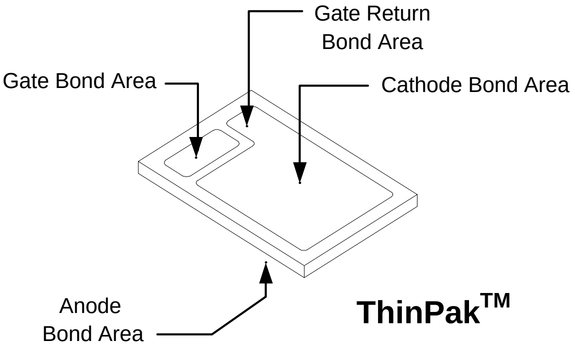
The VCS features the high peak current capability and low On-state voltage drop common to SCR thyristors combined with extremely high dI/dt capability. This semiconductor is intended for the control of high power circuits with the use of very small amounts of input energy and is ideally suited for capacitor discharge applications.

The ThinPak^{TM} Package is a perforated, metalized ceramic substrate attached to the silicon using 302°C solder. An epoxy underfill is applied to protect the high voltage termination from debris. All exterior metal surfaces are tinned with 63pb/37sn solder providing the user with a circuit ready part. It's small size and low profile make it extremely attractive to high dI/dt applications where stray series inductance must be kept to a minimum.

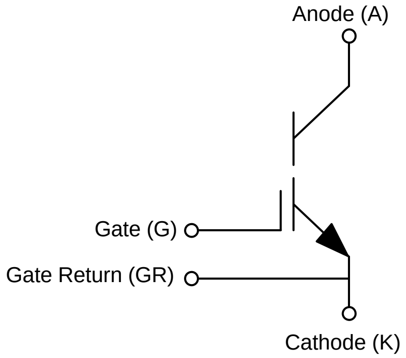
Features

- 1400V Peak Off-State Voltage
- 65A Continuous Rating
- 6kA Surge Current Capability
- >100kA/uSec dI/dt Capability
- <150nSec Turn-On Delay
- Low On-State Voltage
- MOS Gated Control
- Low Inductance Package

Package



Schematic Symbol



Absolute Maximum Ratings

	SYMBOL	VALUE	UNITS
Peak Off-State Voltage	V_{DRM}	1400	V
Peak Reverse Voltage	V_{RRM}	-5	V
Off-State Rate of Change of Voltage Immunity	dv/dt	5000	V/uSec
Continuous Anode Current at 110°C	I_{A110}	65	A
Repetitive Peak Anode Current (Pulse Width=1uSec)	I_{ASM}	6000	A
Rate of Change of Current	dI/dt	125	kA/uSec
Continuous Gate-Cathode Voltage	V_{GKS}	+/-20	V
Peak Gate-Cathode Voltage	V_{GKM}	+/-25	V
Minimum Negative Gate-Cathode Voltage Required for Garanteed Off-State	$V_{GK(OFF-MIN)}$	-5	V
Maximum Junction Temperature	T_{JM}	150	°C
Maximum Soldering Temperature (Installation)		260	°C

This **SILICON POWER** product is protected by one or more of the following U.S. Patents:

5,521,436
5,585,310
5,248,901
5,366,932
5,497,013
5,532,635
5,446,316
5,557,656
5,564,226
5,517,058
4,814,283
5,135,890
5,105,536
5,777,346
5,446,316
5,577,656
5,473,193
5,166,773
5,209,390
5,139,972
5,103,290
5,028,987
5,304,847
5,569,957
4,958,211
5,111,268
5,260,590
5,350,935
5,640,300
5,184,206
5,206,186
5,757,036
5,777,346
5,995,349
4,801,985
4,476,671
4,857,983
4,888,627
4,912,541
5,424,563
5,399,892
5,468,668
5,082,795
4,980,741
4,941,026
4,927,772
4,739,387
4,648,174
4,644,637
4,374,389
4,750,666
4,429,011
5,293,070

Performance Characteristics T_J=25°C unless otherwise specified

Parameters	Symbol	Test Conditions		Min.	Typ.	Max.	Units
				Measurements			
Anode to Cathode Breakdown Voltage	$V_{(BR)}$	V_{GK}=-5, I_A=1mA		1400			V
Anode-Cathode Off-State Current	i_D	V_{GE}=-5V, V_{AK}=1200V	T_C=25°C		<10	100	uA
			T_C=150°C		250	1000	uA
Gate-Cathode Turn-On Threshold Voltage	$V_{GK(TH)}$	$V_{AK}=V_{GK}$, I_{AK}=1mA			0.7		V
Gate-Cathode Leakage Current	$I_{GK(lkg)}$	V_{GK}=+/-20V				750	nA
Anode-Cathode On-State Voltage	V_T	I_T=65A, V_{GK}=+5V	T_C=25°C		1.3	1.8	V
		(See Figures 1,2 & 3)	T_C=150°C		1.1	1.4	V
Input Capacitance	C_{ISS}				18		nF
Turn-on Delay Time	$t_{D(ON)}$	0.2uF Capacitor Discharge			82	150	nS
Rate of Change of Current	dI/dt	T_J=25°C, V_{GK}= -5V to +5V			58		kA/uSec
Peak Anode Current	I_P	V_{AK}=800V, RG=4.7Ω			3300		A
Discharge Event Energy	E_{DIS}	L_S= 8nH (See Figures 4,5 & 6)			36		mJ
Turn-on Delay Time	$t_{D(ON)}$	0.2uF Capacitor Discharge			64	120	nS
Rate of Change of Current	dI/dt	T_J=150°C, V_{GK}= -5V to +5V			100		kA/uSec
Peak Anode Current	I_P	V_{AK}=1200V, RG=4.7Ω			5200		A
Discharge Event Energy	E_{DIS}	L_S= 8nH (See Figures 4,5 & 6)			74		mJ
Junction to Case Thermal Resistance	$R_{\theta JC}$	Anode (bottom) side cooled (Note 1.)			0.035		°C/W
Junction to Case Thermal Resistance	$R_{\theta JC}$	Cathode-Gate (top) side cooled (Note 2.)			0.6		°C/W

Notes:

1. Case Exterior Assumed to be 0.002" of 63sn/37pb solder applied directly to Anode. (See Figure 7.)
2. Case Exterior Assummed to be 0.002" of 63sn/37pb solder applied directly to cathode bond area of thinPak. (See Figure 7.)

Typical Performance Curves (unless otherwise specified)

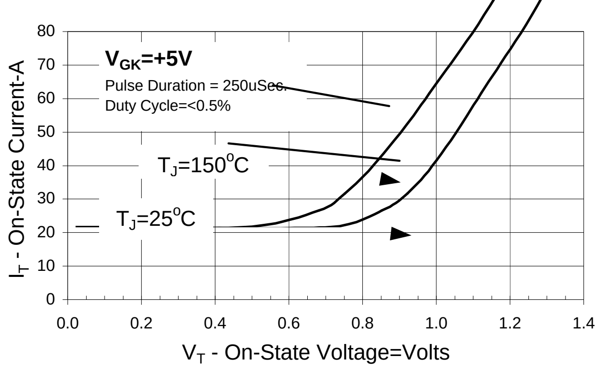


Figure 1. On-State Characteristics

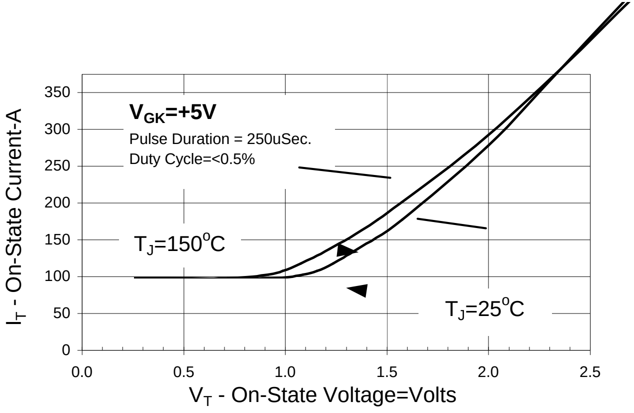


Figure 2. On-State Characteristics

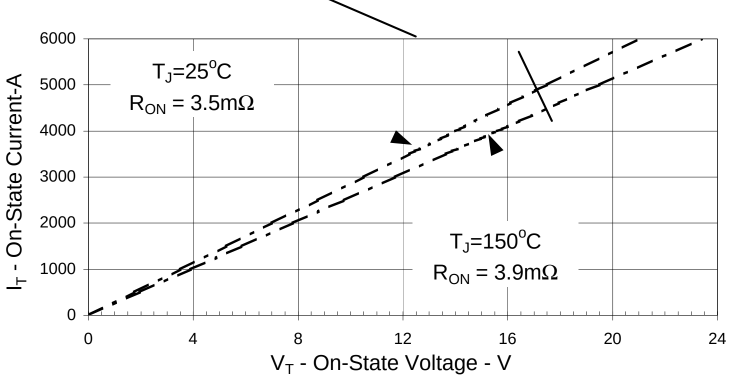


Figure 3. Predicted High Current On-State Characteristics

Typical Performance Curves (Continued)

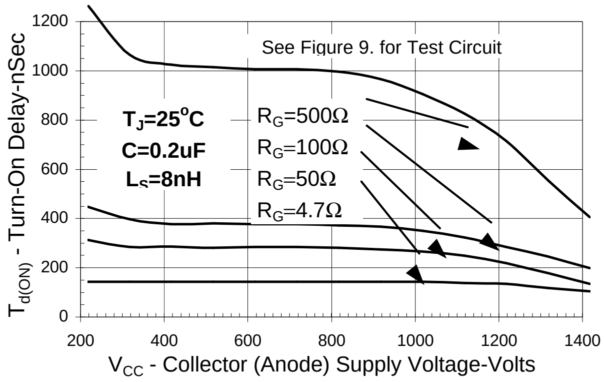


Figure 4. Turn-On Delay Characteristics

R_G=4.7Ω - 500Ω, T_J=25°C

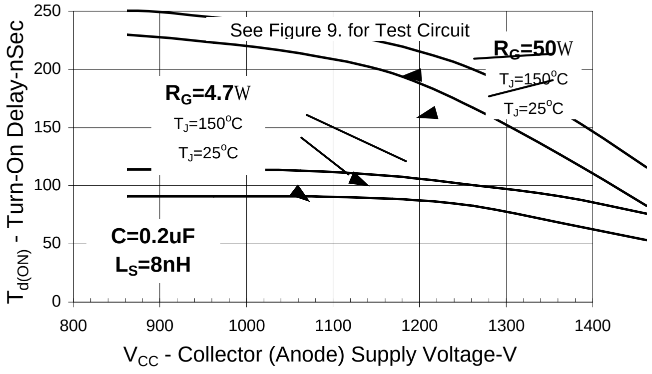


Figure 5. Turn-On Delay Characteristics

R_G=4.7Ω & 50Ω, T_J=25°C & 150°C

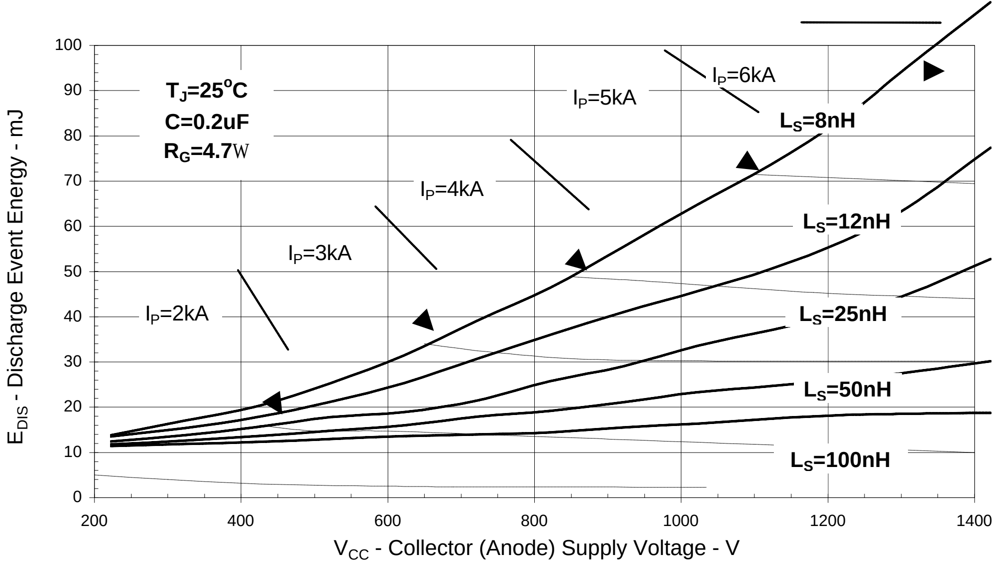


Figure 6. 0.2uF Discharge Pulse Performance Characteristics (See Figure 9.)

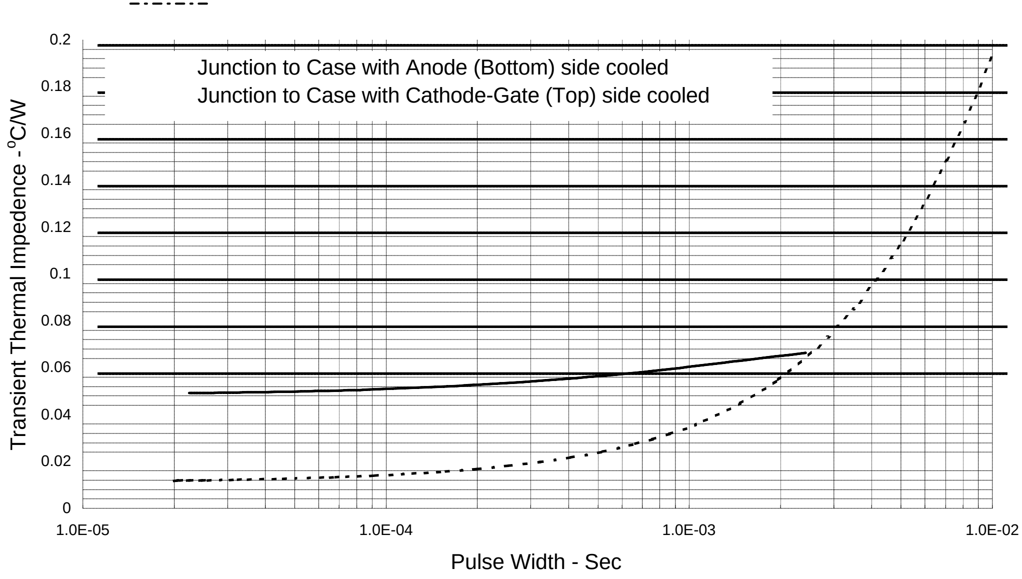


Figure 7. Transient Thermal Impeadance Response

Typical Performance Curves (Continued)

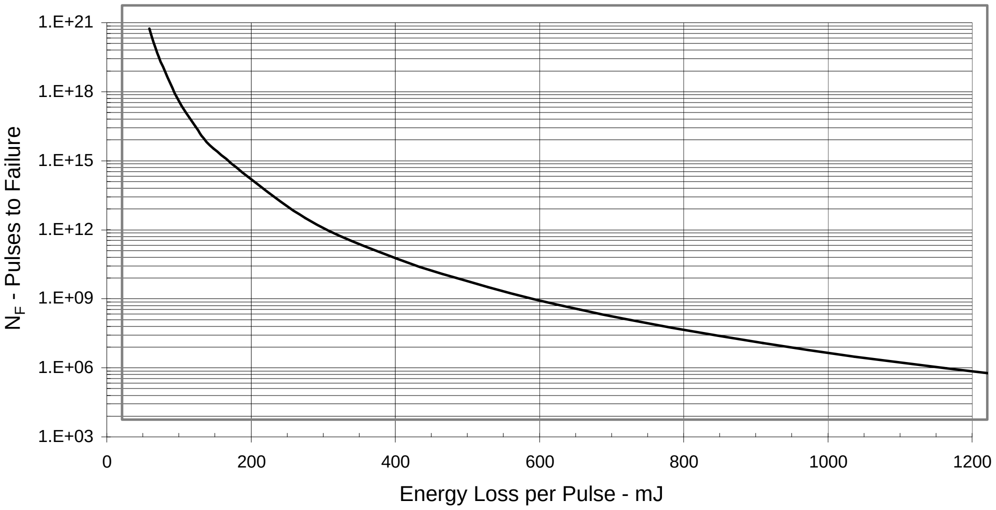
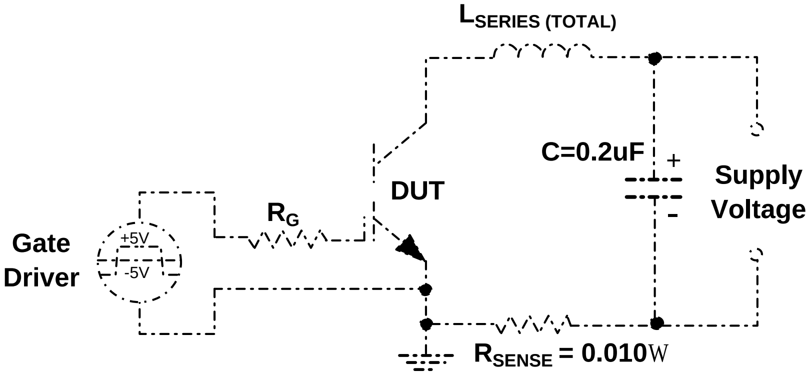


Figure 8. Pulses to Failure (Pulse Widths < 100uSec)

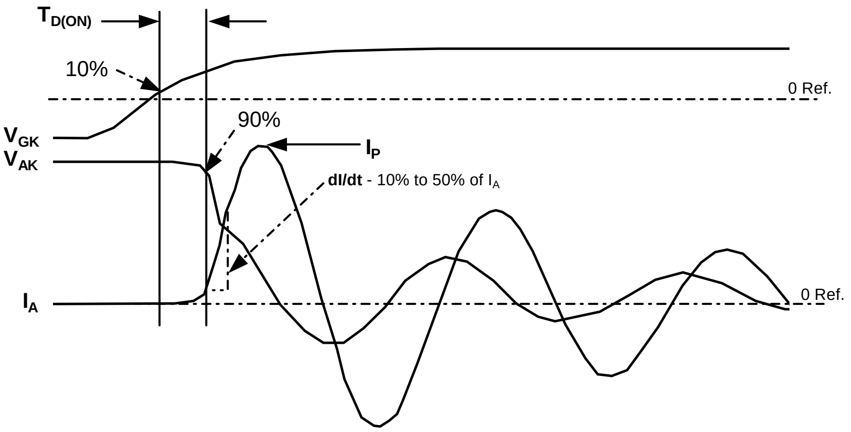
Test Circuit and Waveforms



- $L_{SERIES(TOTAL)}$ is caculated using
  $1 / (f\ 2\pi)^2C$
  where f = frequency of I_A (See Figure 10)

- R_{SENSE} is a calibrated Current Viewing Resistor (CVR)

Figure 9. 0.2uF Pulsed Discharge Circuit Schematic



- The waveform shown is representative of one produced using a very low inductance circuit (<10nH).

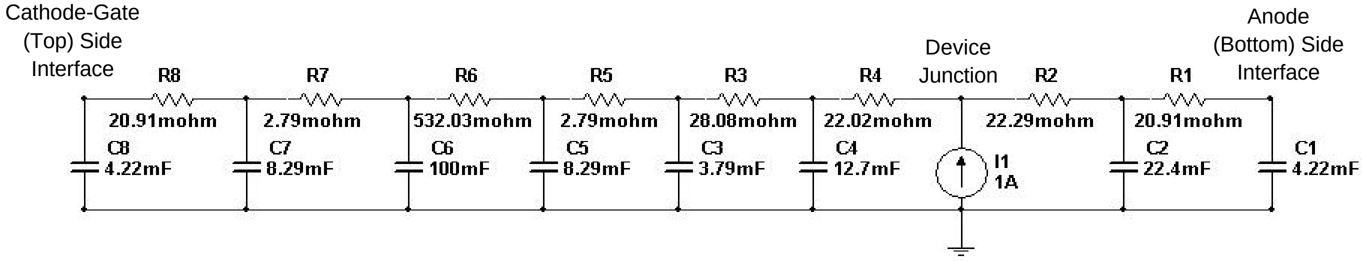
- V_{GK} is held positive until I_A oscillations have ended (I_A=0).

Figure 10. 0.2uF Pulsed Discharge Circuit Waveforms

Application Notes

A1. Junction Temperature Calculation

The figure below shows a lump model of the thermal properties of the size 6 thinPak packaged VCS, from the 2-mil solder on the top of the lid on the left to the 2-mil solder on the bottom of the device on the right. By adding the user's lump model of the rest of the thermal system the user can calculate the junction and case temperature rise under any operating condition.



A2. Calculation of Pulses to Failure for Intermediate/Long Pulse Widths

The user may calculate the Number of Pulses to failure (N_F) for long to intermedeiate pulse widths (not covered in the typical performance curve section) by applying the junction temperature rise (dT), calculated as described in A1, to the formula N_F=(300/dT)9 .

A3. Use of Gate Return Bond Area.

The MCT was designed for high di/dt applications. An independent cathode connection or "Gate Return Bond Area" was provided to minimize the effects of rapidly changing Anode-Cathode current on the Gate control voltage, (V=L*di/dt). It is therefore, critcal that the user utilize the Gate Return Bond Area as the point at which the gate driver reference (return) is attached to the VCS device.

Packaging and Handling

1. All metal surfaces are tinned using 63pb/37sn solder.
2. Installation reflow temperature should not exceed 260°C or internal package degradation may result.
3. Package may be cooled from either top or bottom (See Figures 7 & A1 Application Notes.)
4. As with all MOS gated devices, proper handling procedures must be observed to prevent electrostatic discharge which may result in permanant damage to the gate of the device

Package Dimensions