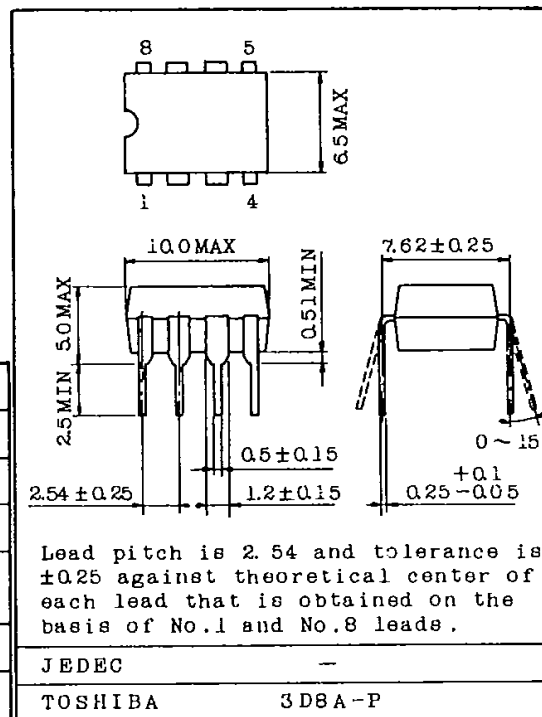


SINGLE OPERATIONAL AMPLIFIER  
OPERATIONAL AMPLIFIER  
DC AMPLIFIER

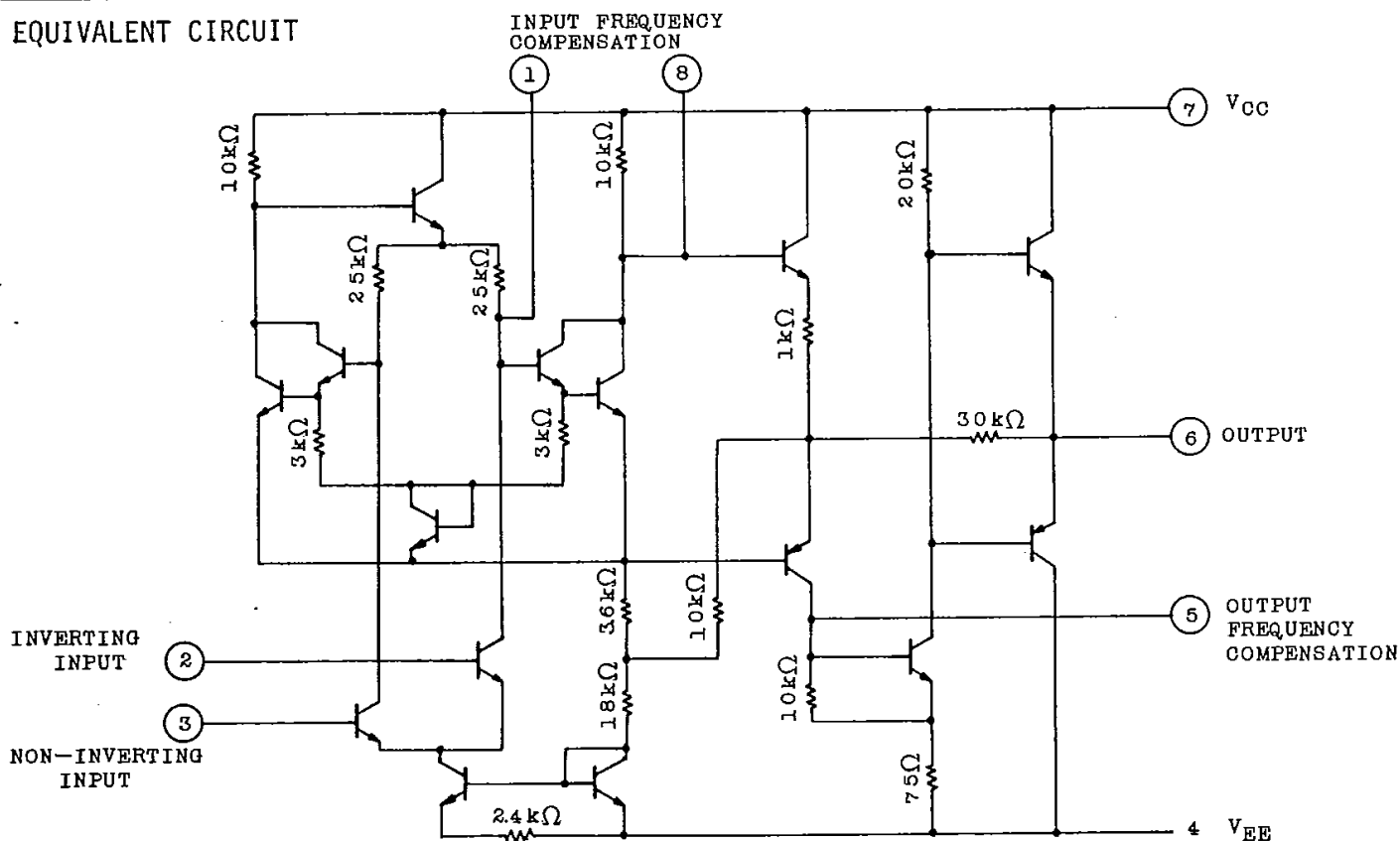
- High Gain
- Low Input Offset Voltage :  $V_{IO}=0.5mV$  (Typ.)

MAXIMUM RATINGS ( $T_a=25^{\circ}C$ )

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	$V_{CC}, V_{EE}$	$\pm 18$	V
Power Dissipation	$P_D$	300	mW
Differential Input Voltage	$DV_{IN}$	6	V
Input Voltage ( $V_{CC}, V_{EE}=\pm 15V$ )	$V_{IN}$	+10 -15	V
Output Short Circuit Current	$I_{OS}$	$\pm 20$	mA
Operating Temperature	$T_{opr}$	-30 ~ 75	$^{\circ}C$
Storage Temperature	$T_{stg}$	-55 ~ 125	$^{\circ}C$



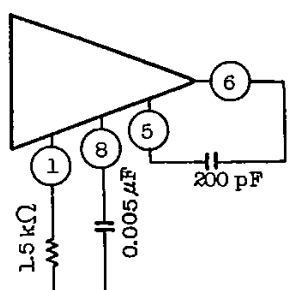
EQUIVALENT CIRCUIT



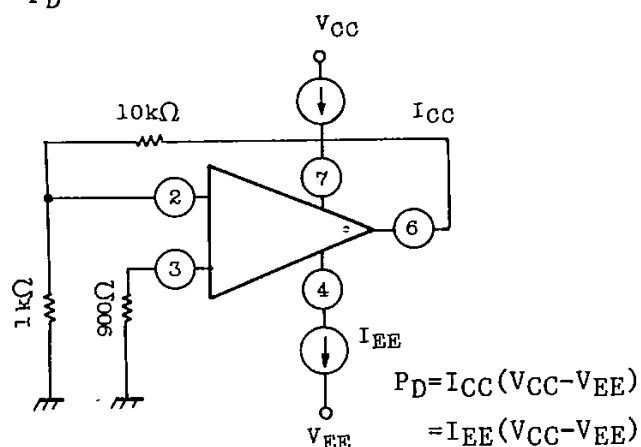
ELECTRICAL CHARACTERISTICS ( $V_{CC}=15V$ ,  $V_{EE}=-15V$ ,  $T_a=25^{\circ}C$ )

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	$V_{IO}$	2	$R_g \leq 10k\Omega$	-	-	5	mV
Input Offset Current	$I_{IO}$	3	-	-	50	150	nA
Input Bias Current	$I_I$	3	-	-	200	500	nA
Input Impedance	$Z_{IN}$	-	$f=1kHz$	150	380	-	$k\Omega$
Output Impedance	$Z_o$	-	$f=1kHz$	-	150	-	$\Omega$
Voltage Gain	$G_V$	5	$R_L \geq 2k\Omega$ , $f=1kHz$ $V_{OUT}=\pm 10V$	20	45	-	$\times 10^3$
Maximum Output Voltage	$V_{OM}$	4	$R_L \geq 10k\Omega$	$\pm 12$	$\pm 14$	-	V
	$V_{OMR}$		$R_L \geq 2k\Omega$	$\pm 10$	$\pm 13$	-	
Maximum Output Voltage Swing	$V_{Op-p}$	5	$R_L = 10k\Omega$ , $f=1kHz$	24	28	-	V
Common Mode Input Voltage	$CMV_{IN}$	6	-	+9 -12	+10 -13	-	V
Common Mode Input Signal Rejection Ratio	CMRR	6	$f=1kHz$	70	90	-	dB
Supply Voltage Rejection Ratio	SVRR	2	$R_g=10k\Omega$	-	25	100	$\mu V/V$
Power Dissipation	$P_D$	1	-	-	80	150	mW
Input Noise Voltage	$e_{np-p}$	7	$R_g=10k\Omega$ , $f=0 \sim 100Hz$	-	-	20	$\mu V$
Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	2	$R_g \leq 100\Omega$ , $T_a=-30 \sim 75^{\circ}C$	-	-	20	$\mu V/^{\circ}C$

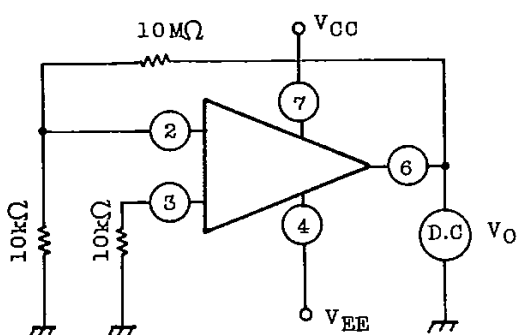
TEST CIRCUIT



(1)  $P_D$



(2)  $V_{IO}$ , SVRR



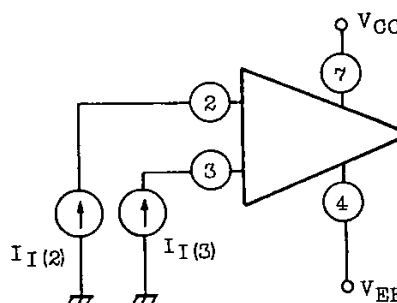
$$V_{IO} = V_{OUT} / 1000$$

$$SVRR = (V_{OUT1} - V_{OUT2}) / 5000$$

$$V_{OUT1}: V_{CC} = V_{EE} = 17.5V$$

$$V_{OUT2}: V_{CC} = V_{EE} = 12.5V$$

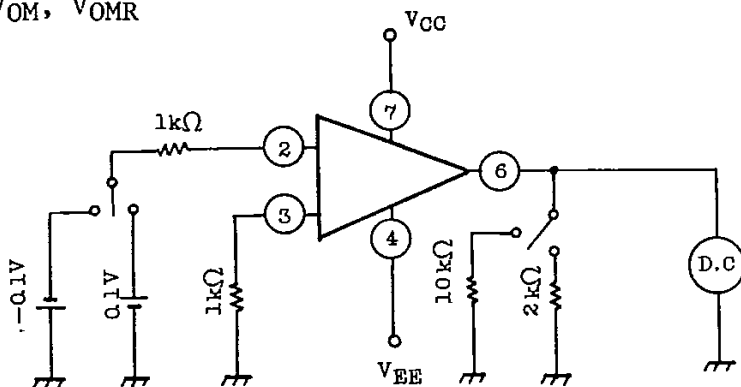
(3)  $I_I$ ,  $I_{IO}$



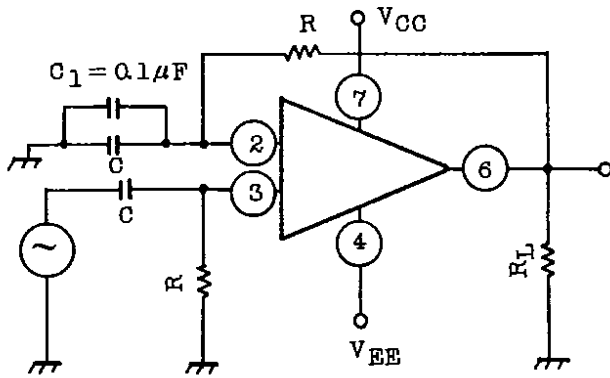
$$I_I = \frac{I_{I(-)} + I_{I(+)}}{2}$$

$$I_{IO} = |I_{I(-)} - I_{I(+)}|$$

(4)  $V_{OM}$ ,  $V_{OMR}$

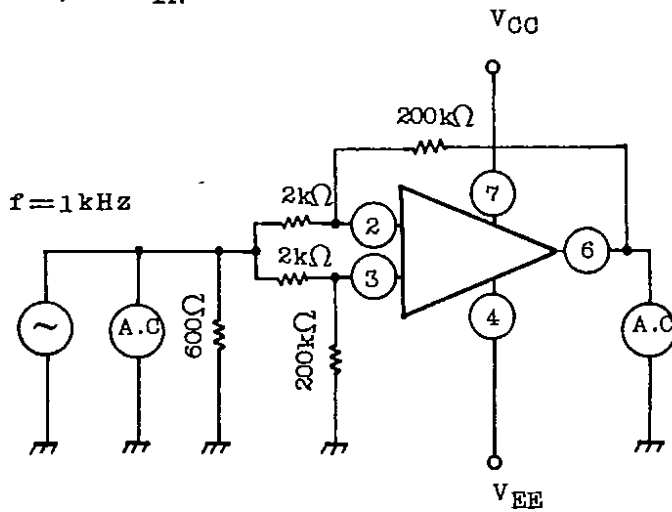


(5)  $G_V$ ,  $V_{Op-p}$



C : DC COUPLE  
 C<sub>1</sub> : HF BYPASS  
 $\omega \gg 1/RC$   
 $G_V = V_{OUT}/V_{IN}$

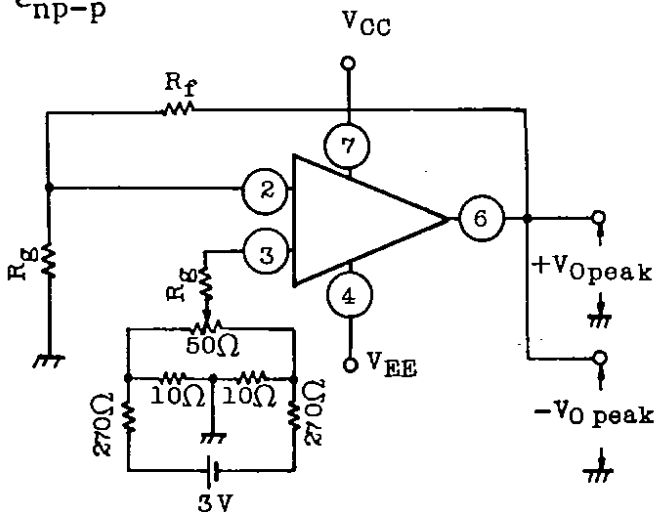
(6) CMRR,  $CMV_{IN}$



$$CMRR = 20 \log \frac{70.7}{V_{OUT}} \text{ (dB)}$$

$$V_{IN} = 0.707 (V_{rms})$$

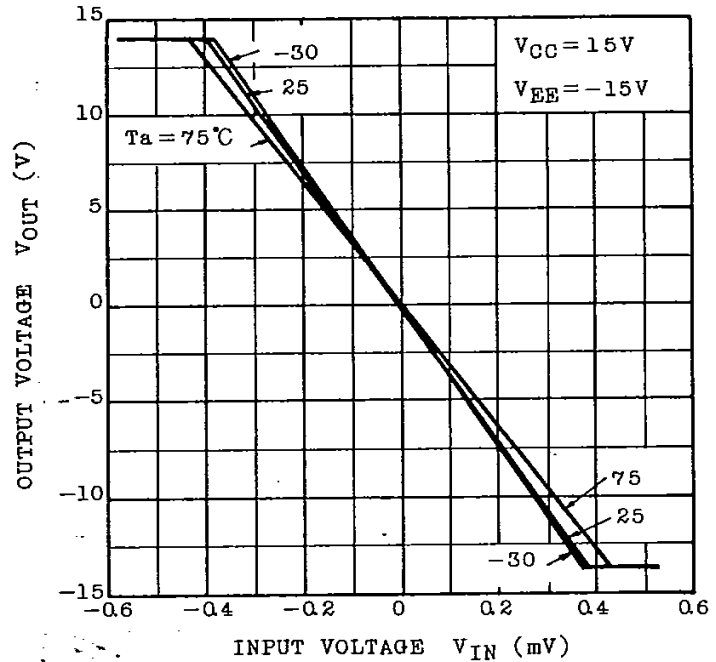
(7)  $e_{np-p}$



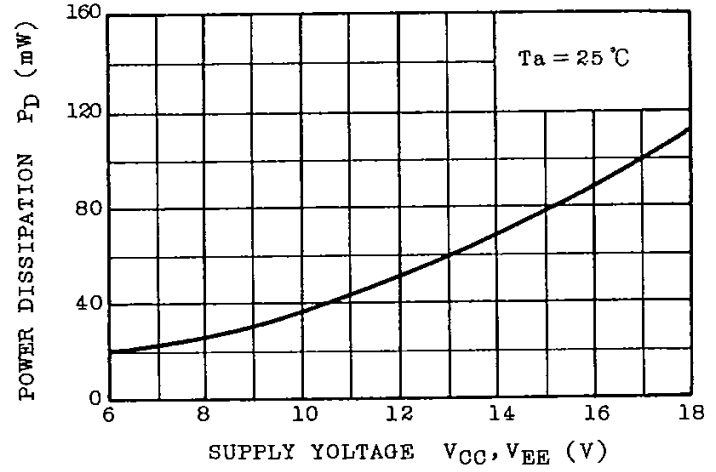
AFTER ADJUSTING BY  $V_R$ ,  
 BEING TESTED  $+V_{Opeak}$ ,  $-V_{Opeak}$   
 $e_{np-p}$

$$= \frac{R_g}{R_f} (|+V_{Opeak}| + |-V_{Opeak}|)$$

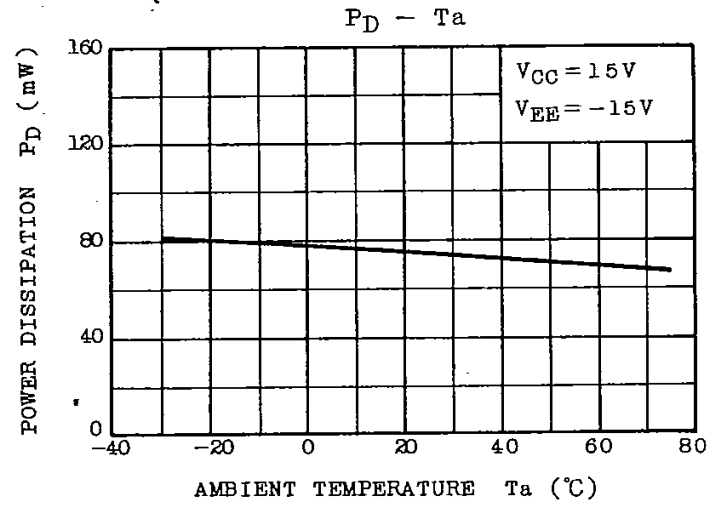
$V_{OUT} - V_{IN}$



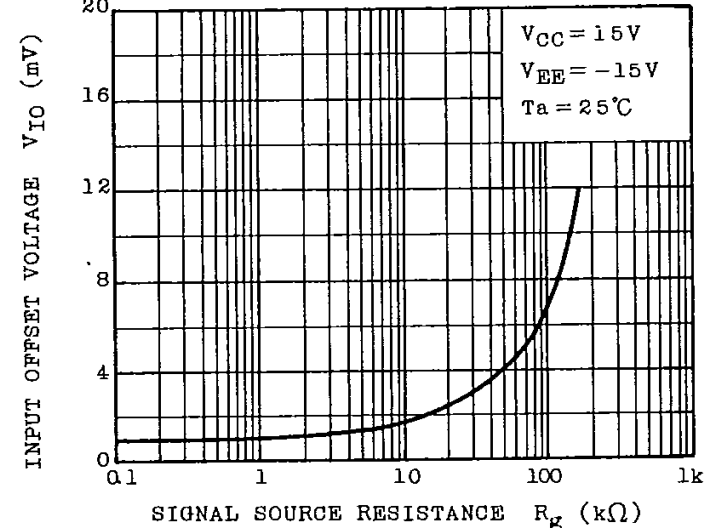
$P_D - V_{CC}, V_{EE}$



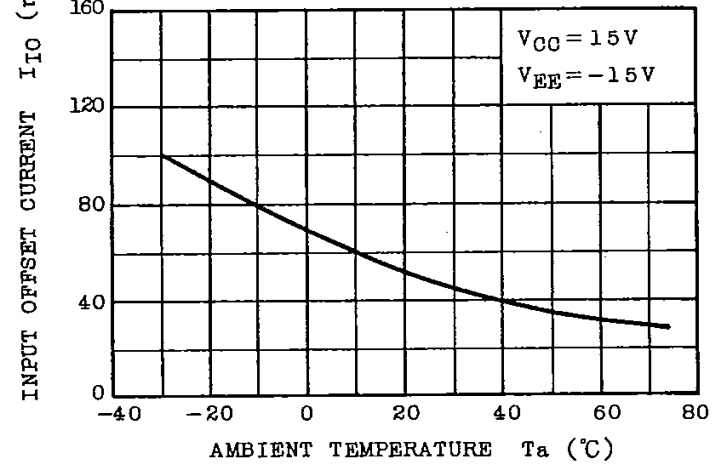
$P_D - T_a$



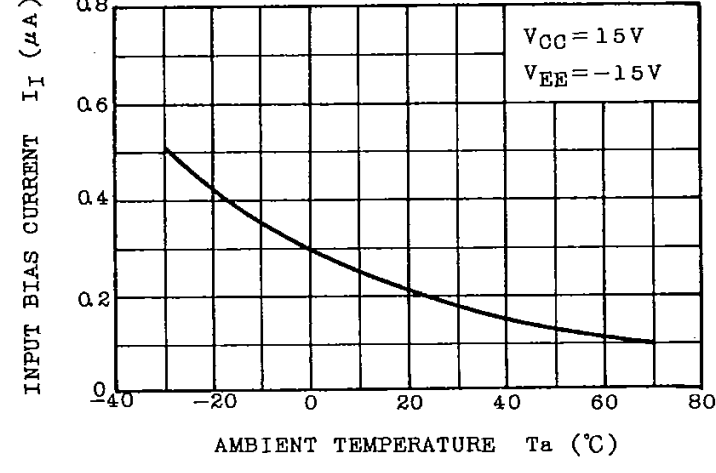
$V_{IO} - R_g$

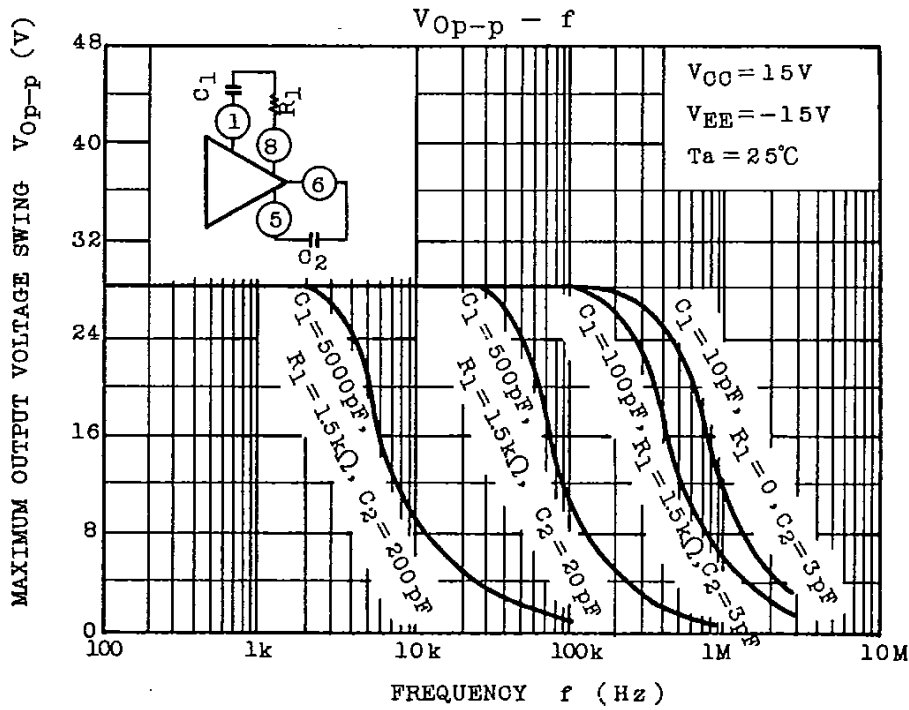
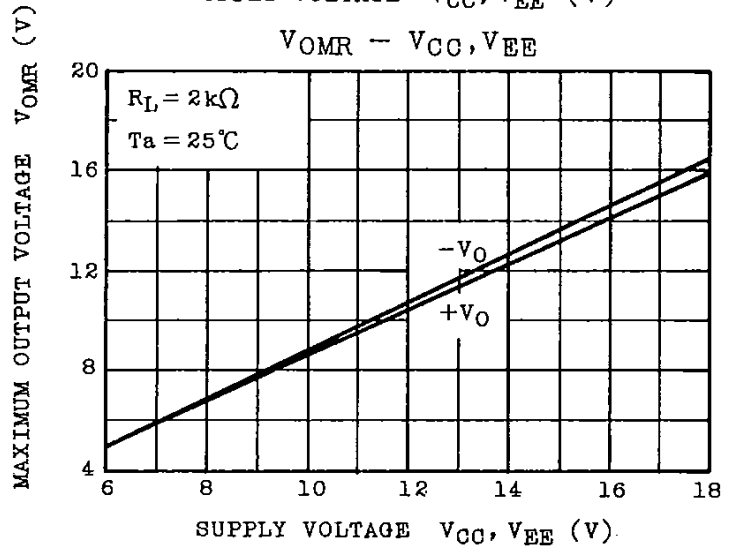
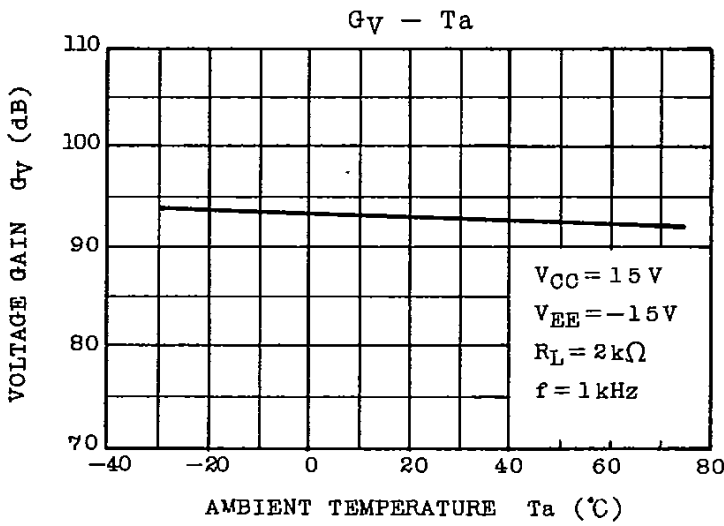
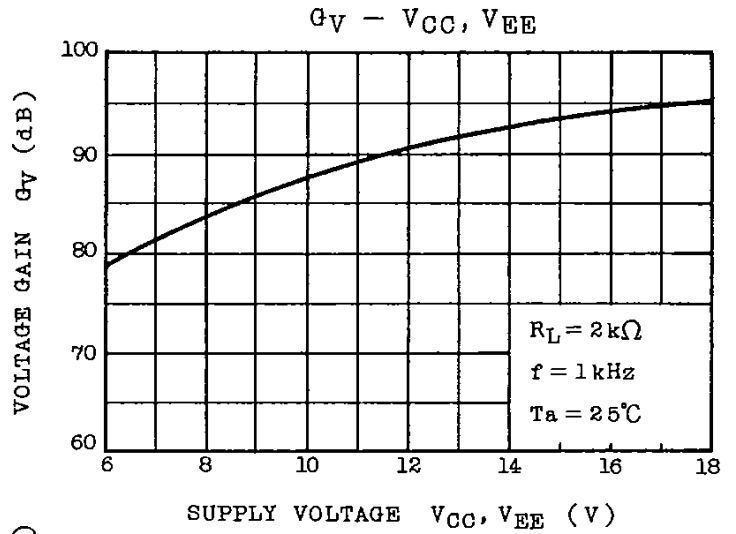
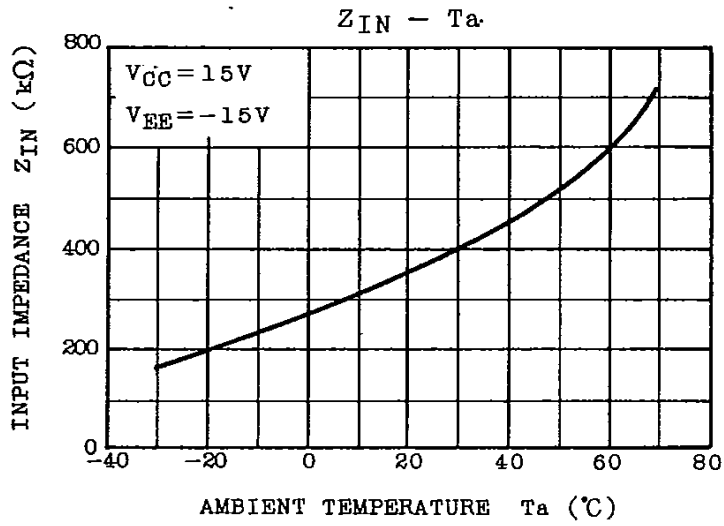


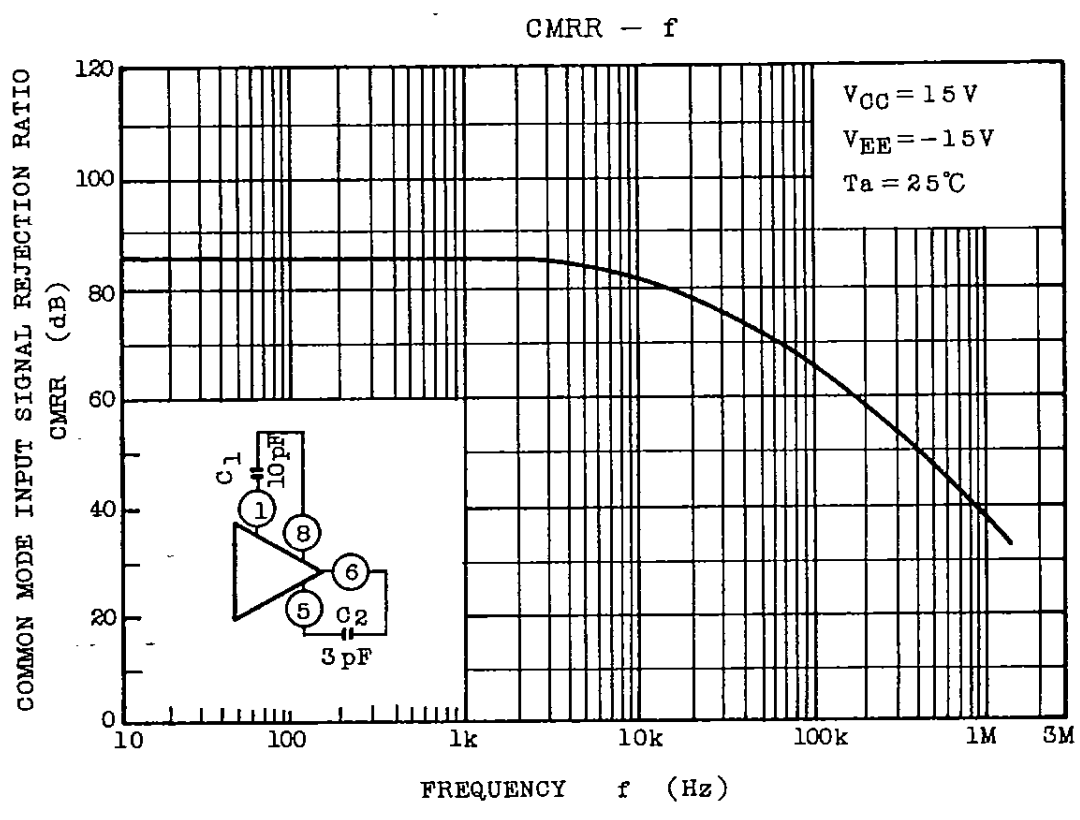
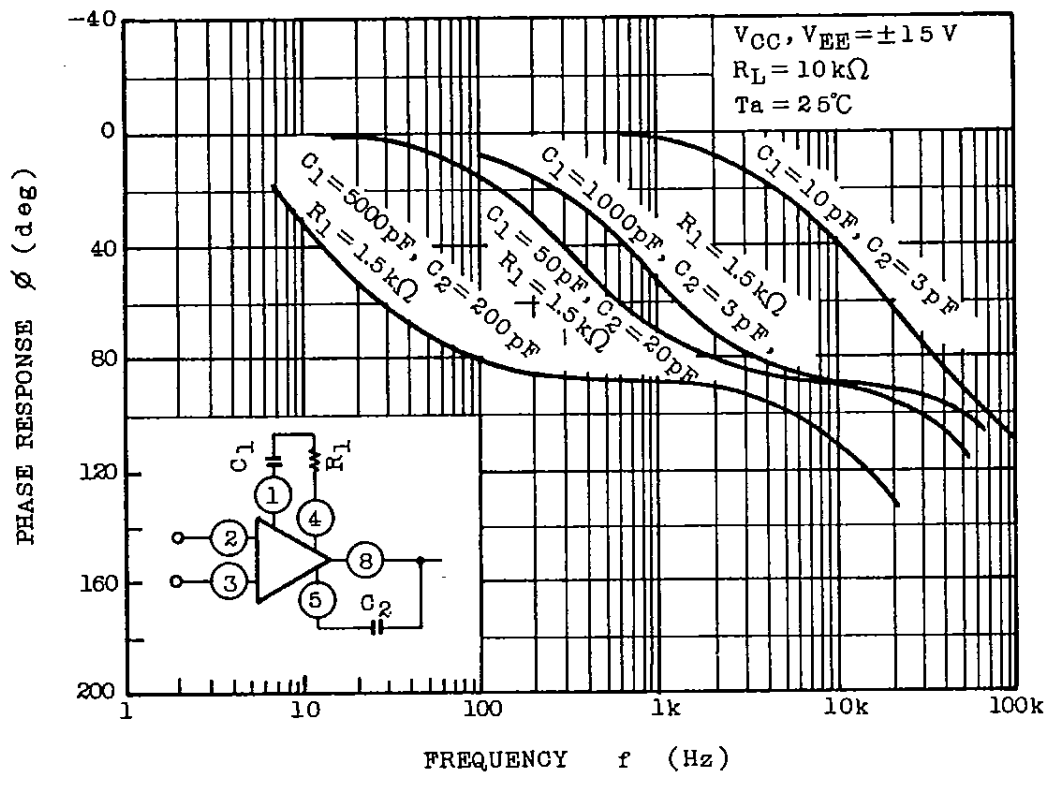
$I_{IO} - T_a$

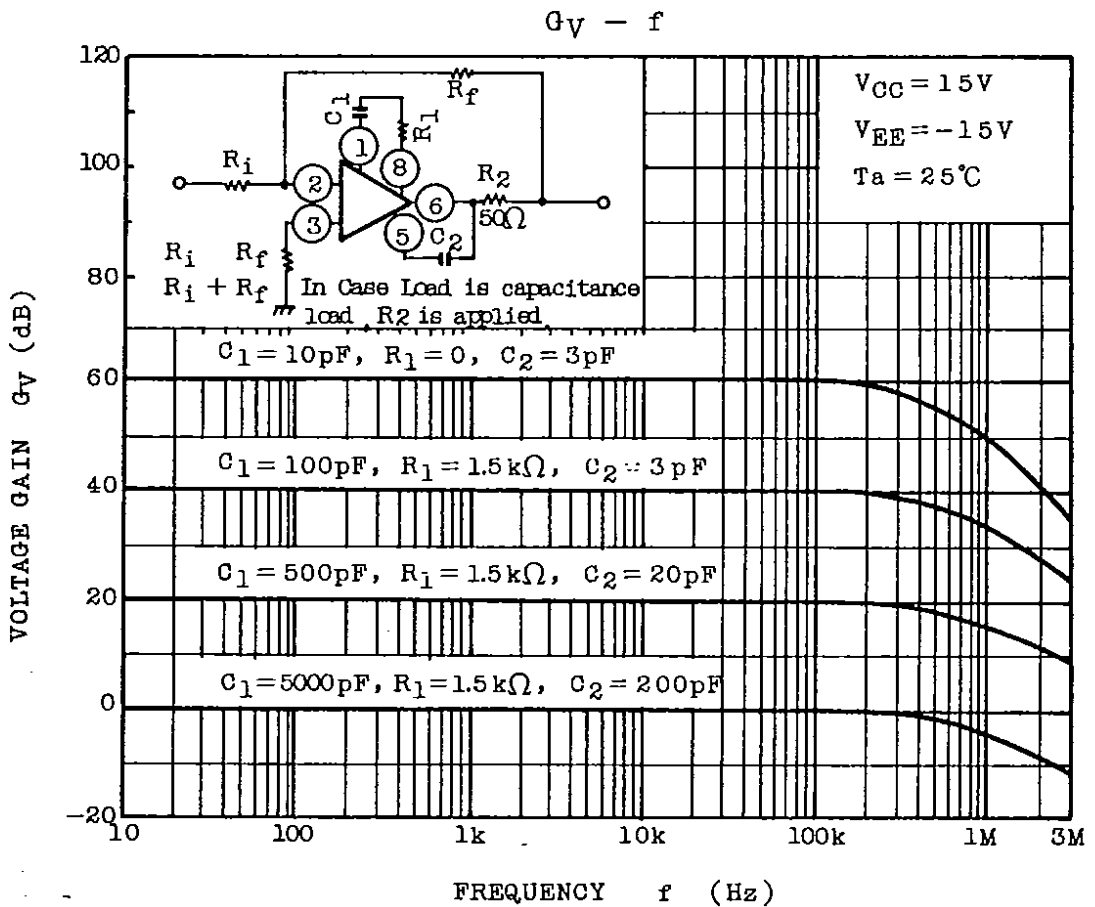
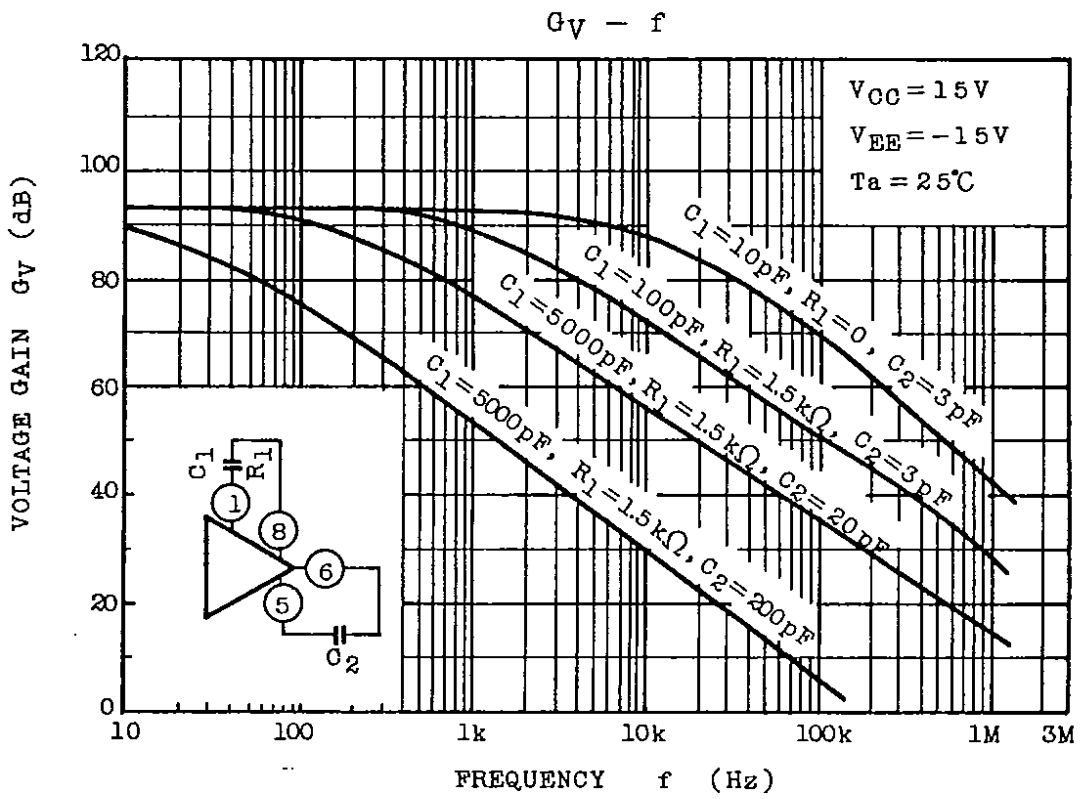


$I_I - T_a$

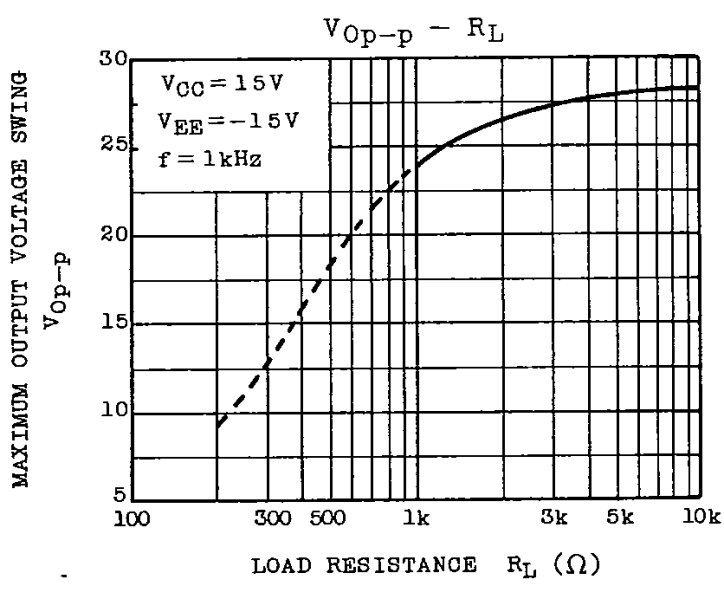
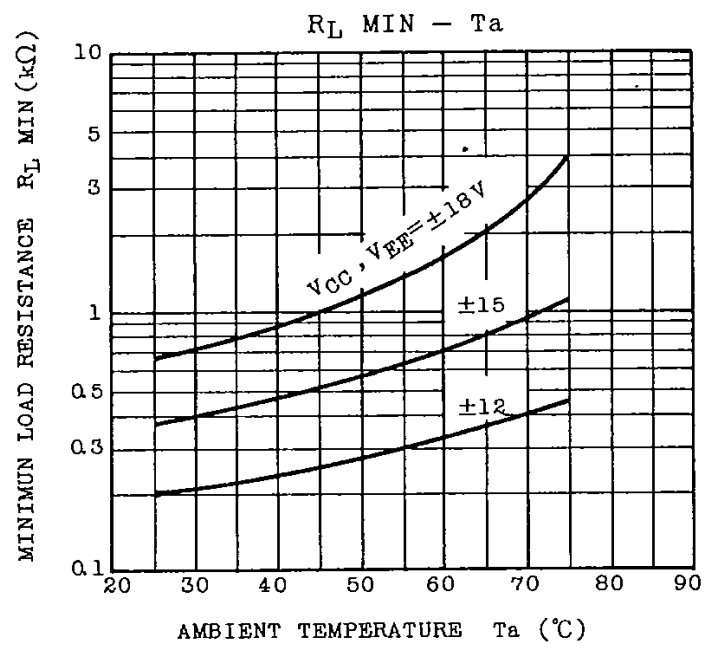
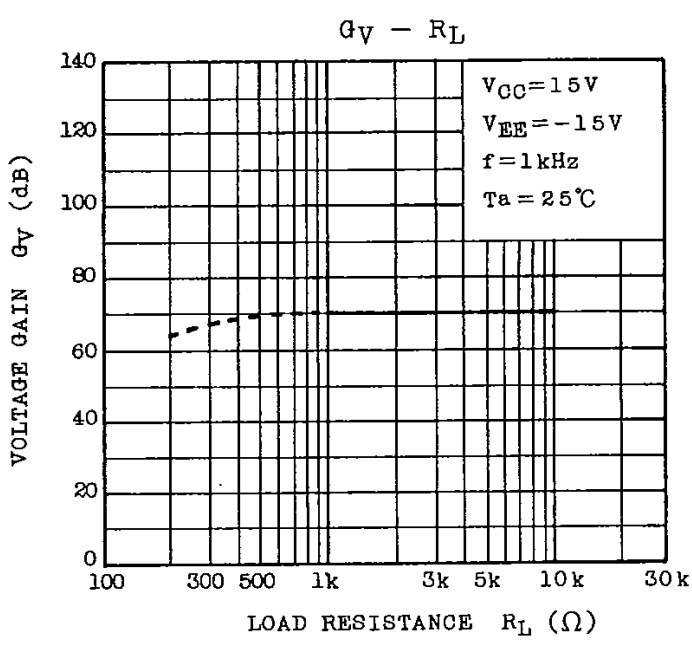








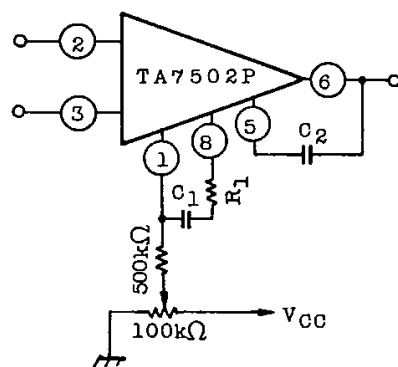




## INPUT OFFSET VOLTAGE ADJUSTMENT

The input offset voltage of the TA7502P can easily be nulled, as shown in Fig.1 (a). In this way its stability directly depends on power supply stability. The other power supply  $V_{BB}$  should be added, as shown in Fig.1 (b), when power supply of operational amplifier is unregulated.

(a)



(b)

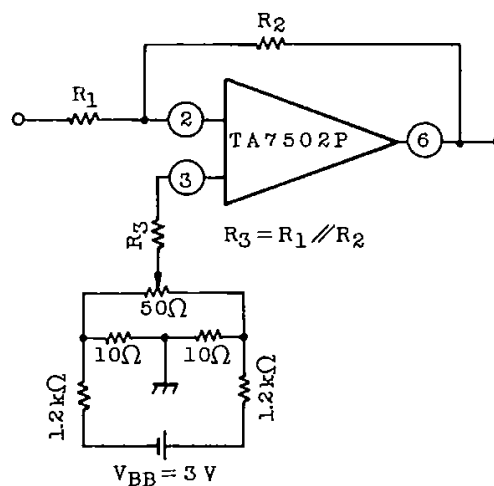


Fig. 1 OFFSET VOLTAGE ADJUSTMENTS

## HYSTERESIS PREVENTION

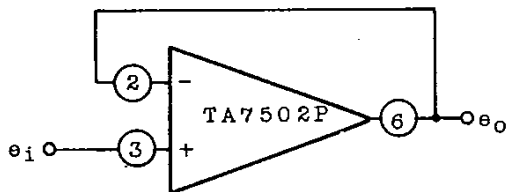
The TA7502P has hysteresis at the positive area in its transfer characteristics. Because when voltage at Term.2 exceeds voltage at Term.1 (about 10V), the transistor in IC chip will be saturated and occur a kind of oscillation phenomenon by becoming positive feedback loop.

It is called "Latch up" and the TA7502P may give rise to abnormal behavior or catastrophic failure under this condition.

To protect against damage from latch up, a diode should be added between Term. 6 and Term. 8, as shown in Fig. 3 (a) and a resistor R should be added in series with feedback loop in Voltage follower application.

The TA7502P has a wide range of common mode input voltage ( $\pm 9V$ ), and its linearity is guaranteed 9 volts in the electrical characteristics. Furthermore, it is possible to improve input voltage ranges by changing power supply voltage, as shown in Table 1.

(a)



(b)

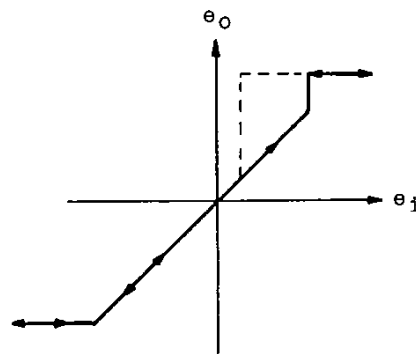
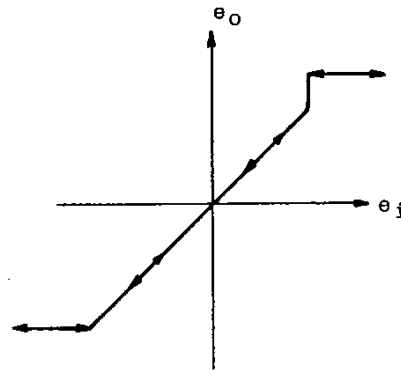
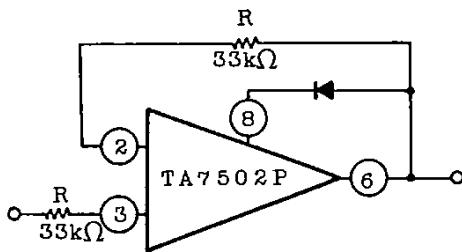


Fig. 2 BASIC VOLTAGE FOLLOWER AND TRANSFER CHARACTERISTIC



(a) VOLTAGE FOLLOWER FREE FROM LATCH UP

(b) INPUT/OUTPUT CHARACTERISTICS

V <sub>CC</sub> (V)	V <sub>EE</sub> (V)	CMV <sub>IN(+)</sub> (V)	CMV <sub>IN(-)</sub> (V)
+5	-25	+1.4	-23.7
+10	-20	+6.0	-18.5
+15	-15	+11.0	-13.7
+20	-10	+15.9	-8.6
+25	-5	+21.1	-3.8

TABLE 1. SUPPLY VOLTAGE-COMMON MODE VOLTAGE

## OVERLOAD PROTECTION

Input Protection against differential signal up to the levels of the maximum differential voltage can be provided by the diode clamps of Fig. 4.

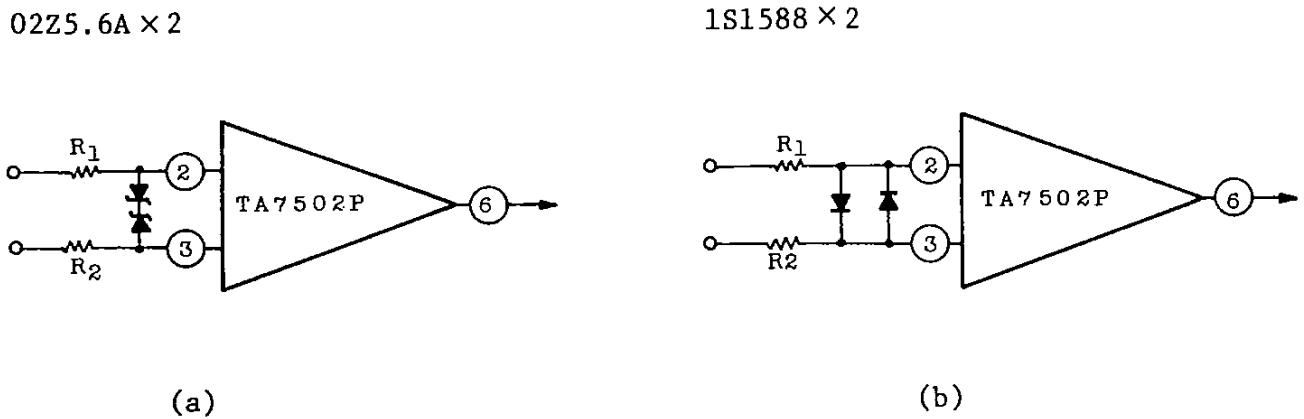


Fig. 4 INPUT PROTECTION AGAINST DIFFERENTIAL INPUT OVERLOAD .

## OUTPUT SHORT CIRCUIT PROTECTION

The TA7502P endure short circuit current of 80mA maximum for five second at 25°C ambient temperature without degradation. The circuit in Fig. 6 is applied to protect TA7502P from long time short current.

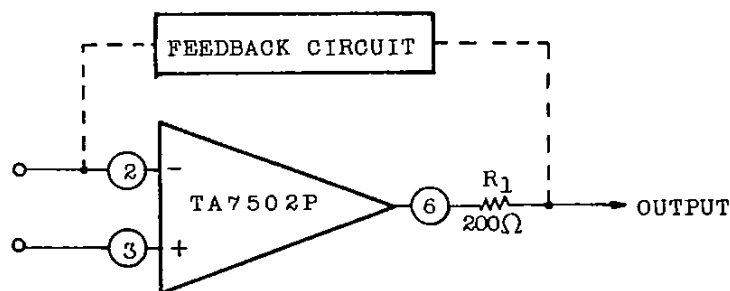


Fig. 5 OUTPUT SHORT CIRCUIT PROTECTION