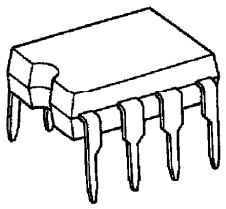
TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

TA75254P

SINGLE OPERATIONAL AMPLIFIER

The TA75254P monolithic instrumentation operational amplifier combined superlative performance in low signal level applications and has low input offset voltage and bias current combined with very high levels of gain, input impedance, CMRR and SVRR.
The TA75254P is an excellent choice for a wide variety of applications including strain gauge and thermocouple bridges, high gain active filters, integrators and samlpe-and-hold amplifiers.



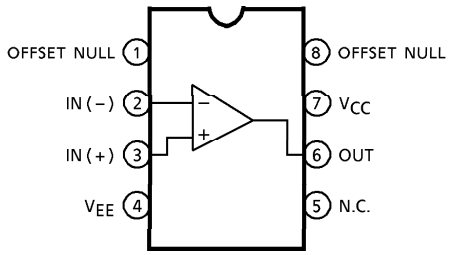
DIP8-P-300-2.54A

Weight : 0.5g (Typ.)

FEATURES

- Low Input Offset Voltage : 1.3mV MAX.
- Low Input Offset Voltage Drift : 1.5μV/°C
- Low Input Bias Current : 30nA MAX.
- Low Input Offset Current : 10nA MAX.
- Internally Frequency Compensation
- Offset Nulling Capability
- Supply Voltage : ±3~±18V

PIN CONNECTION (TOP VIEW)



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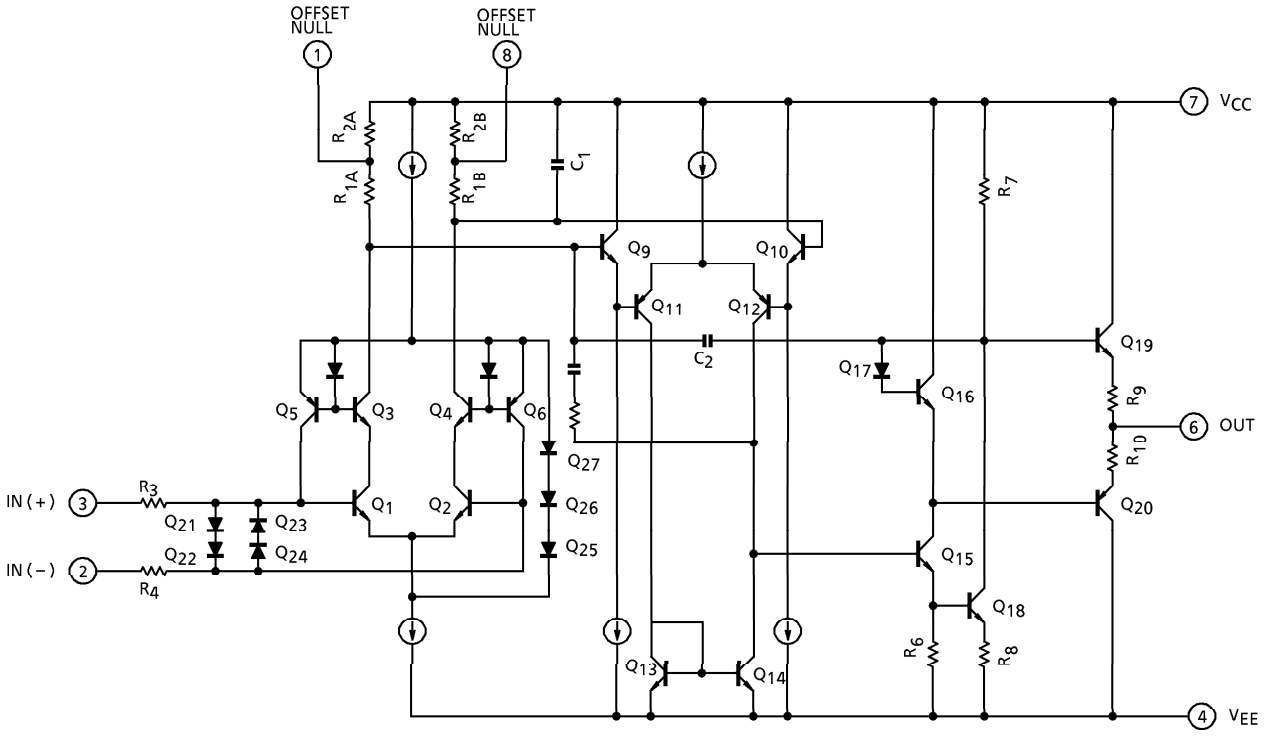
EQUIVALENT CIRCUIT



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}, V_{EE}	18, − 18	V
Differential Voltage	DV_{IN}	± 12	V
Input Voltage	V_{IN}	V_{CC}~V_{EE}	V
Power Dissipation	P_D	500	mW
Operating Temperature	T_{opr}	− 40~85	°C
Storage Temperature	T_{stg}	− 55~125	°C

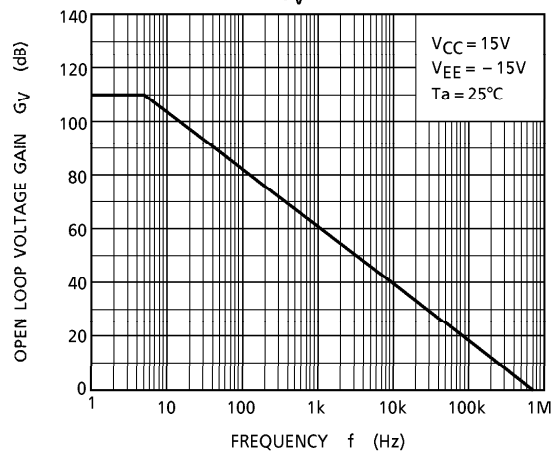
ELECTRICAL CHARACTERISTICS (V_{CC} = 15V、 V_{EE} = − 15V、 Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	V_{IO}	—	$R_g \leqq 10k\Omega$	—	0.3	1.3	mV
Input Offset Current	I_{IO}	—	—	—	0.3	10	nA
Input Bias Current	I_I	—	—	− 30	—	30	nA
Common Mode Input Voltage	CMV_{IN}	—	—	± 13	± 14	—	V
Maximum Output Voltage	V_{OM}	—	$R_L = 10k\Omega$	± 12	± 13	—	V
	V_{OMR}		$R_L = 2k\Omega$	± 11.5	± 12.8	—	
Source Current	I_{source}	—	—	10	25	—	mA
Sink Current	I_{sink}	—	—	10	25	—	mA
Open Loop Voltage Gain	G_V	—	$R_L \geqq 2k\Omega$	86	110	—	dB
Common Mode Input Signal Rejection Ratio	CMRR	—	$R_g \leqq 10k\Omega$	70	110	—	dB
Supply Voltage Rejection Ratio	SVRR	—	$R_g = 10k\Omega$	80	110	—	dB
Slew Rate	SR	—	—	—	0.2	—	V / μs
Unity Gain Cross Frequency	f_T	—	—	—	0.5	—	MHz
Supply Current	I_{CC}, I_{EE}	—	—	—	3.2	6.0	mA
Input Noise Voltage	V_{NI}	—	—	—	1	—	μV_{rms}
Input Resistance	R_{IN}	—	—	—	50	—	MΩ
TC Of Input Offset Voltage (Note 1)	$\Delta V_{IO} / \Delta T$	—	$R_g \leqq 10k\Omega$, unnull	—	1.2	4.5	μV / °C
		—	$R_g \leqq 10k\Omega$, null, $R_P = 20k\Omega$	—	0.4	1.5	
TC Of Input Bias Current	$\Delta I_I / \Delta T$	—	—	—	18	—	PA / °C
TC Of Input Offset Current	$\Delta I_{IO} / \Delta T$	—	—	—	12	—	PA / °C

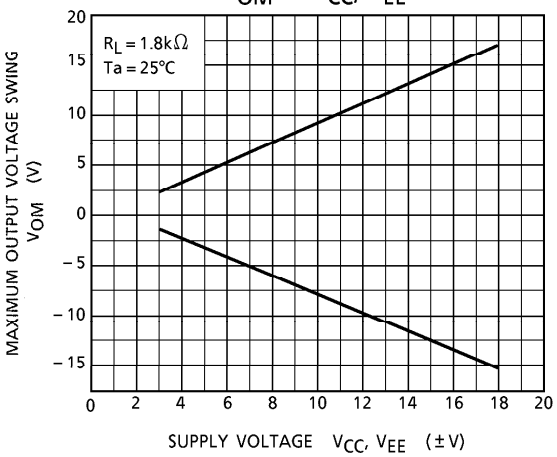
(Note 1) Sample Tested (LTPD10)

CHARACTERISTICS

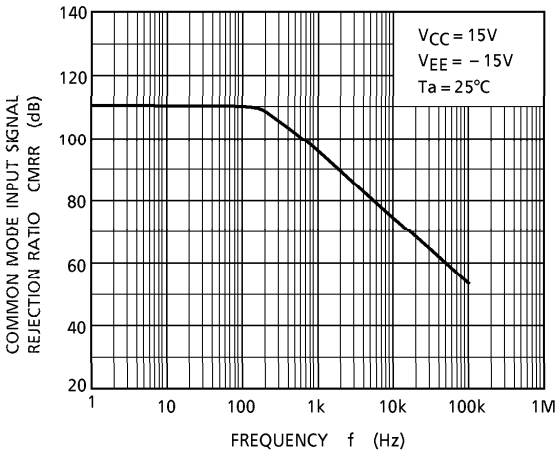
G_V – f



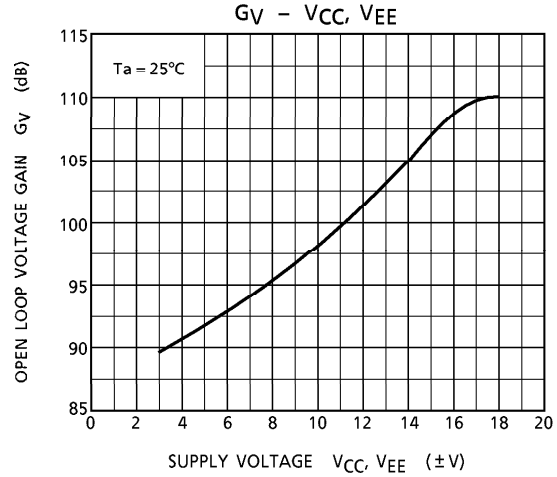
V_{OM} – V_{CC}, V_{EE}



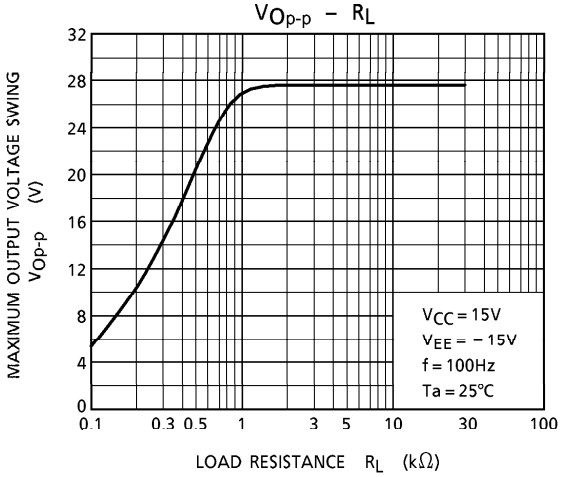
CMRR – f



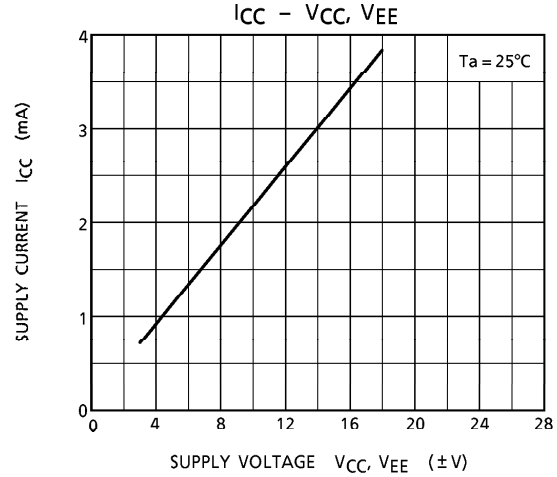
G_V – V_{CC}, V_{EE}

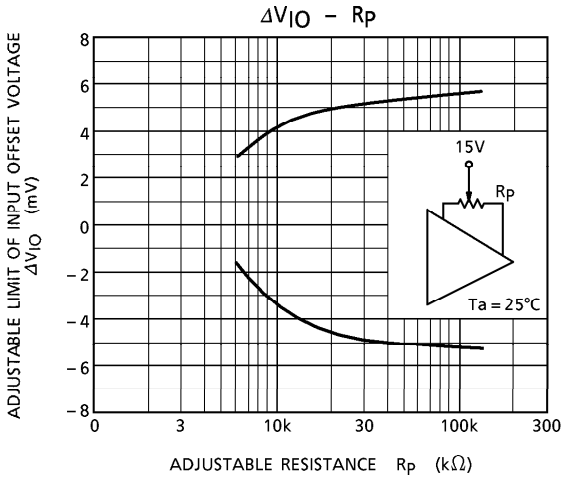


V_{Op-p} – R_L



I_{CC} – V_{CC}, V_{EE}

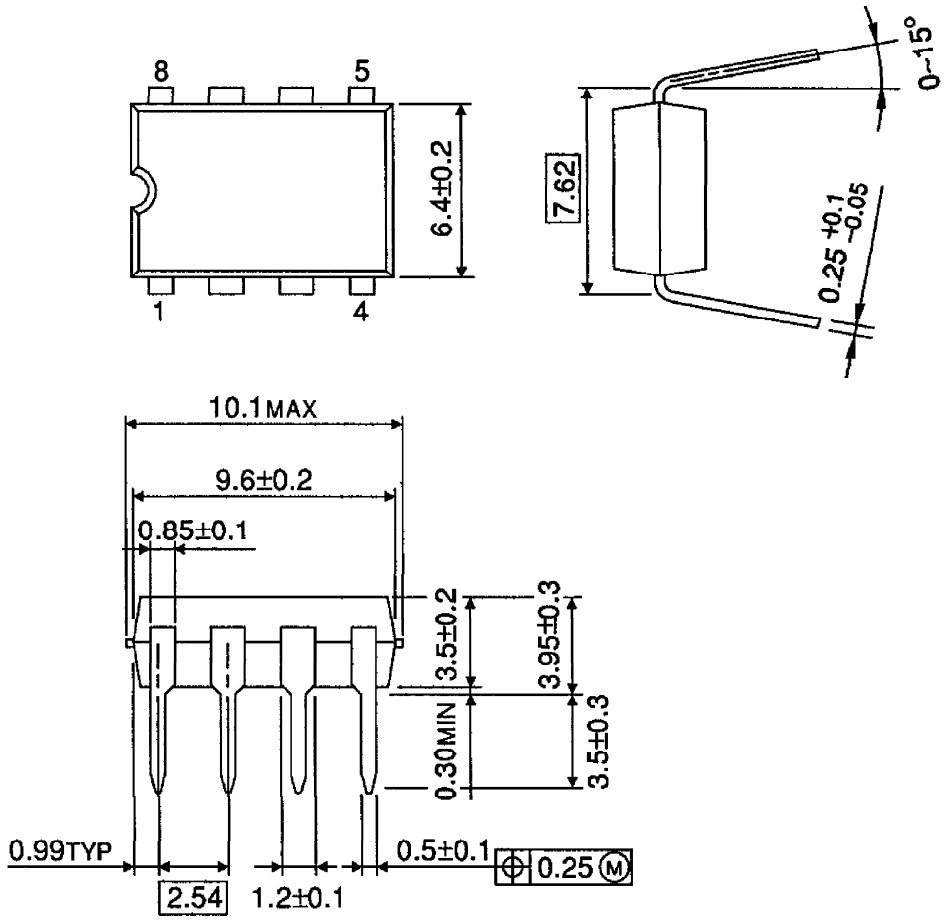



ΔVIO – RP
ADJUSTABLE LIMIT OF INPUT OFFSET VOLTAGE ΔVIO (mV)
8
6
4
2
0
– 2
– 4
– 6
– 8
0
3
10k
30
100k
300
ADJUSTABLE RESISTANCE RP (kΩ)
15V
RP
Ta = 25°C

OUTLINE DRAWING

DIP8-P-300-2.54A

Unit : mm



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