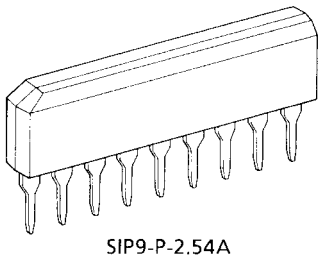
TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

TA8000S,TA8000F

5V VOLTAGE REGULATOR WITH WATCHDOG TIMER

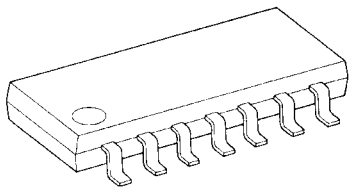
The TA8000S TA8000F is an IC specially designed for automotive microcomputer systems. It produces an output voltage of 5 ± 0.25V without need for adjustment from its accurate reference voltage and amplifier circuit.
At power-on, it outputs a reset signal to reset the system. It will also output a reset signal when the 5 V output voltage drops below 85% because of external disturbance or other problem. It also incorporates a watchdog timer for self-diagnosing the system. When the system malfunctions, the IC generates reset pulses intermittently to prevent the system from running away.

TA8000S



SIP9-P-2.54A

TA8000F



SOP14-P-225-1.27

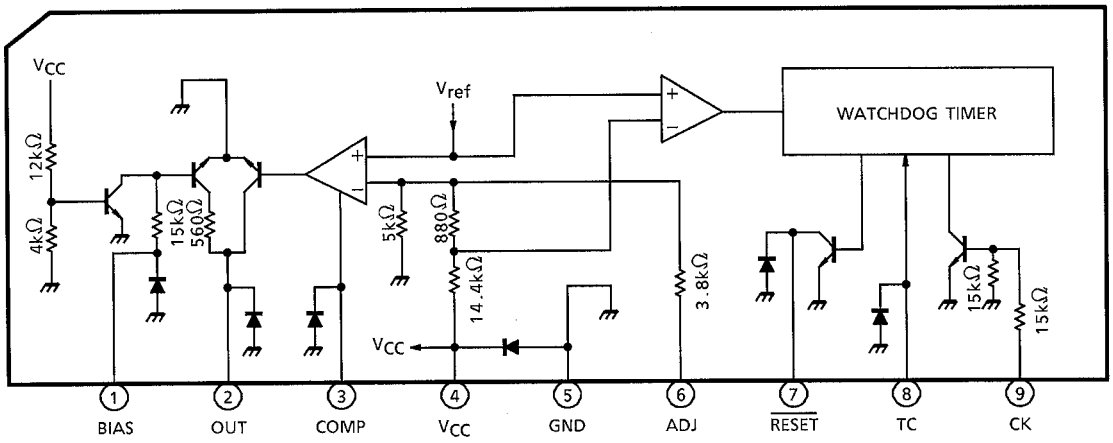
Weight
SIP9-P-2.54A : 0.92 g (typ.)
SOP14-P-225-1.27 : 0.2 g (typ.)

FEATURES

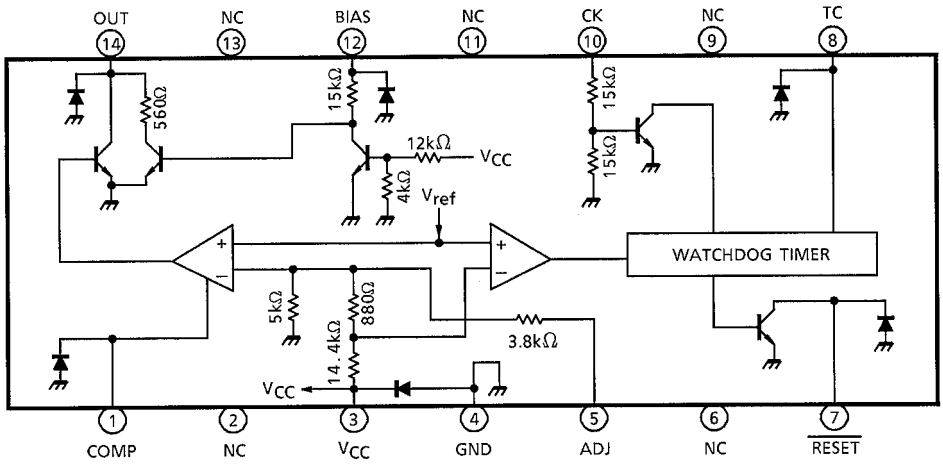
- Accurate output : 5 ± 0.25V
- Output voltage adjusting pin attached
- Power-on reset timer incorporated
- Watchdog timer incorporated
- Wide operating voltage range : 40 V (max.)
- Operating temperature range : from −40 to 85°C
- Load dump protection : 80 V (max.) (1 second)
- Small SIP-9 pin : TA8000S
  SOP-14 pin : TA8000F

BLOCK DIAGRAM AND PIN LAYOUT

TA8000S



TA8000F



Note : The TA8000S and TA8000F are the same chip; only the packages are different.

PIN DESCRIPTION

PIN No.		SYMBOL	DESCRIPTION
TA8000S	TA8000F		
1	12	BIAS	Power supply start pin. The start current is supplied from the input voltage through a resistor. The output current −obtained from this start current is as follows: I_{OUT} (BIAS pin) ≥30×(V_{IN}−0.7) / (15+R1) (mA) where R1 : external resistor connected to BIAS pin (kΩ) This current is absorbed by an internal circuit when V_{CC} increases above 2.7V, in which case I_{OUT} is supplied from V_{CC}.
2	14	OUT	This pin connects to the base of an external PNP transistor for control purposes to stabilize the output voltage. Therefore, the power supply can be designed to suit the load capacitance. Since the recommended current of I_{OUT} is 8mA, the output current that can be flowed is 300mA providing that H_{FE} of the external transistor is 40.
3	1	COMP	This pin is used for phase correction to stabilize the output.
4	3	V_{CC}	Internal circuit power supply pin. This pin also is used to detect the output voltage.
5	4	GND	Ground pin.
6	5	ADJ	Output voltage adjusting pin. The voltage can be raised by inserting a resistor between ADJ and GND and lowered by inserting a resistor between ADJ and V_{CC}. When ADJ and GND are shorted, the output voltage is 10V. (See Typical Characteristics.)
7	7	$\overline{\text{RESET}}$	NPN transistor open-collector output. (1) This output goes low at 85% or less of the rated output voltage. (2) A reset signal is generated whose time constant is determined by CR of the TC pin. (3) When no clock is fed to the CK input, a reset pulse is generated intermittently. This function can be used as a watchdog timer for microcomputer systems.
8	8	TC	This pin is used to set the time for the reset and watchdog timers. Any desired time can be set using external RT and C_T.
9	10	CK	Watchdog timer input pin. Pull up this pin to V_{CC} when you are using only the power-on reset timer.
—	2, 6, 9, 11, 13	NC	Non-connected pin. (Electrically, this pin is completely open.)

FUNCTIONAL DESCRIPTION

The TA8000S / F incorporates a constant-voltage 5V power supply function to feed stable power to the CPU and a system reset function to ensure stable operation of the CPU, etc. These functions are explained below.

(1) Constant-voltage 5V power supply function

This constant-voltage function has the reference voltage V_{ref} in the IC that is insusceptible to temperature changes and input voltage fluctuations. The power supply circuit is designed in such a way that this voltage is stepped up to 5V by using an OP amp and a voltage-dividing resistor. These OP amp and dividing resistor and an output transistor connected to the OP amp output together configure a closed loop.
If you are using only the reset timer and not this power supply function, connect the BIAS, OUT, and COMP pins to GND.

(2) System reset function (See Timing Chart)

- Voltage monitoring function

  When powered on, the power-on reset timer starts counting the moment the voltage V_{CC} applied to the CPU exceeds 4.25V. When powered off, this voltage monitoring function outputs a reset signal immediately when V_{CC} drops below 4.25V. A reset signal also is output immediately when V_{CC} drops for some reason during normal operation. Then, when V_{CC} is restored to the normal voltage and exceeds 4.25V, the power-on reset timer starts counting.

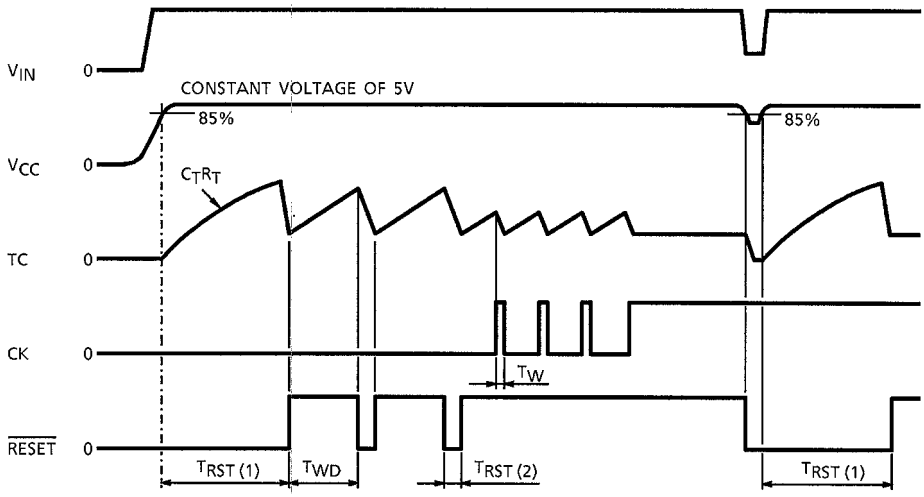
- Power-on reset timer function

  To allow the 5V constant voltage to stabilize at power-on, as well as provide a sufficient time for the clock oscillation in the CPU to stabilize, the device remains reset for a predetermined time before being released from the reset state. The duration of this time can be set as desired by choosing appropriate values for the external resistor and capacitor connected to the TC pin.
  The system starts charging the capacitor when the V_{CC} voltage exceeds 4.25V. When this charge voltage exceeds 4V, the capacitor is discharged by the IC's internal transistor. When the capacitor is discharged down to 2V, the reset signal is inverted to deactivate the reset.

- Watchdog timer function

  Program your system to output a clock each time one program routine is finished in the CPU system software, and input this clock to the CK pin of the IC. The IC's TC pin is repeatedly charged and discharged between 2V and 4V. However, when a clock is input, it switches over and starts discharging in the middle of charging and then starts charging from 2V again. Since the clock is generated at predetermined intervals when the CPU system is operating normally, the TC pin switches over and starts discharging before the charge voltage reaches 4V. However, if no clock is input while being charged from 2V to 4V, the clock is assumed to have stopped, i.e., the CPU system has gone wild, so that a reset signal is output to reset the CPU system.
  The IC's CK pin is connected to the CPU system with a differential circuit. This is to ensure that when an erratic condition occurs in the CPU system, a low signal is always input to the CK pin regardless of whether the clock output from the CPU has stopped in the high or low state. When the CK pin is fixed high, no reset signal is output, in which case only the power-on reset timer is useful.

TIMING CHART



Note: $T_{RST(1)}$, $T_{RST(2)}$, T_{WD}, T_W : See Electrical Characteristics.

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Input Voltage	V_{IN1}	80 (1s)	V
	V_{IN2}	−5 ~ + 16	
Output Current	I_{OUT1}	10	mA
	I_{OUT2}	4	
Output Voltage	V_{OUT1}	80 (1s)	V
	V_{OUT2}	16	
Power Dissipation	P_D	500 / 280	mW
Operating Temperature	T_{opr}	−40~85	°C
Storage Temperature	T_{stg}	−55~150	°C
Lead Temperature time	T_{sol}	260 (10s)	°C

Note: V_{IN1} : BIAS input
V_{IN2} : CK input
I_{OUT1}, V_{OUT1} : OUT output
I_{OUT2}, V_{OUT2} : $\overline{\text{RESET}}$ output
P_D : TA8000S / TA8000F

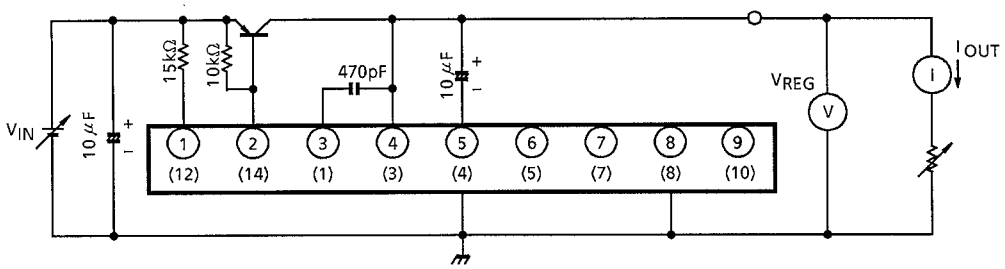
ELECTRICAL CHARACTERISTICS (V_{IN} = 6 to 17V, Ta = −40 to 85°C)

CHARACTERISTIC	SYMBOL	PIN	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Output Voltage	V_{REG}	V_{CC}	1		4.75	5.0	5.25	V
Line Regulation		V_{CC}	—	VIN = 6~40V	—	0.1	0.5	%
Load Regulation		V_{CC}	—	I_{LOAD} = 1~50mA	—	0.1	0.5	%
Temperature Coefficient		V_{CC}	—		—	0.01	—	% / °C
Output Voltage	V_{OL}	$\overline{RESET}$	2	I_{OL} = 2mA	—	—	0.5	V
Output Leakage Current	I_{LEAK}	$\overline{RESET}$	3	V_{OUT} = 10V	—	—	5	μA
Input Current	I_{IN}	TC	4	V_{IN} = 0~3.5V	−3	—	3	μA
Threshold Voltage	V_{IH}	TC	5	$\overline{RESET}$ High to Low	—	80%× V_{REG}	—	V
	V_{IL}			$\overline{RESET}$ Low to High	—	40%× V_{REG}	—	
Input Current	I_{IN}	CK	6	V_{IN} = 5V	—	0.3	0.7	mA
Input Voltage	V_{IH}	CK	5		2	—	—	V
	V_{IL}	CK	5		—	—	0.5	
Reset Detect Voltage		V_{CC}	—		82%× V_{REG}	85%× V_{REG}	88%× V_{REG}	V
Standby Current	I_S	V_{CC}	8	V_{IN} = 14V	—	5	6.5	mA
Watchdog Timer	T_{WD}	$\overline{RESET}$	7		0.9× C_TR_T	1.1× C_TR_T	1.3× C_TR_T	ms
Reset Timer (1)	$T_{RST\ (1)}$	$\overline{RESET}$	7		1.3× C_TR_T	1.6× C_TR_T	1.9× C_TR_T	
Reset Timer (2)	$T_{RST\ (2)}$	$\overline{RESET}$	7		0.15× C_T	0.3× C_T	0.6× C_T	
Clock Pulse Width	T_W	CK	—		3	—	—	μs

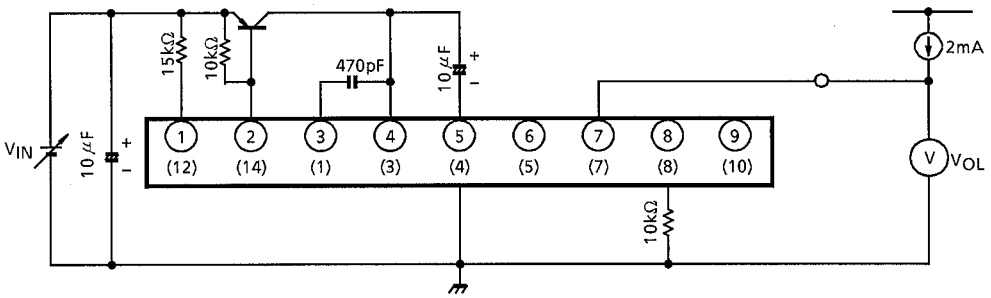
Note: Reset timer (1) : Power-on reset time
Reset timer (2) : Watchdog reset time
The unit for C_T is μF , the unit for R_T is kΩ

TEST CIRCUIT (Numbers in O show pin numbers of the TA8000S; those in ( ) show pin numbers of the TA8000F.)

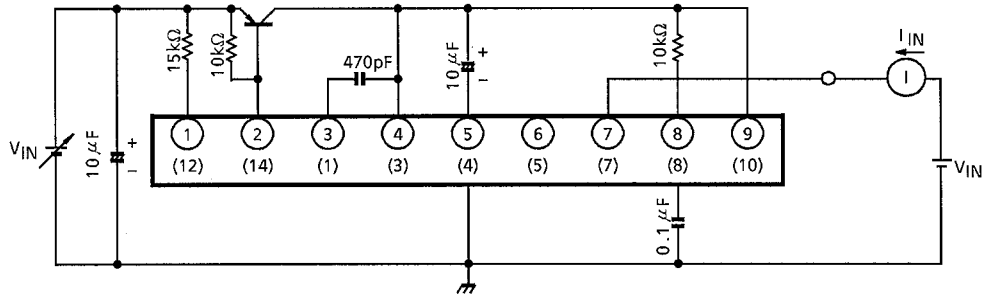
1. V_{REG}



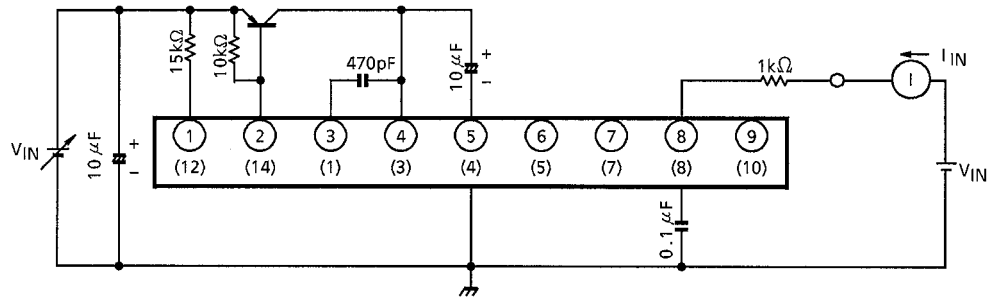
2. V_{OL} ($\overline{RESET}$)



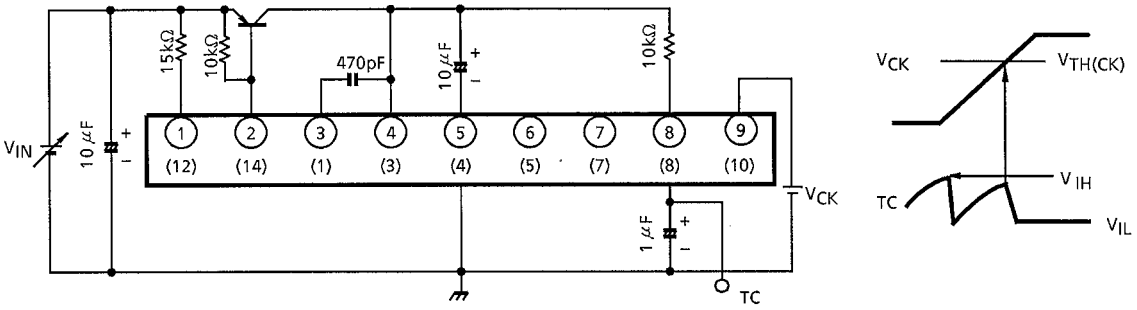
3. I_{LEAK} ($\overline{RESET}$)



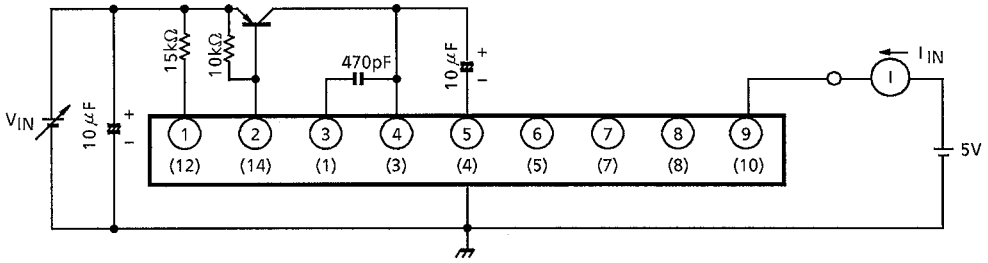
4. I_{IN} (TC)



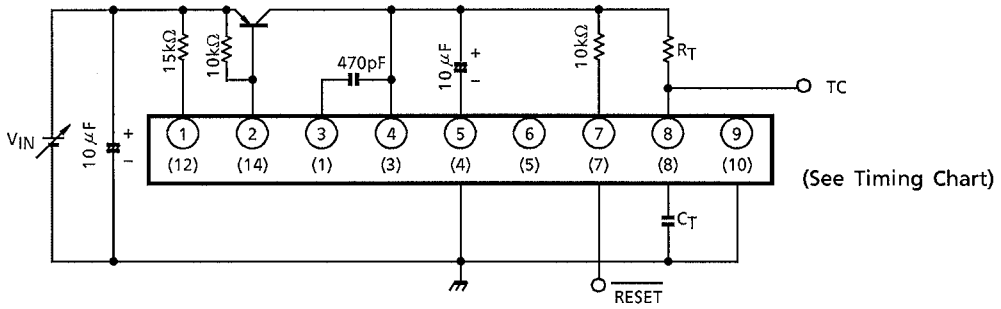
5. V_{IH}, $V_{IL\ (TC)}$, V_{IH}, $V_{IL\ (CK)}$



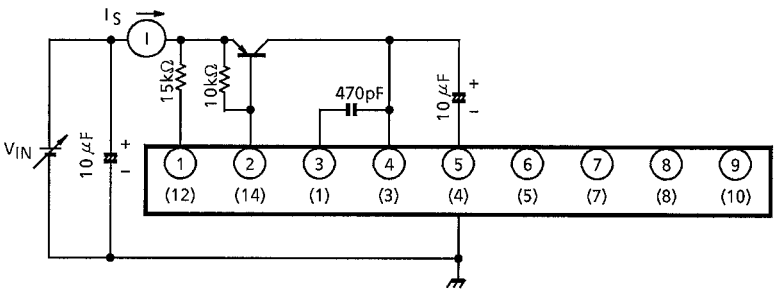
6. $I_{IN\ (CK)}$



7. V_{RESET}, T_{WD}, $T_{RST\ (1)}$, $T_{RST\ (2)}$



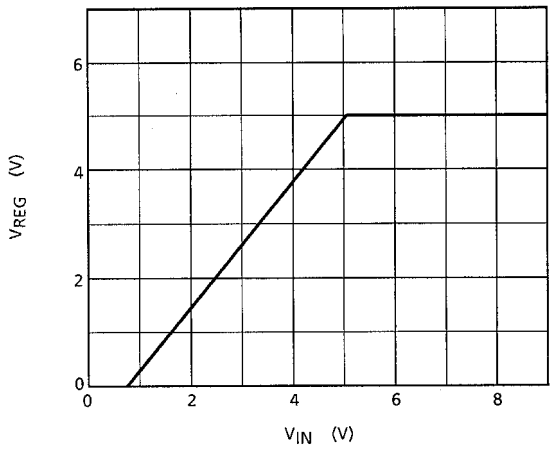
8. I_S



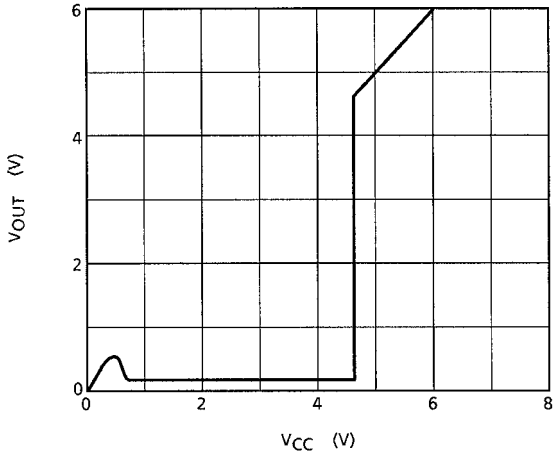
TYPICAL CHARACTERISTICS

1. Input-output characteristic

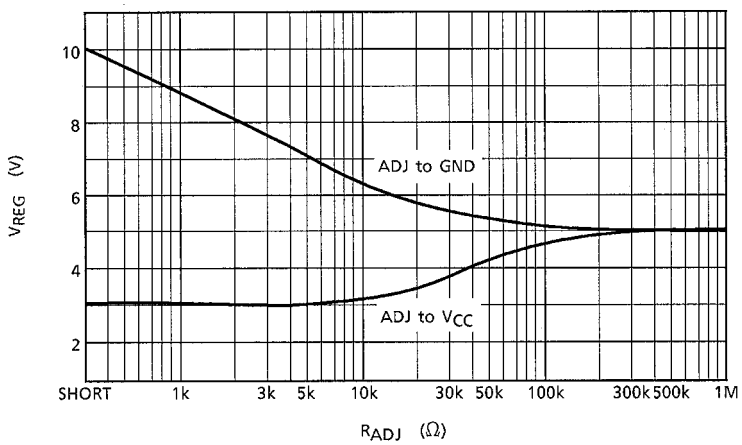
(R_L = 25Ω, external transistor 2SA968-Y)
(R_L: Load resistance between V_{REG} and GND)



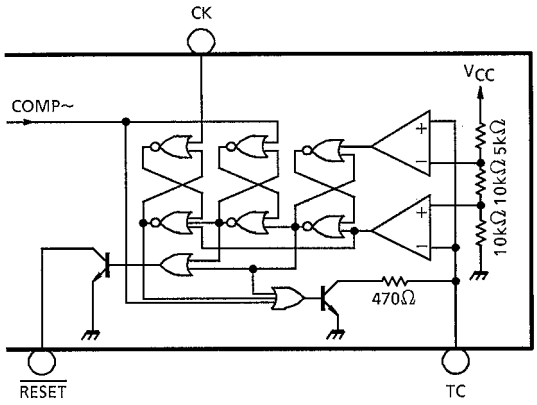
2. Reset Output Characteristic



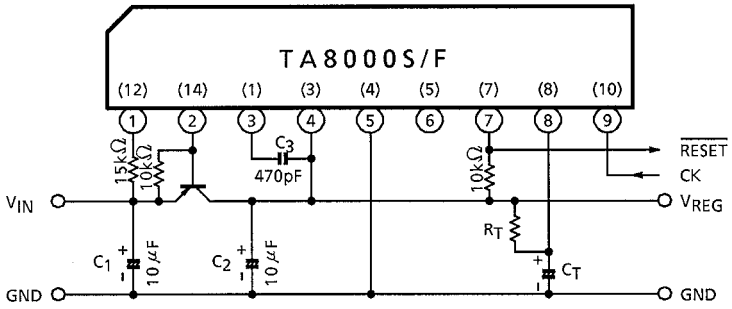
3. Output Adjusting Resistance Characteristic



RESET TIMER EQUIVALENT CIRCUIT



EXAMPLE OF APPLICATION CIRCUIT (Numbers in O show pin numbers of the TA8000S; those in ( ) show pin numbers of the TA8000F.)



*: Cautions for Wiring

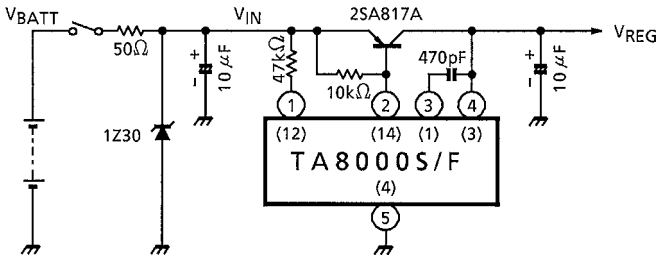
1. C_1 and C_2 are for absorbing disturbance, noise, etc. Connect them as close to the IC as possible.
2. C_3 is for phase compensation. Also, connect C_3 close to the IC.

120 Vpeak LOAD DUMP

Note : No protection is needed if a voltage above 80V is not applied. Therefore, protection by a Zener diode and resistor is unnecessary.

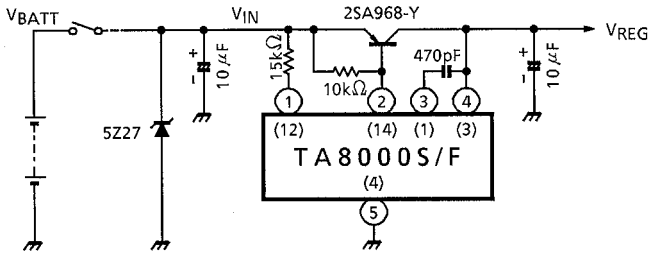
1. Low Output Current Circuit

I_{LOAD} = 10mA Max., V_{BATT} = 6 to 17V

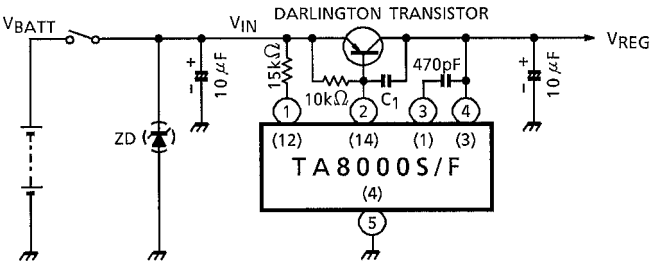


2. High Output Current Circuit

I_{LOAD} = 300mA Max., V_{BATT} = 6~17V



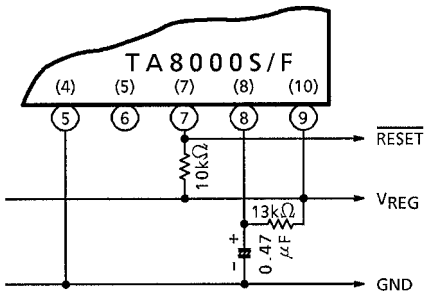
EXAMPLE OF APPLICATION CIRCUIT USING DARLINGTON TRANSISTOR



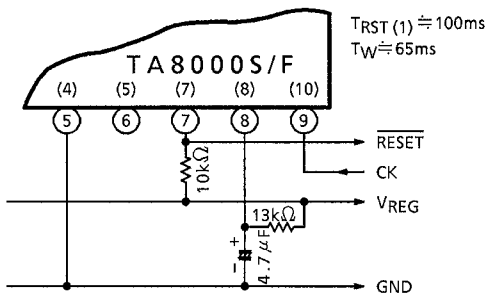
*: ● Select a C_1 value according to the working condition - - typically above 2000pF.
● Insert ZD when necessary.

APPLICATION CIRCUIT OF WATCHDOG / RESET TIMER

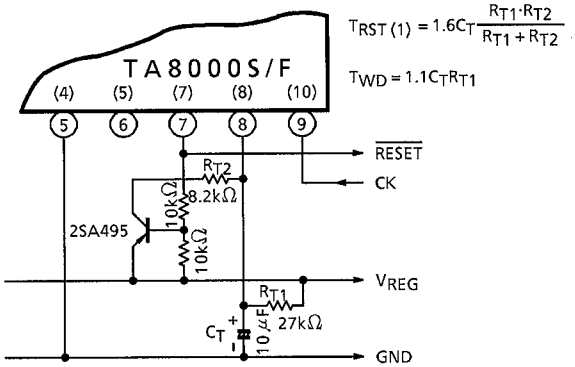
1. $T_{RST\ (1)} \approx 10ms$ Power-On Reset Timer



2. $T_{RST\ (1)} \approx 1.5T_{WD}$



3. $T_{RST\ (1)} \approx 100ms$, $T_{WD} \approx 300ms$



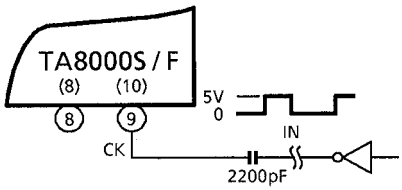
4. Recommended Conditions

PART NAME	MIN	MAX	UNIT
C_T	0.01	100	μF
R_T	5	100	kΩ
R_{T1}	—	100	kΩ
R_{T1} // R_{T2} (Note)	5	—	kΩ

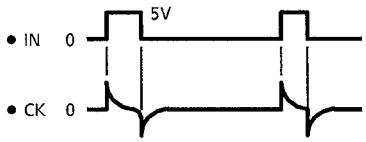
Note: R_{T1} // R_{T2} = (R_{T1}×R_{T2}) / (R_{T1}+R_{T2})

CK INPUT APPLICATION CIRCUIT

Capacitor Coupling



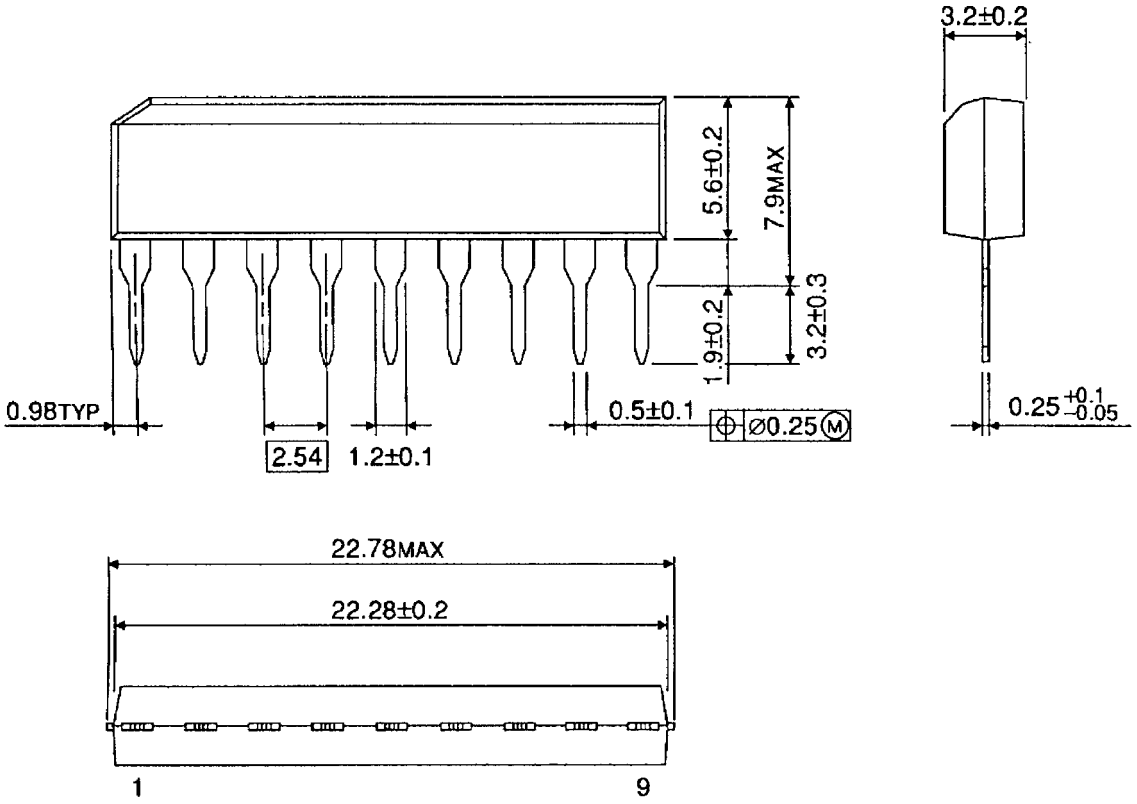
Timing Chart



The capacitor coupling allows reset pulses to be supplied intermittently from the $\overline{\text{RESET}}$ pin whether the input level (IN) is high or low.

PACKAGE DIMENSIONS

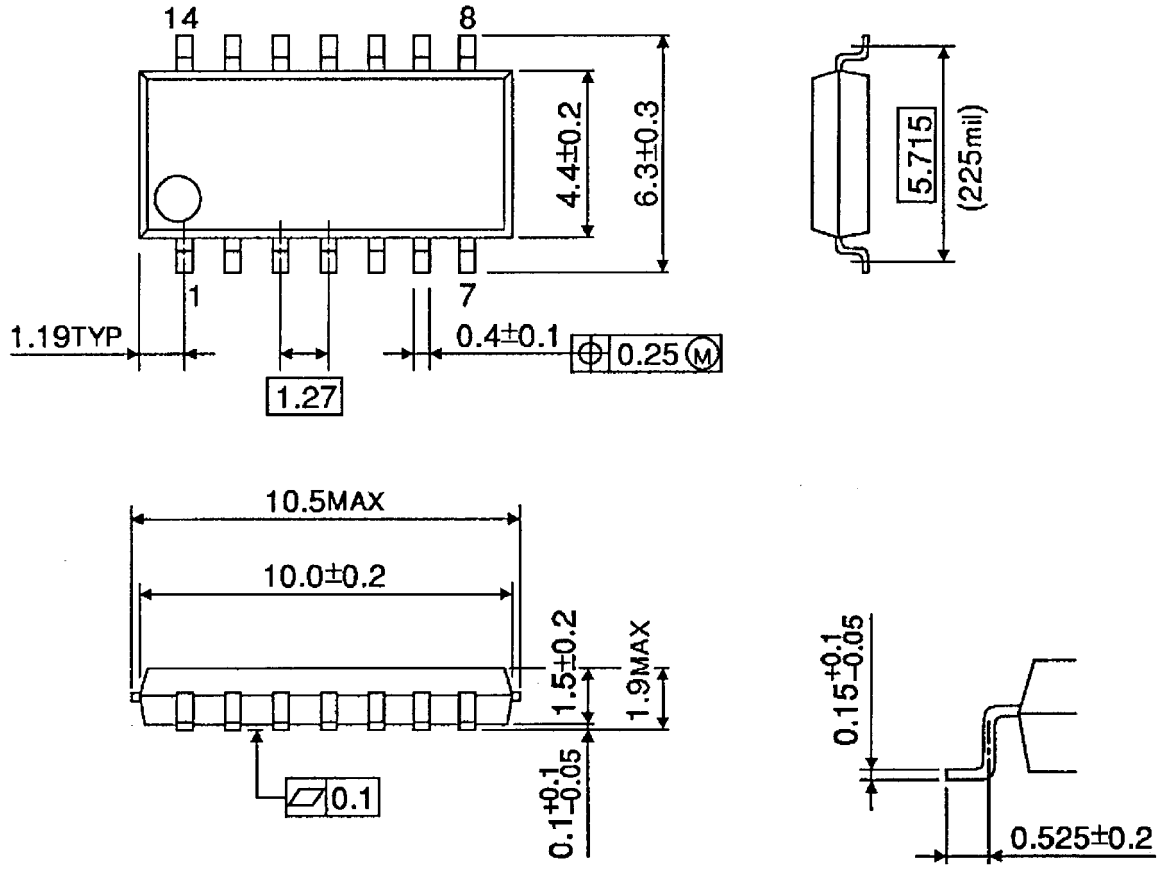
SIP9-P-2.54A Unit : mm



Weight: 0.92 g (typ.)

PACKAGE DIMENSIONS

SOP14-P-225-1.27 Unit : mm



Weight: 0.2 g (typ.)

RESTRICTIONS ON PRODUCT USE

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