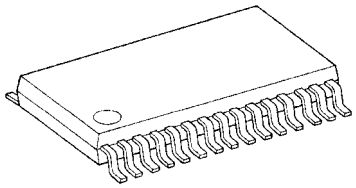
TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

TA8482FN

BRIDGE DRIVER + SENSOR AMP 1−CHIP IC FOR DC MOTORS

TA8482FN is a loading motor driver for video camera. It is a 1−chip IC with tape top / end sensor amplifiers, reel FG amplifiers, and buffer amplifiers for servo error L.P.F.



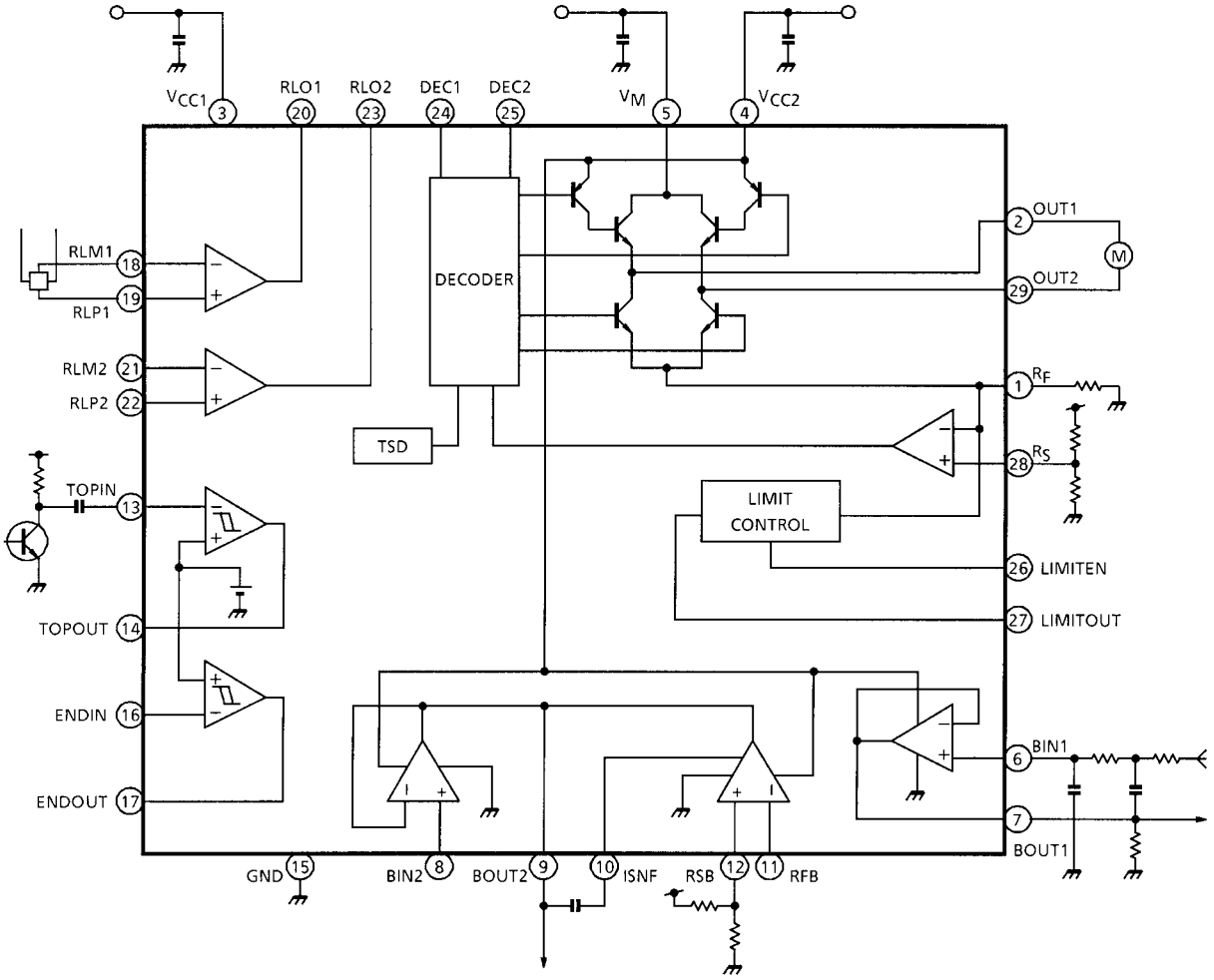
SSOP30-P-300-0.65

Weight: 0.17 g (Typ.)

FEATURES

- 4 Modes ：Forward Rotation, Reverse Rotation, Stop, and Brake
- Built−in Current Limiter
- Built−in Thermal Shutdown Circuit
- Built−in Tape Top / End Sensor Amplifiers
- 2 Built−in Reel FG Amplifiers
- 2 Built−in Buffer Amplifiers for Servo Error L.P.F.
- Built−in Buffer Limiter
- Package：VSOP−30

BLOCK DIAGRAM



PIN FUNCTION

PIN No.	SYMBOL	PIN NAME
1	R_F	Output current detect pin
2	OUT1	Motor drive output pin 1
3	V_{CC1}	Power supply input pin 1
4	V_{CC2}	Power supply input pin 2
5	V_M	Motor drive voltage input pin
6	BIN1	Buffer amp 1 input pin
7	BOUT1	Buffer amp 1 output pin
8	BIN2	Buffer amp 2 input pin
9	BOUT2	Buffer amp 2 output pin
10	ISNF	Buffer limiter amp phase compensating pin
11	RFB	Buffer limiter amp input pin
12	RSB	Buffer limiter amp reference voltage input pin
13	TOPIN	Tape−top sensor amp input pin
14	TOPOUT	Tape−top sensor output pin
15	GND	GND pin
16	ENDIN	Tape−end sensor amp input pin
17	ENDOUT	Tape−end sensor amp output pin
18	RLM1	Reel FG amp 1 negative side input pin
19	RLP1	Reel FG amp 1 positive side input pin
20	RLO1	Reel FG amp 1 output pin
21	RLM2	Reel FG amp 2 negative side input pin
22	RLP2	Reel FG amp 2 positive side input pin
23	RLO2	Reel FG amp 2 output pin
24	DEC1	Decoder input pin 1
25	DEC2	Decoder input pin 2
26	LIMITEN	Limiter controller input pin
27	LIMITOUT	Limiter controller output pin
28	R_S	Limiter amp reference voltage input pin
29	OUT2	Motor drive output pin 2
30	N.C	—

TRUTH TABLE

DECODER CIRCUIT

DEC1	DEC2	OUT1	OUT2
L	L	Z	Z
H	L	H	L
L	H	L	H
H	H	L	L

Z: High impedance

LIMITER CONTROLLER CIRCUIT

LIMITEN	LIMITER AMP CIRCUIT	LIMITOUT
H	When operated (when output current is detected)	L
	When not operated	H
L	H	

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Small Signal Section Supply Voltage	V_{CC1}	10	V
Output Section Supply Voltage	V_{CC2}	11	V
Output Section Supply Voltage	V_M	8	V
Output Current	I_O	0.6	A
Power Dissipation	P_D	0.86 (Note 1)	W
		1.13 (Note 2)	
Operating Temperature	T_{opr}	−20~80	°C
Storage Temperature	T_{stg}	−55~150	°C

Note 1: Single body
Note 2: Substrate mounting (50 × 50 × 1.6 mm Cu 40%)
*: Devices may break outside the range of maximum rating.

OPERATING SUPPLY VOLTAGE RANGE (Ta = 25°C)

CHARACTERISTIC	SYMBOL	OPERATING RANGE	UNIT
Small Signal Section Supply Voltage	V_{CC1}	2.7~4.0	V
Output Section Supply Voltage	V_{CC2}	V_{CC1}~9.0	V
Output Section Supply Voltage	V_M	1.0~7.0 (Note 3)	V

Note 3: $V_{CC2} \geq V_M$
*: The range of operating conditions covers normal operations under the condition specified for electrical characteristics.

ELECTRICAL CHARACTERISTICS
(V_{CC1} = 3.0 V, V_{CC2} = 4.75 V, V_M = 3.0 V, Ta = 25°C)

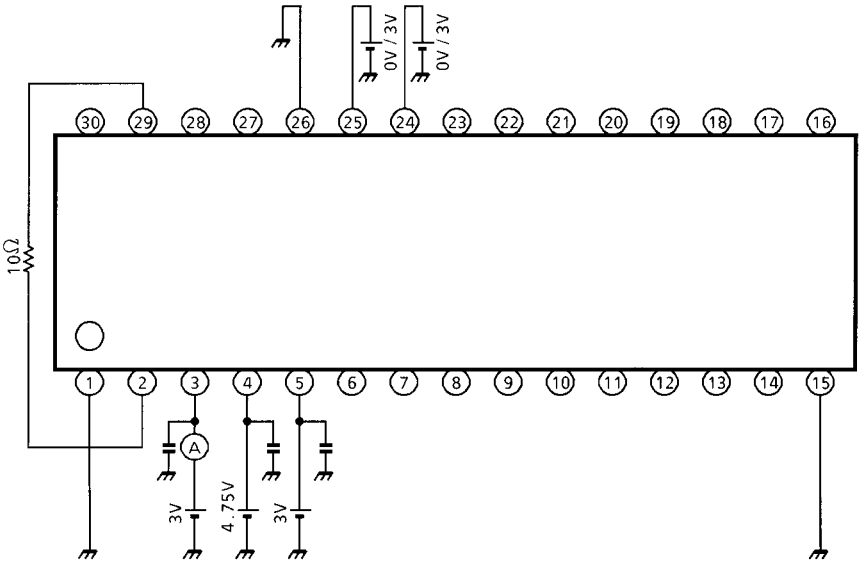
CHARACTERISTIC			SYMBOL	TEST CIR-CUIT	TEST CONDITIONS	MIN	TYP.	MAX	UNIT
Supply Current			I_{CC11}	1	R_L = 10 Ω DEC1 : L, DEC2 : L	—	3	4.2	mA
			I_{CC12}		R_L = 10 Ω DEC1 : H / L, DEC2 : L / H	—	20	30	
			I_{CC13}		R_L = 10 Ω DEC1 : H, DEC2 : H	—	42	60	
			I_{CC21}	2	R_L = 10 Ω, V_{CC1} = 0 V DEC1 : L, DEC2 : L	—	—	1	μA
			I_{CC22}		R_L = 10 Ω DEC1 : L, DEC2 : L	—	0.7	1	mA
			I_{CC23}		R_L = 10 Ω DEC1 : H / L, DEC2 : L / H	—	20	30	
			I_{CC24}		R_L = 10 Ω DEC1 : H, DEC2 : H	—	0.7	1	
			I_M	3	R_L = 10 Ω DEC1 : L, DEC2 : L	—	—	1	μA
Decoder Circuit	Input Voltage	"H" level	V_{IN1}	4	R_L = 10 Ω	2.0	—	—	V
		"L" level	V_{IN2}		R_L = 10 Ω	—	—	0.6	
	Input Current		I_{IN}		V_{IN} = 3.0 V	—	—	3	μA
	Input Leakage Current		I_{INL}		V_{IN} = 0 V	—	—	1	
Output Circuit	Saturation Voltage (Upper Side + Lower Side)		$V_{sat\ (H+L)}$	5	I_O = 0.2 A	—	0.3	0.45	V
					I_O = 0.4 A	—	0.6	0.75	
Current Limiter Amp	Reference Voltage Input Range		V_{RS}	6		0.05	—	1.0	V
	Detecting Voltage		V_{LIMIT}	7	R_L = 10 Ω, R_F = 1 Ω V_{RS} = 0.2 V	0.18	0.2	0.22	
Current Limiter Controller	Input Voltage	"H" level	$V_{LE(H)}$	8	R_L = 10 Ω	2.0	—	—	V
		"L" level	$V_{LE(L)}$		R_L = 10 Ω	—	—	0.6	
	Input Current		I_{LC}		V_{LE} = 3.0 V	—	—	3	μA
	Input Leakage Current		I_{LCL}		VLE = 0 V	—	—	1	
	Output Voltage	"H" level	$V_{LO(H)}$		I_O = 10 μA	V_{CC1} −0.5	—	—	V
		"L" level	VLO(L)		I_O = 10 μA	—	—	0.4	

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITIONS	MIN	TYP.	MAX	UNIT
Reel FG Amp	Common-Phase Voltage Range	V_{CMRFG}	9		1.0	—	2.0	V
	Input Current	I_{FG}	10	V_{CMRFG} = 1.5 V	—	—	1	μA
	Output Offset Voltage	V_{OFFG}			—	0	±290	mV
	Closed Loop Voltage Gain	G_{VFG}	11	f_{FG} = 1 kHz	27	29	31	dB
	Open Loop Voltage Gain	G_{VOFG}	—	f_{FG} = 1 kHz Design assurance	—	55	—	dB
	Output Residual Voltage	Vsat-FG (H)	12	I_O = 10 μA (Upper side)	—	—	0.2	V
		$V_{sat-FG\ (L)}$		I_O = 10 μA (Lower side)	—	—	0.2	
Top/End Sensor Amp	Input Resistance	R_{IN}	13		4	5	6	kΩ
	Minimum Input Sensitivity	R_{HS}	—	Design assurance	30	40	50	mV_{p-p}
Buffer Amp	Input voltage range	V_{CMRB}	14		0	—	V_{CC2}	V
	Input Current	I_B		V_{BIN} = 0 V, (Note)	—	—	1	μA
	Input Offset Voltage	V_{OFB}		V_{BIN} = 1.5 V	—	0	±7	mV
	Output Voltage (Upper Side)	$V_{OB(H)}$		R_L =20 kΩ (against GND)	V_{CC2} −1.7	—	—	V
	Output voltage (Lower Side)	$V_{OB(L)}$	15	V_{BOUT} = 0 V, R_L = 500 kΩ (against V_{CC2})	—	—	0.1	V
	Band Width	f_B	—	Design assurance	—	800	—	kHz
Buffer Limiter Amp	Common-Phase Input Voltage Range	V_{CMRBL}	16		0	—	V_{CC2} −1.7	V
	Input Current	I_{BL}	17	V_{BL} = 0 V	—	—	1	μA
	Input Offset Voltage	V_{OFBL}	18	V_{RSB} = 1.5 V	—	0	±7	mV
Thermal Shutdown Circuit Operating Temperature		T_{SD}	—	Design assurance	—	150	—	°C

Note: Design target value is fixed at 0.5μA (Max.)

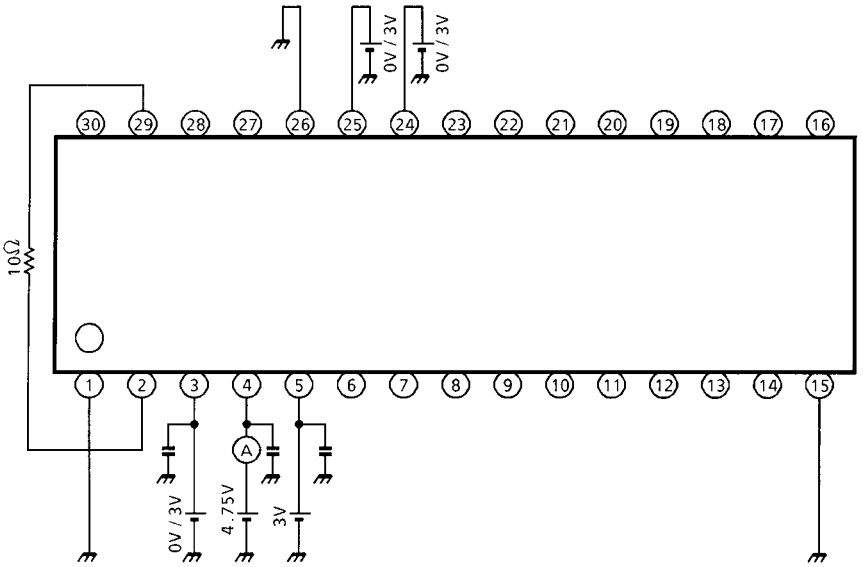
TEST CIRCUIT 1

1. I_{CC1}, I_{CC2}, I_{CC3}



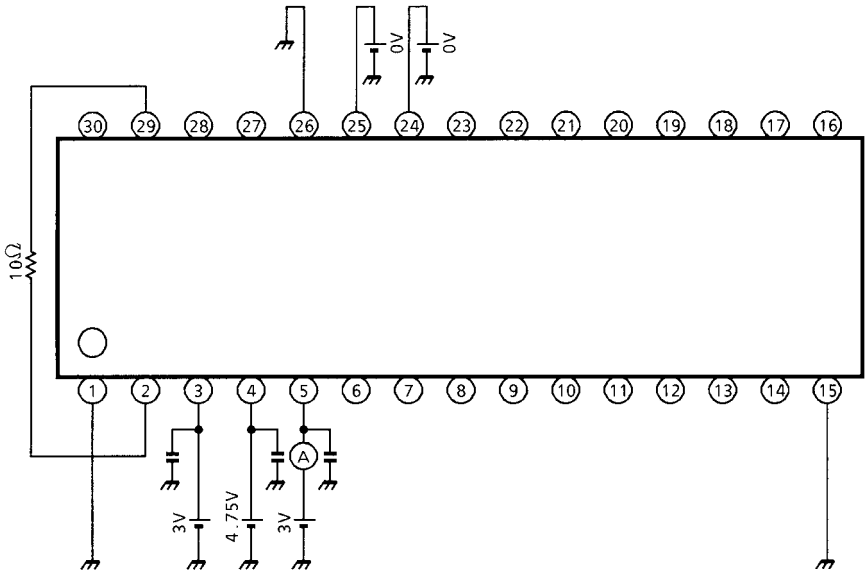
- I_{CC11}
  DEC1 = L, DEC2 = L
- I_{CC12}
  DEC1 = H, DEC2 = L
  and
  DEC1 = L, DEC2 = H
- I_{CC13}
  DEC1 = H, DEC2 = H

2. I_{CC21}, I_{CC22}, I_{CC23}, I_{CC24}



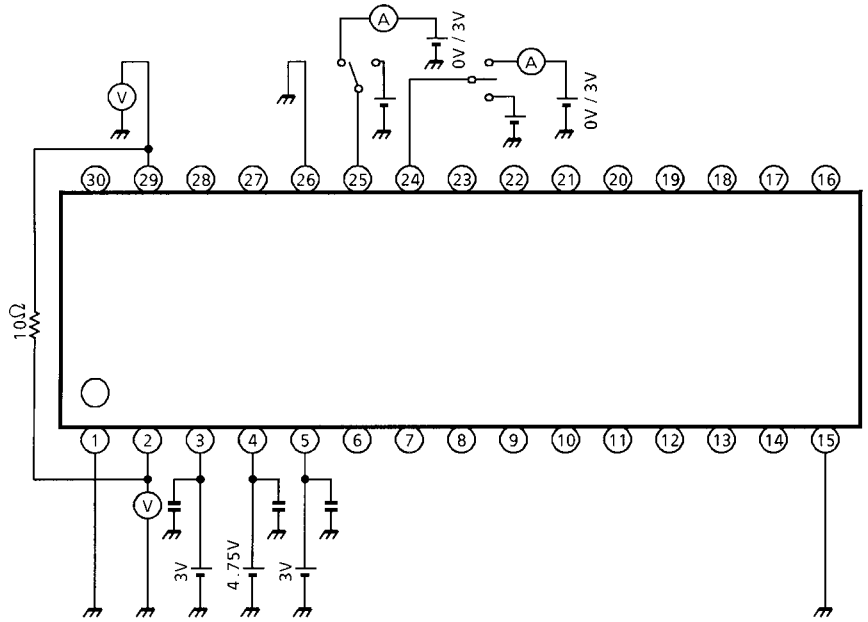
- I_{CC21}
  V_{CC1} = 0 , DEC1 = L,
  DEC2 = L
- I_{CC22}
  V_{CC1} = 3 V, DEC1 = L,
  DEC2 = L
- I_{CC23}
  DEC1 = H, DEC2 = L
  and
  DEC1 = L, DEC2 = H
- I_{CC24}
  DEC1 = H, DEC2 = H

3. I_M



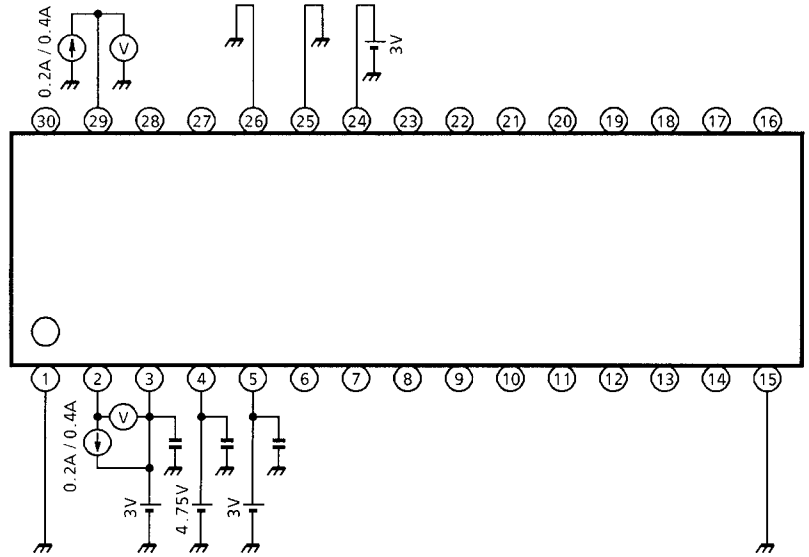
- I_M
  DEC1 = L, DEC2 = L

4. V_{IN1}, V_{IN2}, I_{IN1}, I_{INL}

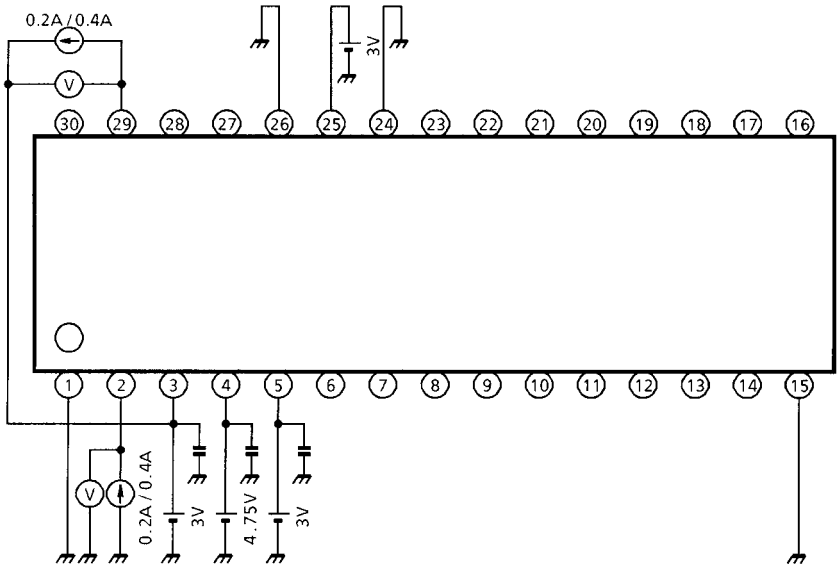


- V_{IN1}, V_{IN2}
  V_{DEC1} = 0.6 V, V_{DEC2} = 2.0 V
  V_{DEC1} = 2.0 V, V_{DEC2} = 0.6 V
  V_{DEC1} = 2.0 V, VD_{EC2} = 2.0 V
  Check the output functions on the above-mentioned three conditions.
- I_{IN1}
  V_{IN} = 3.0 V
- I_{INL}
  V_{IN} = 0 V

5. $V_{sat\ (H+L)}$



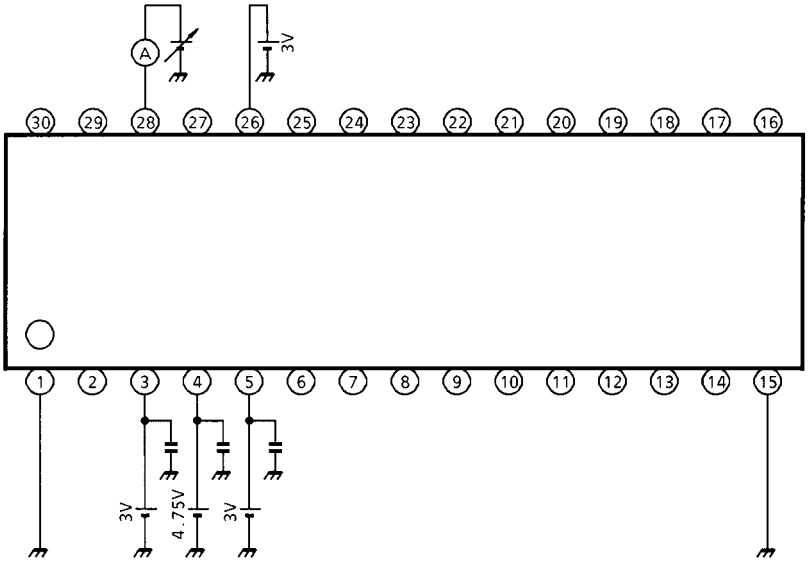
- $V_{sat\ (H+L)}$
  Input DEC1 = H, DEC2 = L, and measure OUT1 (upper side) and OUT2 (lower side) with regard to I_O = 0.2 A / 0.4 A.



- $V_{sat\ (H+L)}$
  Input DEC1 = H, DEC2 = L, and measure OUT1 (upper side) and OUT2 (lower side) with regard to I_O = 0.2 A / 0.4 A.

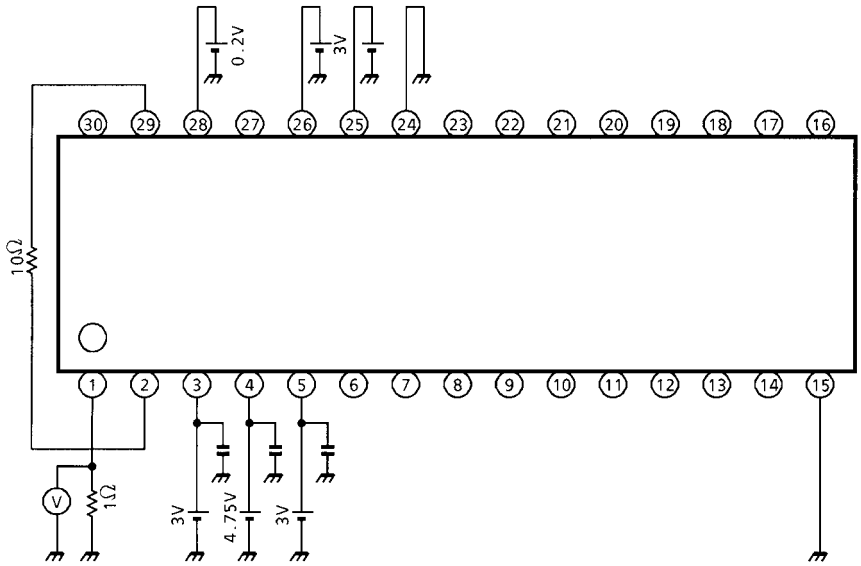
  The sum of the upper / lower values of OUT1 and OUT2 is fixed at $V_{sat\ (H+L)}$.

6. V_{RS}



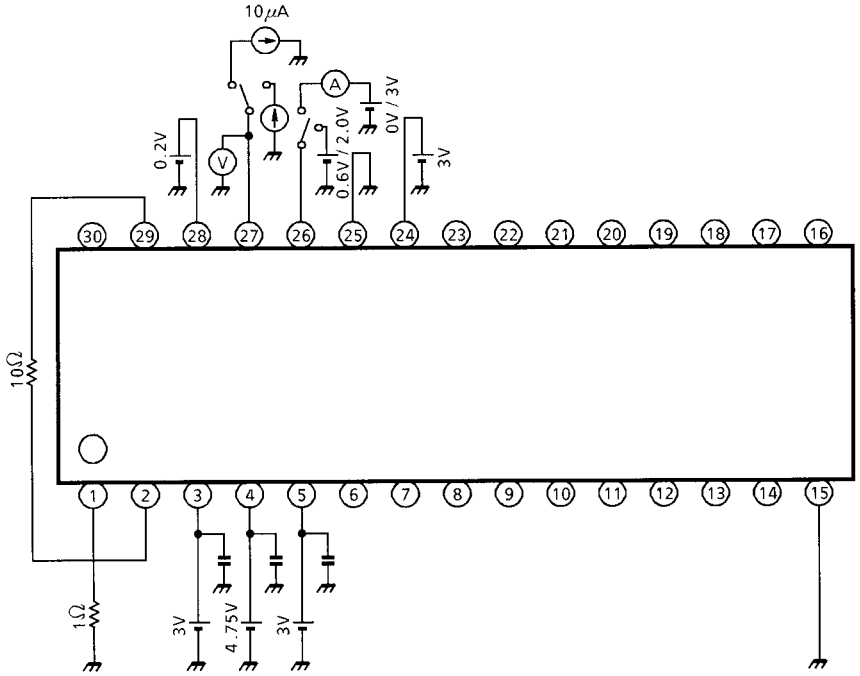
- V_{RS}
  Change V_{RS} and measure input current.

7. V_{LIMIT}



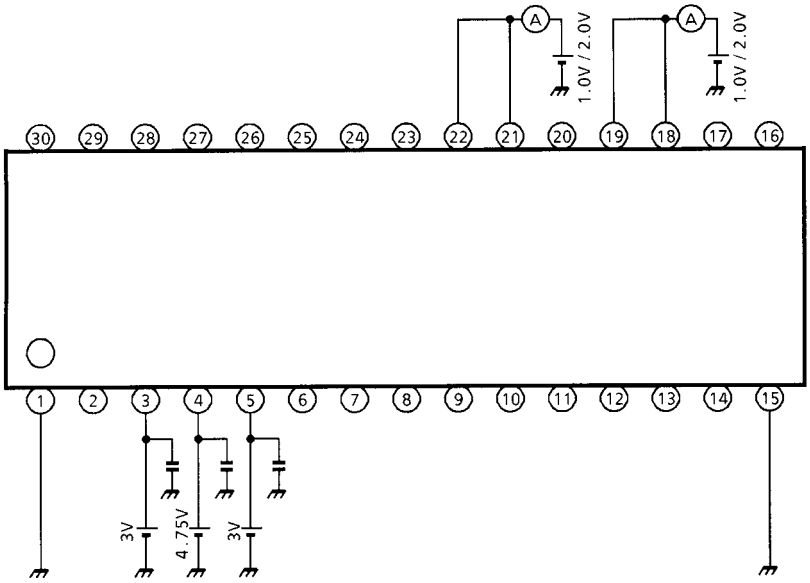
- V_{LIMIT}
  Input V_{RS} = 0.2 V and measure R_F (= 1Ω) generating voltage at the time of limiter amp operation.

8. $V_{LE\ (H)}$, $V_{LE\ (L)}$, I_{LC}, I_{LCL}, $V_{LO\ (H)}$, $V_{LO\ (L)}$

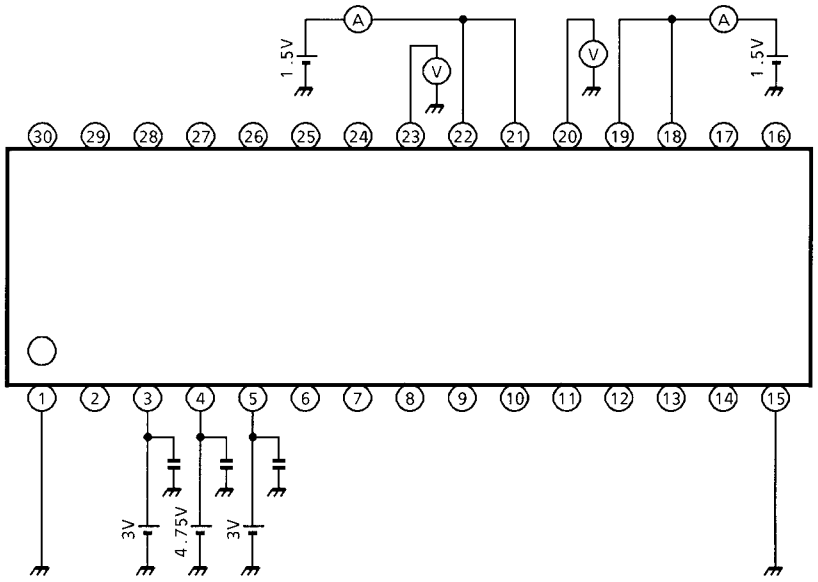


- $V_{LE\ (H)}$, $V_{LE\ (L)}$
  Input V_{LE} = 2.0 V / 0.6 V in a limiter amp operating state and check the LIMIT OUT terminal voltage.
- I_{LC}
  V_{LE} = 3.0 V
- I_{LCL}
  V_{LE} = 0 V
- $V_{LO\ (H)}$, $V_{LO\ (L)}$
  Input V_{LE} = 0.6 V / 2.0 V in a limiter amp operating state and measure the LIMIT OUT terminal voltage when I_O = 10 μA.

9. V_{CMRFG}



10. I_{FG}, V_{OFFG}



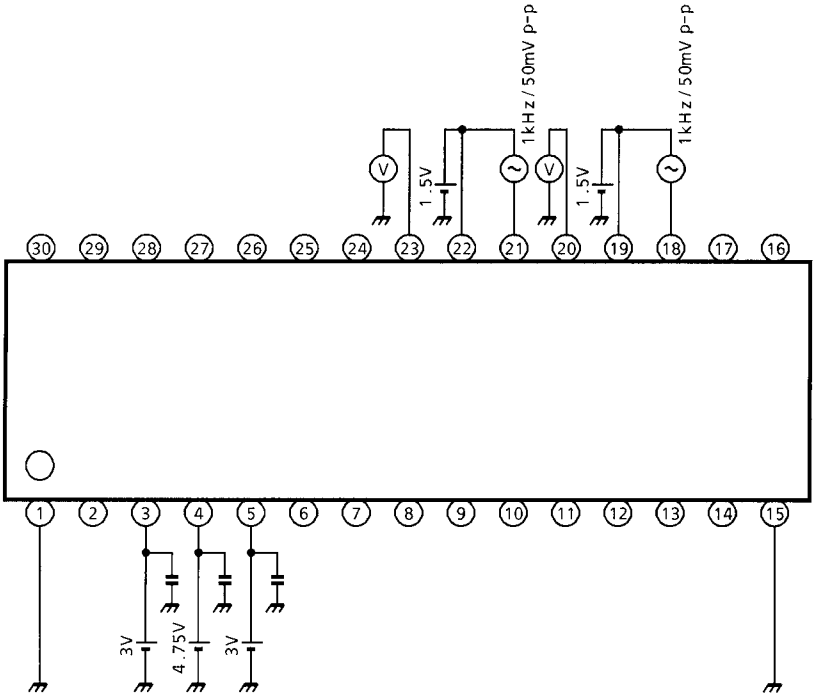
- I_{FG}
  Measure the input current (I_{FG}') when V_{CMRFG} = 1.5 V, and calculate the following formula:

  $$I_{FG} = \frac{1}{2} \times I_{FG}'$$

- V_{OFFG}
  Measure the R_{LO} pin output voltage when V_{CMRFG} = 1.5 V, and calculate the following formula :

  $$V_{OFFG} = V_{RLO} - 1.5$$

11. G_{VFG}

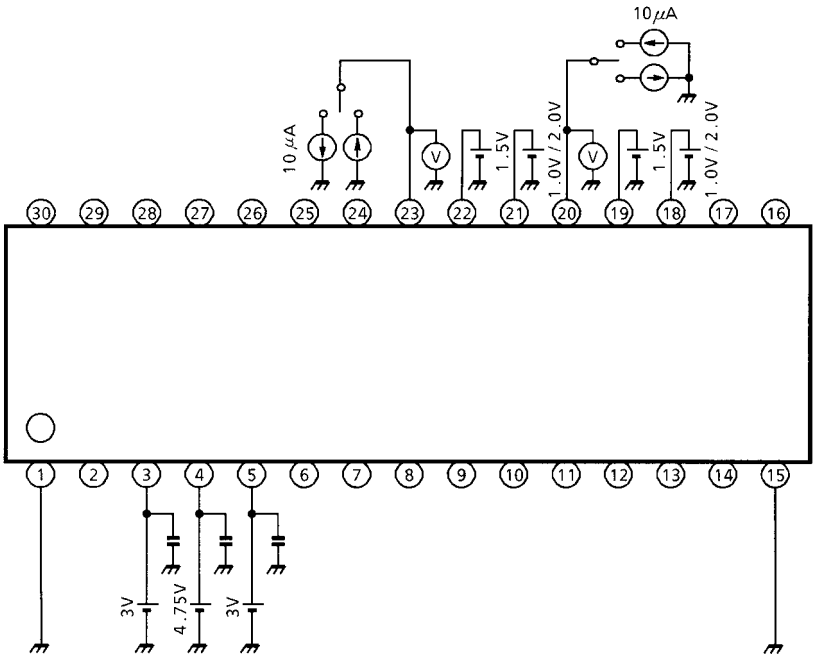


- G_{VFG}
  V_{RLP} = 1.5 V, input signals

  f_{FG} = 1 kHz, V_{FG} = 50 $mV_{p\text{-}p}$ between RLP and RLM, and measure V_{RLO} in this case.

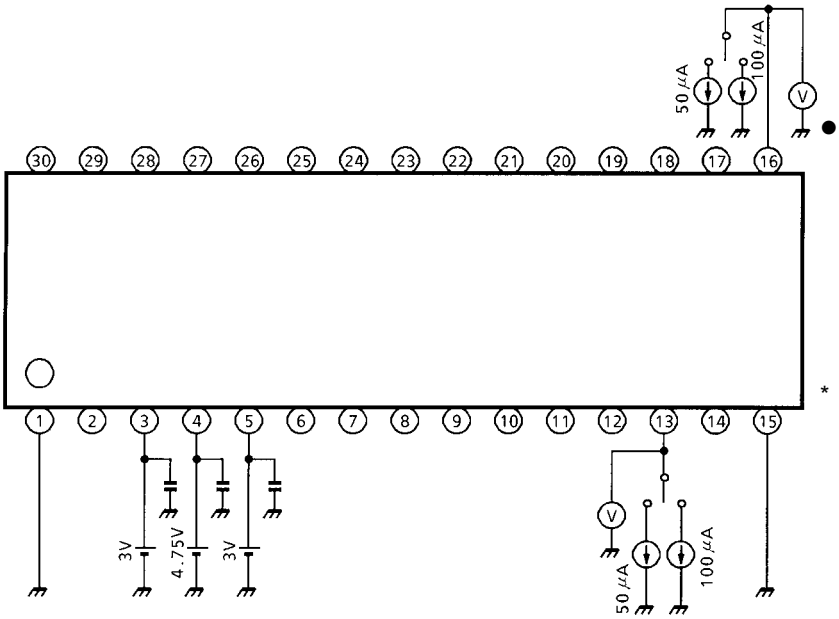
  $$GVFG = 20 \log \frac{V_{RLO}}{0.05} \text{ [dB]}$$

12. $V_{sat-FG\ (H)}$, $V_{sat-FG\ (L)}$



- $V_{sat-FG\ (H)}$
  Input V_{RLP} = 1.5 V, V_{RLM} = 1.0 V, measure the R_{LO} pin voltage when I_O = 10 μA (source current), and calculate the following formula:
  $V_{sat-FG\ (H)} = 3.0 - V_{RLO}$ [V]
- $V_{sat-FG\ (L)}$
  Input V_{RLP} = 1.5 V, V_{RLM} = 2.0 V and measure the R_{LO} pin voltage when I_O = 10 μA (sink current).

13. R_{IN}

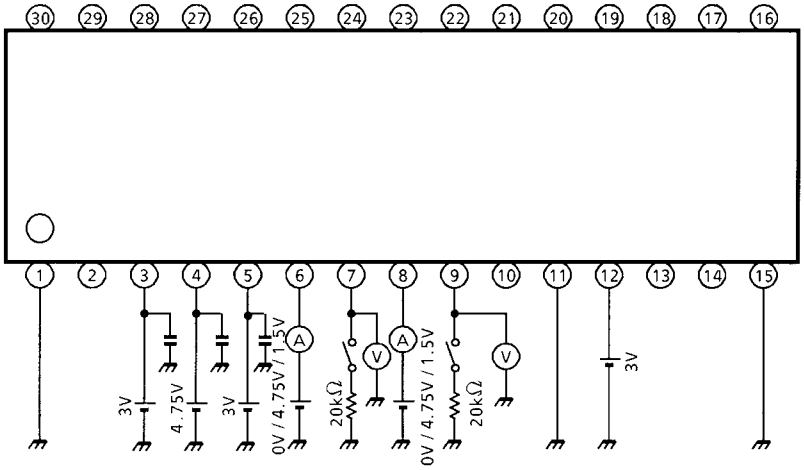


- R_{IN}
  Measure the V_{TOPIN}, V_{ENDIN} at the time 50 μA / 100 μA current flows from TOPIN / ENDIN pin, and calculate the following formula :

$$R_{IN} = \frac{V\,(50\,\mu A) - V\,(100\,\mu A) - 0.007}{50\,\mu A}\ [\Omega]$$

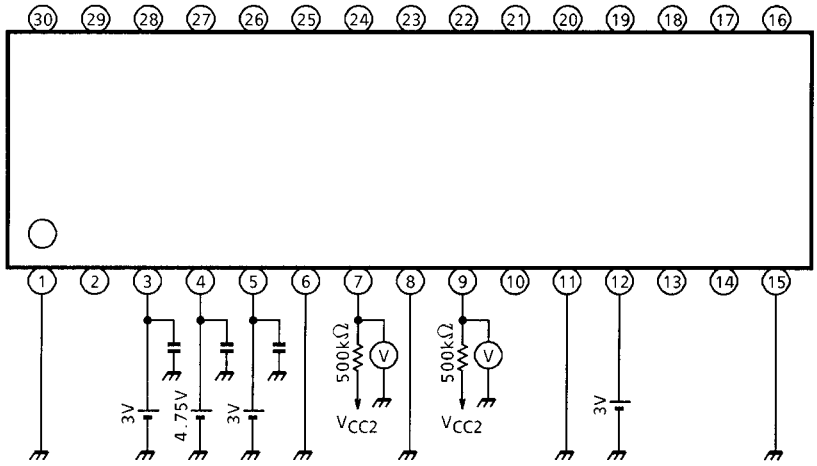
* The 7 mV in the formula represents the V_{BE} change of the internal Tr. at the time of 50 μA / 100 μA.

14. V_{CMRB}, I_B, $V_{OB\ (H)}$

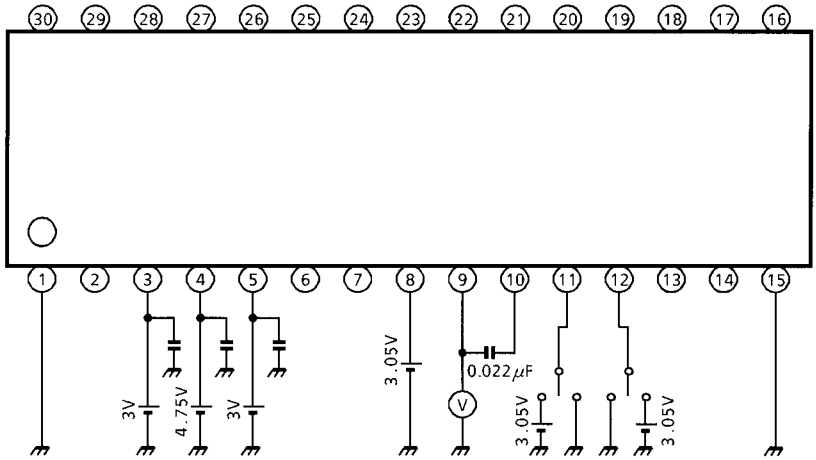


- V_{CMRB}
  Input V_{BIN} = 0 V / 4.75 V and measure BOUT pin voltage.
- I_B
  V_{BIN} = 1.5 V
- $V_{OB\ (H)}$
  Input V_{BIN} = 4.75 V and connect 20 kΩ (against GND) to BOUT pin.

15. $V_{OB\ (L)}$

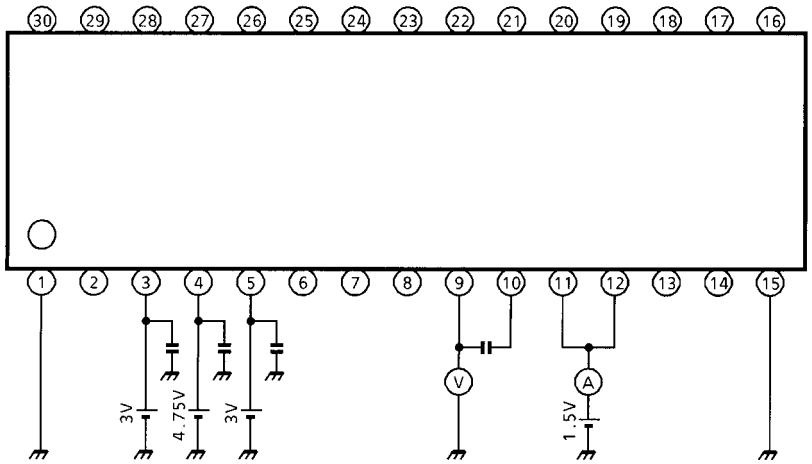


16. V_{CMRBL}

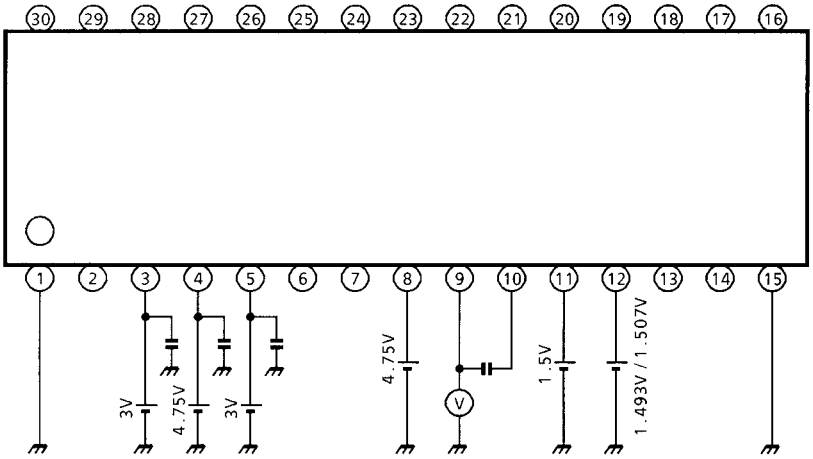


- V_{CMRBL}
  Check BOUT2 pin : L when
  V_{RFB} = 3.05 V, V_{RSB} = 0 V.
  Check BOUT2 pin : L when
  V_{RFB} = 0 V, V_{RSB} = 3.05.

17. I_{BL}



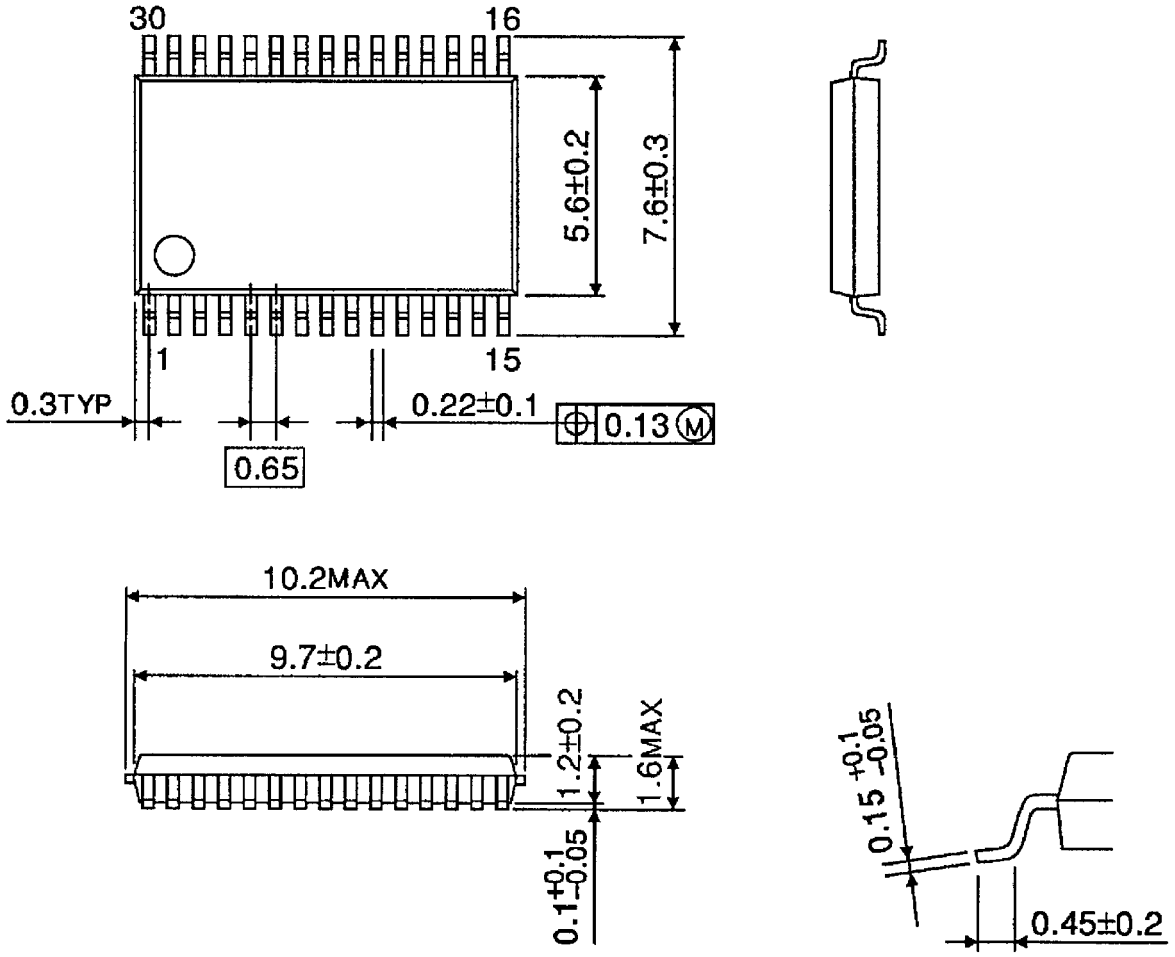
18. V_{OFBL}



- V_{OFBL}
  Input V_{RSB} = 1.5 V,
  V_{RFB} = 1.5 V ± 7 mV, and
  check the switching of BOUT2
  pin output function.
  BOUT2: H when
  V_{RFB} = 1.493 V.
  BOUT2: L when
  V_{RFB} = 1.507 V.

PACKAGE DIMENSIONS

SSOP30−P−300−0.65 Unit: mm



Weight: 0.17 g (Typ.)

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