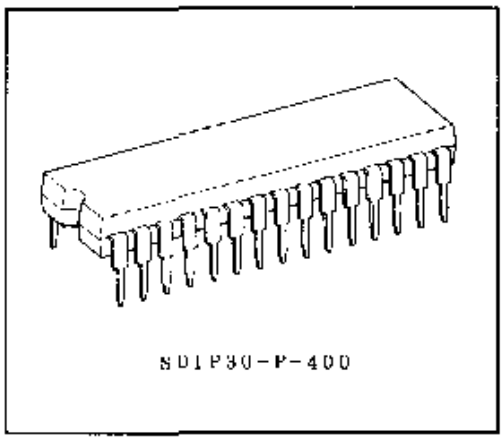
TA8718N

TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT
SILICON MONOLITHIC

TENTATIVE DATA

VIDEO-CHROMA-DEFLECTION SYSTEM FOR A COLOR TELEVISION (PAL).



SDIP30-P-400

Weight: 2.2g(Typ.)

The TA8718N combines a PAL video-chroma-deflection system in a 30-lead, shrink-type, dual-in-line plastic package.
A PAL system with using TA8718N needs minimal external parts and PCB area.
Lead-functions of the TA8718N are almost compatible with those of multi-standard video-chroma-deflection IC (TA8659AN). So, the PCB can be made so that both the TA8659AN for multi standard TV and the TA8718N for PAL only TV are able to use in a same board.

FUNCTIONS

Video Section

- Contrast control with uni-color control
- Brightness control
- Internal vertical blanking
- On-screen-display circuits (R,G,B)
- RGB primary color outputs
- ACL (Automatic Contrast Limitter)
- WPS (White Peak Slicer)

Chroma Section

- ACC circuit
- Color control/uni-color control
- Adjustment free APC

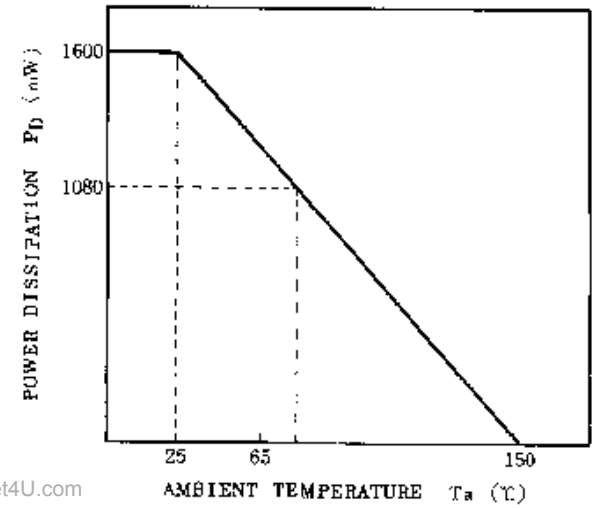
Deflection Section

- Adjustment free H/V oscillator by countdown system
- Vertical-ramp generator
- Picture phase adjustment
- 50Hz/60Hz Mode

MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{CC}	15	V
Power Dissipation	P_D	1600 (Note)	mW
Input Signal Amplitude	e_{In}	5	Vpp
Operating Temperature	T_{opr}	-10~65	°C
Storage Temperature	T_{stg}	-55~150	°C

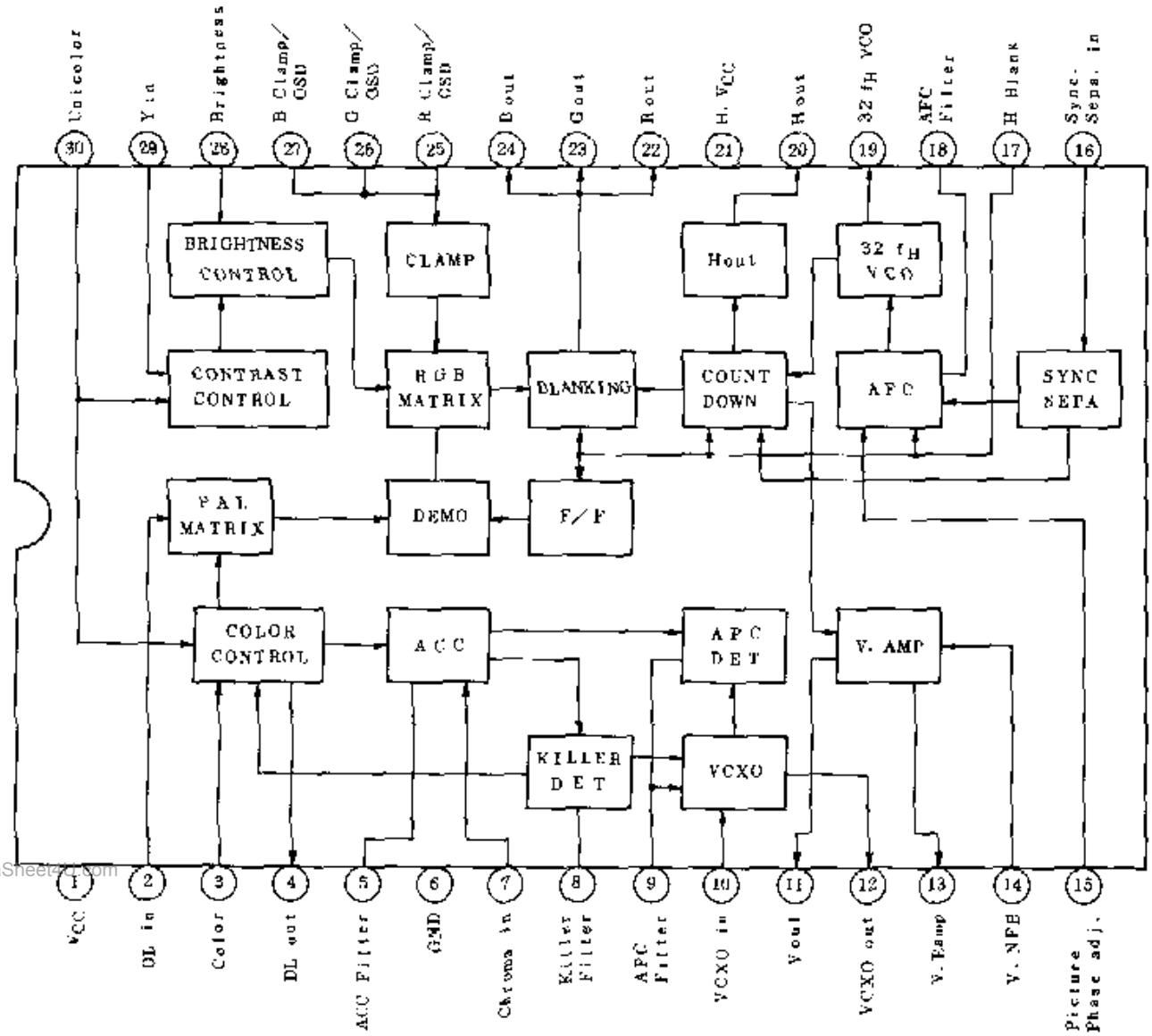
(Note) Derated above Ta=25°C in the proportion of 12.8mW/°C as shown below.



RECOMMENDED SUPPLY VOLTAGE

SUPPLY TERMINAL	SYMBOL	MIN.	TYP.	MAX.	UNIT
1	V_{CC}	10.8	12.0	13.2	V
21	11·V_{CC}	8.1	9.0	9.9	

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (Unless otherwise specified, V_{CC}=12V, H.V_{CC}=9V, Ta=25°C)

DC CHARACTERISTICS

PIN No.	TERMINAL	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
1	V_{CC}	V1	-	12	-	V	
2	DL in	V2	11.0	11.3	11.5		
3	Color	V3	-	-	-		
4	DL out	V4	6.2	6.4	7.2		
5	ACC Filter	V5	9.6	10.1	10.6		Terminal open
6	GND	V6	-	GND	-		
7	Chroma in	V7	3.2	3.7	4.2		No signal
8	Killer Filter	V8	5.2	5.7	6.2		No signal
9	APC Filter	V9	5.1	6.0	6.9		
10	VCXO in	V10	2.8	3.3	3.8		
11	V out	V11	3.0	3.7	4.5		
12	VCXO out	V12	7.8	8.8	9.9		
13	V.Ramp	V13	7.4	7.6	7.8		
14	V.NFB	V14	-	-	-		
15	Picture Phase Adj.	V15	4.1	4.5	4.9		
16	Sync. Sepa. in	V16	2.2	2.7	3.2		
17	FBP in	V17	-	-	-		
18	AFC Filter	V18	6.7	7.3	7.8		
19	32fH VCO	V19	5.3	6.0	6.3		
20	H out	V20	4.7	5.0	5.3		
21	H.V_{CC}	V21	-	9.0	-		
22	R out	V22	2.7	3.0	3.5		
23	G out	V23	2.7	3.0	3.5		#28: 3.1V
24	B out	V24	2.7	3.0	3.5		
25	R Clamp, R OSD in	V25	3.9	4.4	5.2		
26	G Clamp, G OSD in	V26	3.9	4.4	5.2		#28: 3.1V
27	B Clamp, B OSD in	V27	3.9	4.4	5.2		
28	Brightness	V28	-	-	-		
29	Y in	V29	2.8	3.1	3.5		
30	Unicolor	V30	-	-	-		

SUPPLY CURRENT

PIN No. : #

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
V_{CC}	I_{CC}	31.9	46.8	69.0	mA
H.V_{CC}	I_{CCH}	6.7	11.1	16.7	

AC CHARACTERISTICS

VIDEO STAGE

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Video Input Impedance	Zin29	Note 1	7.5	10	12.5	kΩ
Video Input Dynamic Range	VYi	Note 2	3.2	3.7	-	Vp-p
Linearity (lower side)	Vdo1	Note 3	0.1	0.4	0.7	V
Linearity (higher side)	Vdo2	Note 4	7.7	8.1	8.5	V
Video Gain	GY	Note 5	6.1	8.0	9.2	Times
Video Frequency Band Width	Gf	Note 6	1	0	-3	dB
Uni-Color Control DC Voltage Range	ΔV_{UY}	Note 7	1.0	1.5	2.0	V
Uni-Color Control Ratio	ΔG_{UY}	Note 8	19	20	21	dB
Uni-Color Center Voltage	V_{UYC}	Note 9	3.1	3.4	3.7	V
Brightness Control Sensitivity	GBR	Note 10	0.9	1.0	1.1	Times
Brightness Control Center Voltage	V#28	Note 11	2.8	3.1	3.4	V
ACL Sink Current	I_{ACL}	Note 12	1.0	1.5	2.0	mA
ACL Starting Level	VPL	Note 13	7.3	7.5	7.7	V
White Peak Slice Level	VPS	Note 14	7.9	8.1	8.3	V
V-BLK Output Level	VVR VVG VVB	Note 15	1.0	1.5	2.0	V
H-BLK Output Level	VHR VHG VHB	Note 16	1.0	1.5	2.0	V
DC Restoration Ratio	η_{DC}	Note 17	95	98	100	%
Output Sink Current	Iout	Note 18	1.4	2.0	2.6	mA
Video Mute SW Threshold Level	V#28M	Note 19	0.2	0.4	0.7	V
Video Mute Output Level	V#22M V#23M V#24M	Note 20	3.0	3.2	3.4	V
Service Output Level	V#22S V#23S V#24S	Note 21	3.0	3.2	3.4	V
Clamp Terminal Voltage	Vclmp	Note 22	3.9	4.4	4.9	V

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
OSD Threshold (H)	V_{OHON}	Note 23	6.1	6.6	7.1	V
OSD Threshold (L)	V_{OLON}		6.1	6.6	7.1	V
OSD Output Level (H)	V_{OSDH}		7.3	7.5	7.7	V
OSD Output Level (L)	V_{OSDL}		2.2	2.5	2.8	V
OSD Output H Level Rise Time	τ_{RHi}	Note 24	-	10	100	nsec
OSD Output H Level Fall Time	τ_{FHi}		-	30	100	
OSD Output L Level Fall Time	τ_{RLo}		-	25	100	
OSD Output L Level Rise Time	τ_{FLo}		-	15	100	
OSD Output H Level Rise Delay Time	t_{PRHi}		-	0	±45	
OSD Output H Level Fall Delay Time	t_{PFHi}		-	45	100	
OSD Output L Level Fall Delay Time	t_{PRLo}		-	35	100	
OSD Output L Level Rise Delay Time	t_{PFLo}		-	25	100	
Blanking Pulse ON Level	V_{BPON}	Note 25	0.75	1.25	1.75	V
Blanking Pulse Delay Time	t_{BPON}	Note 26	-	0.35	0.5	μsec
	t_{BPOF}		-	0.7	0.9	

CHROMA STAGE

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Delay Line Drive Chroma Level	v_{4C1}	Note 27	0.85	1.2	1.7	Vp-p
	v_{4C2}		1.7	2.4	3.4	
ACC Characteristic	e_a	Note 28	0.2	0.5	-	Vp-p
	A		0.9	1.0	1.3	Times
Delay Line Amp. Characteristic	v_{2C}	Note 29	0.11	0.16	0.25	mVp-p
	v_{4C}		0.85	1.2	1.7	Vp-p
	G_{DL}		14	17.5	21	dB
50Hz/60Hz Switching Threshold	V2 60	Note 30	8.5	9.5	10.5	V
Color Control Characteristic	V3	Note 31	2.7	3.1	3.5	V
	$\Delta V3$		0.6	1.3	1.9	

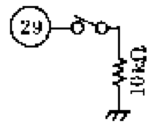
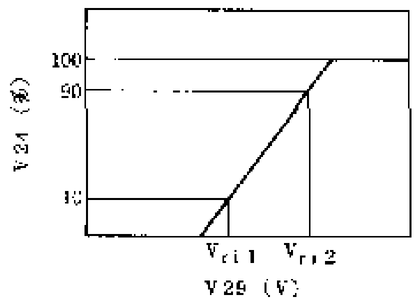
CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Uni-Color Control Characteristic	e_U	Note 32	18	20	22	dB
	V30		2.7	3.1	3.5	V
	ΔV30		0.6	1.3	1.9	
Killer Threshold	e_{hCol}	Note 33	0.6	2.5	4.3	mVp-p
	$e_{hB/W}$		0.6	1.0	1.7	
Killer Ident Threshold	$V_{8B/W}$	Note 34	-	6.0	-	V
	V_{8S}		-	6.4	-	
	V_{8C}		-	6.4	-	
	ΔV8		0.2	0.4	-	
APC Pull-in/Hold Range	f_{12P}	Note 35	±250	±500	±1000	Hz
	f_{12H}		±250	±500	±1000	
Subcarrier Frequency Control Sensitivity	β	Note 36	1.5	2.75	4.0	Hz/mV
APC Sweeping Period-1	S_{V1}	Note 37	6.3	6.7	7.1	V
	S_{V2}		5.3	5.7	6.0	
	S_{V3}		0.7	1.0	1.3	
APC Sweeping Period-2	t1	Note 38	4	12	20	msec
	t2		35	70	115	
	t3		39	82	135	
Color Differential Signal Output Level	v_{22R}	Note 39	2.4	3.5	5.0	Vp-p
	v_{23G}		1.5	2.1	3.1	
	v_{24B}		4.4	6.3	8.9	
Relative Ratio	$v_{R/B}$	Note 40	0.43	0.56	0.69	Times
	$v_{G/B}$		0.27	0.34	0.41	
Relative Phase	θ_{R-B}	Note 40	80	90	95	deg
	θ_{G-B}		221	236	246	
Residual Carrier	v_{RSC}	Note 41	-	-	30	mVp-p
	v_{GSC}		-	-	20	
	v_{BSC}		-	-	50	
Output Harmonics	v_{RHC}	Note 42	-	-	100	mVp-p
	v_{GHC}		-	-	50	
	v_{BHC}		-	-	100	

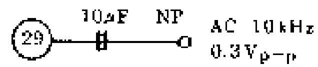
DEFLECTION STAGE

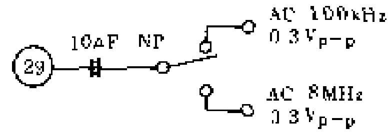
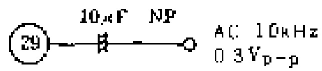
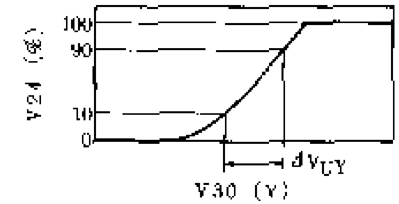
CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Sync. Sepa. Input Current Sensitivity	I_{IN16}	Note 43	15	25	40	μA
H.AFC Phase Detector Current	I_{DET}	Note 44	490	600	760	μA
H.AFC Masking Period	T_{CO18}	Note 45	-	309~6	-	H
32fH VCO Starting Voltage	V_{ON}	Note 46	4.4	4.6	4.8	V
H. Output Starting Voltage	V_{ON20}	Note 47	4.7	5.2	5.7	V
Horizontal Free-running Frequency	f_0	Note 48	15.475	15.625	15.775	kHz
Horizontal Frequency Control Range	f_{max}	Note 49	16.400	16.700	16.900	kHz
	f_{min}		14.700	15.000	15.200	
Horizontal Frequency Control Sensitivity	β_H	Note 50	2.2	2.5	2.8	kHz/V
H.Output Duty Cycle	T20	Note 51	41	43	45	%
H.Output Level	V_{H20}	Note 52	4.7	5.0	5.3	V
	V_{L20}		-	0	100	mV
Horizontal Phase Adjustment Range	$\Delta G15$	Note 53	2.6	2.8	3.0	μsec
Horizontal Phase Shift With 50/60 Switching	G17	Note 54	1.5	1.6	1.7	μsec
Vertical Retrace Pulse Period	T_{r1}	Note 55	-	10	-	H
	T_{r2}		-	10	-	
Peak Voltage of Ramp Wave	V_{H13}	Note 56	7.4	7.6	7.8	V
Ramp Output Current	I_{o13}	Note 57	-	28	-	mA
Vertical Amplifier Gain	G_V	Note 58	18	20	22	dB
Vertical Output Maximum Voltage	V_{H11}	Note 59	3.0	3.7	4.5	V
Vertical Output Minimum Voltage	V_{L11}	Note 60	-	0	0.3	V
Vertical Output Current	I_{o11}	Note 61	20	35	-	mA
Vertical Pull in Range	f_{PV1}	Note 62	-	268.5	-	H
	f_{PV2}		-	352.5	-	
	f_{PV3}	Note 63	-	232.5	-	
	f_{PV4}		-	288.5	-	

ELECTRICAL CHARACTERISTICS TEST CONDITION

Video Stage: Test Circuit 1

NOTE	CHARACTERISTIC	SYMBOL	TEST CONDITION					TEST METHOD
			Unicolor	Color	Bright	SW29	SW30	
1	Video Input Impedance	Z_{in29}	Min.	Min.	Center	c	a	 Measure DC voltage at #29. SW off: V#29A SW on : V#29B $Z_{in} = \left(\frac{V\#29A}{V\#29B} - 1\right) \times 10^{4}\,\Omega$
2	Video Input Dynamic Range	V_{Yi}	Min.	Min.	Adj.	c	a	(1) Adjust Brightness Control to set #24 voltage to be 3.0V during trace period. (2) Measure #27 voltage, and apply that voltage to #27 with external power supply. (3) Vary DC voltage at #29, and measure voltage at #24. (4) $V_{Yi} = V_{ri2} - V_{ri1}$ 

<table>
<tr><th rowspan="2">NOTE</th><th rowspan="2">CHARACTERISTIC</th><th rowspan="2">SYMBOL</th><th colspan="5">TEST CONDITION</th><th rowspan="2">TEST METHOD</th></tr>
<tr><th>Unicolor</th><th>Color</th><th>Bright</th><th>SW29</th><th>SW30</th></tr>
<tr><td>3</td><td>Linearity
(Lower side)</td><td>V_{do1}</td><td rowspan="2"></td><td rowspan="2">Min.</td><td rowspan="2">Adj.</td><td rowspan="2">c</td><td rowspan="2">b</td><td rowspan="2">(1) Adjust Brightness Control to set #24 voltage to be 3.0V during trace period.
(2) Measure #27 voltage, and apply that voltage to #27 with external power supply.
(3) Apply DC 7V to #30.
(4) Vary DC voltage at #29, and measure minimum and maximum voltage at #24.
(5) Measure the voltage of Red and Green output in the same way as Blue.</td></tr>
<tr><td>4</td><td>Linearity
(Higher side)</td><td>V_{do2}</td></tr>
<tr><td>5</td><td>Video Gain</td><td>GY</td><td>Max.</td><td>Min.</td><td>ADj.</td><td>a</td><td>a</td><td> 
(1) Adjust Brightness Control to set #24 voltage to be 3.0V during trace period.
(2) Measure AC level at #24. $v_{\#24}$
(3) $GY = v_{\#24}/0.3$
(4) Measure the voltages of Red and Green output in the same way as Blue.</td></tr>
</table>

NOTE	CHARACTERISTIC	SYMBOL	TEST CONDITION					TEST METHOD
			Unicolor	Color	Bright	SW29	SW30	
6	Video Frequency Band Width	Gf	Max.	Min.	Adj.	a	a	 (1) Adjust Brightness Control to set #24 voltage to be 3.0V during trace period. (2) Measure AC level at #24. (3) $G_f = 20\log \frac{v_{\#24}^{8MHz}}{v_{\#24}^{100kHz}}$ [dB] (4) Measure the voltages of Red and Green output in the same way as Blue.
7	Uni-Color Control DC Voltage Range	ΔV_{UY}	Adj.	Min.	Adj.	a	a	 (1) Adjust Brightness Control to set #24 voltage to be 3.0V during trace priode. (2) Vary DC voltage at #30, and Masure AC level at #24. 

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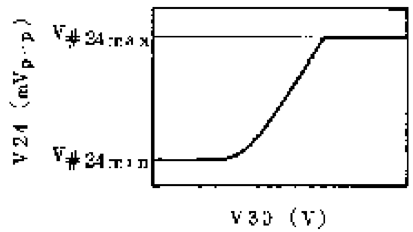
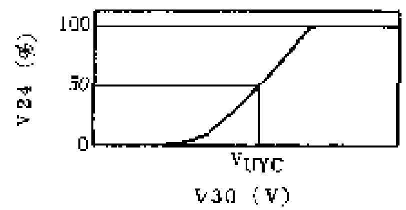
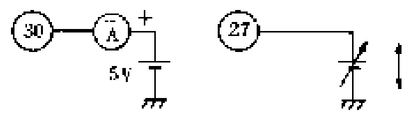
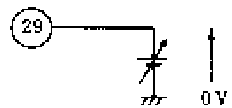
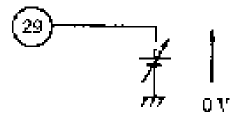
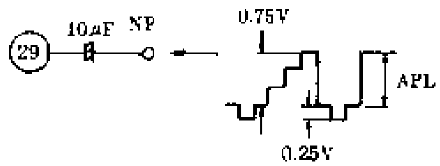
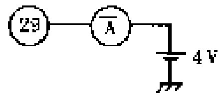
NOTE	CHARACTERISTIC	SYMBOL	TEST CONDITION					TEST METHOD
			Unicolor	Color	Bright	SW29	SW30	
8	Uni-Color Control Range	ΔG_{UY}	Adj.	Min.	Adj.	a	a	(1) The same as the Note 7. (2) $\Delta G_{UY}=20\log(V_{\#24max}/V_{\#24min})$ [dB] 
9	Uni-Color Center Voltage	V_{UYC}	Adj.	Min.	Adj.	a	a	The same as the Note 7. 
10	Brightness Control Sensitivity	G_{BR}	Max.	Min.	Adj.	c	a	(1) Adjust Brightness Control to set #24 voltage to be 3.0V during trace period. (2) Increase voltage at #28 by +1.0V. (3) Measure voltage at #24 during the trace period, V#24. (4) $G_{BR}=(V_{\#24}-3.0)/1.0$

NOTE	CHARACTERISTIC	SYMBOL	TEST CONDITION					TEST METHOD
			Unicolor	Color	Bright	SW29	SW30	
11	Brightness Control Center Voltage	V#28	Max.	Min.	Adj.	c	a	(1) Adjust Brightness Control to set #24 voltage to be 3.0V during trace period. (2) Measure voltage at #28.
12	ACL Sink Current	IACL	5V	Min.	Adj.	c	b	 When voltage at #24 is same as the slice Level, measure input current at #30.
13	ACL Starting Level	VPL	Max.	Max.	Adj.	c	a	 (1) Adjust Brightness Control to set #24 voltage to be 3.0V during trace period. (2) Measure #27 voltage, and apply that voltage to #27 with external power supply. (3) Measure voltage at #24 during trace period when DC voltage at #30 varries.

1A1S:2

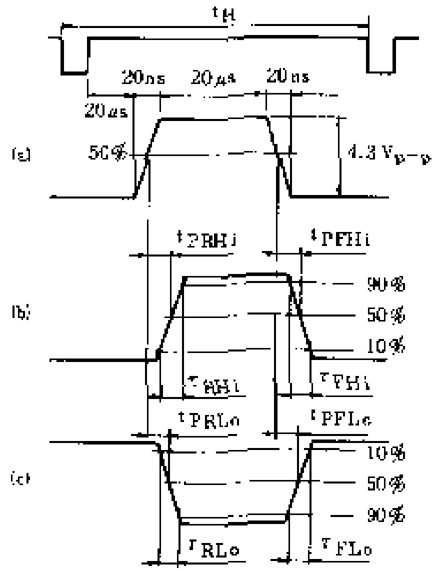
NOTE	CHARACTERISTIC	SYMBOL	TEST CONDITION					TEST METHOD
			Unicolor	Color	Bright	SW29	SW30	
14	White Peak Slice Level	V_{PS}	7V	Max.	Adj.	c	b	 (1) Adjust Brightness Control to set #24 voltage to be 3.0V during trace period. (2) Measure #27 voltage, and apply that voltage to #27 with external power supply. (3) Measure voltage at #24 during trace period it's clipped.
15	V-BLK Output Level	V_{VR} V_{VG} V_{VB}	Max.	Max.	Adj.	c	a	Measure V-BLK pulse levels of #22, #23 and #24.
16	H-BLK Output Level	V_{HR} V_{HG} V_{HB}	Max.	Max.	Adj.	c	a	Measure H-BLK pulse levels of #22, #23 and #24.

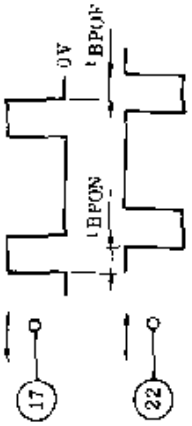
NOTE	CHARACTERISTIC	SYMBOL	TEST CONDITION					TEST METHOD
			Unicolor	Color	Bright	SW29	SW30	
17	DC Restoration Ratio	T_{DC}	Adj.	Min.	Adj.	a	a	 (1) Adjust Brightness Control to set #24 voltage to be 3.0V during trace period when no signal inputs. (2) Adjust Uni-color control to set #24 AC amplitude during trace period to be 1.25Vp-p. (3) APL: 10%~90% Measure pedestal level change. ΔVp (4) $T_{DC}=(1-\Delta Vp)\times 100$ (%)
18	Output Sink Current	Iout	Min.	Min.	Adj.	c	a	 (1) Adjust Brightness Control to set #24 voltage to be 3.0V during trace period. (2) Measure input current at #24. (3) Measure the current of Red and Green outputs in the same way as Blue.

NOTE	CHARACTERISTIC	SYMBOL	TEST CONDITION					TEST METHOD
			Unicolor	Color	Bright	SW29	SW30	
19	Video Mute SW Threshold Level	V#28M	Max.	Max.	Adj.	c	a	 (1) Adjust Brightness Control to set #24 voltage to be 3.0V during trace period. (2) Reduce the applied voltage at #28 and measure the voltage when #3 voltage varies.
20	Video Mute Output Level	V#22M V#23M V#24M	Max.	Max.	GND	c	a	Measure voltage at #22, #23 and #24 during trace period, connecting the terminal 28 to GND (Video Mute condition).
21	Service Output Level	V#22S V#23S V#24S	Max.	Max.	Adj.	c	a	(1) Adjust Brightness Coltrol to set #24 voltage to be 3.0V during trace period. (2) Apply DC 9V to #11. (3) Measure voltage at #22, #23, and #24 during the period.
22	Clamp Terminal Voltage	Vclamp	Max.	-	Adj.	c	a	(1) Adjust Brightness Control to set #24 voltage to be 3.0V during trace period. (2) Measure DC voltage at #25, #26 and #27.

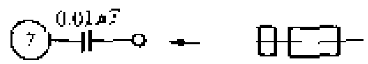
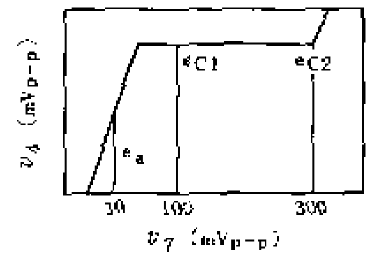
NOTE	CHARACTERISTIC	SYMBOL	TEST CONDITION						TEST METHOD
			Unicolor	Bright	SW29	SW25	SW26	SW27	
23	OSD Threshold (H)	V_{OHON}	Max.	Adj.	c	b	b	b	(1) Adjust Brightness Control to set #22 voltage to be 5V during trace period. (2) Measure #25 DC voltage, and apply that voltage to #25 with external power supply. (3) Increase the voltage. (4) Measure voltage at #25 (V_{OHON}) and #22 (V_{OSDH}) during trace period when voltage at #22 is clamped on ACL level. (5) Measure voltages at #25 (V_{OLON}) and #23 (V_{OSDL}) during trace period when voltage at #23 is clamped lower than black level. (6) Measure the voltage of #26 and #27 in the same way.
	OSD Threshold (L)	V_{OLON}							
	OSD Output (H)	V_{OSDH}							
	OSD Output (L)	V_{OSDL}							

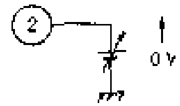
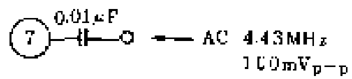
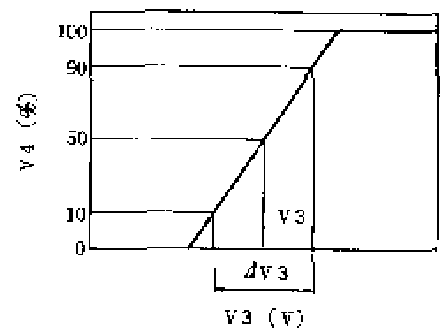
NOTE	CHARACTERISTIC	SYMBOL	TEST CONDITION Unicolor	Color	Bright	SW25	SW26	SW27	TEST METHOD
24	OSD Output H Rise Time	τ_{RHi}	Ma.	Adj.	c	a or b	a or b	a or b	(1) Adjust Brightness Control to set #22 voltage to be 5V during trace period. (2) Apply (a) signal to #25. (3) Measure τ_{RHi}, t_{PRHi}, τ_{FHi} and t_{PFHi} as (b) at #22. (4) Measure τ_{RLo}, t_{PRLo}, τ_{FLo} and t_{PFLo} as (c) at #23 or #24. (5) Measure the same periods of #23 and #24 as #22.
	OSD Output H Fall Time	τ_{FHi}							
	OSD Output L Rise Time	τ_{RLo}							
	OSD Output L Fall Time	τ_{FLo}							
	OSD Output H Rise Delay Time	t_{PRHi}							
	OSD Output H Fall Delay Time	t_{PFHi}							
	OSD Output L Rise Delay Time	t_{PRLo}							
	OSD Output L Fall Delay Time	t_{PFLo}							



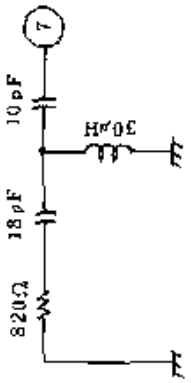
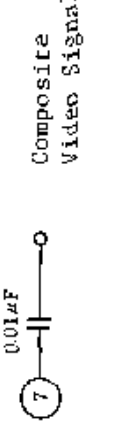
NOTE	CHARACTERISTIC	SYMBOL	TEST CONDITION					TEST METHOD
			Unicolor	Color	Bright	SW29	SW30	
25	Blanking Pulse ON Level	V_{BPON}			3V	c	a	(1) Apply blanking pulses and increase the amplitude from 0Vp-p. (2) Measure the amplitude when blanking output come out at #22. (3) Measure t_{BPON} and t_{BPOF} as the figure.
26	Blanking Pulse Delay Time	t_{BPON}	Max.	Max.				
		t_{BPOF}						

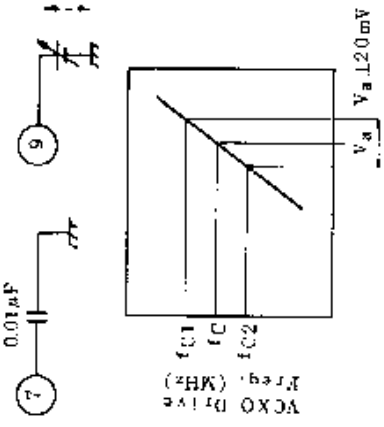
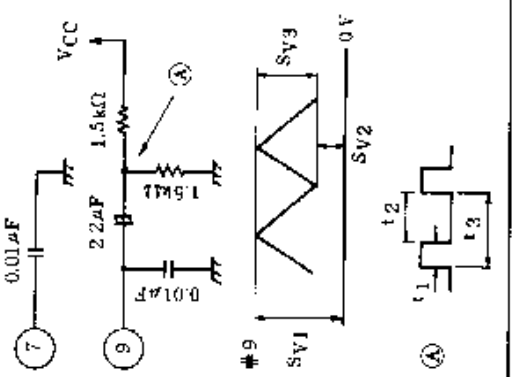
Chroma Stage: Test Circuit 2 (Adjust external components around DL with Philips color pattern.)

NOTE	CHARACTERISTIC	SYMBOL	TEST CONDITION								TEST METHOD
			SW2	SW7a	SW7b	SW7c	SW8	SW9	Color	Contrast	
27	Delay Line Drive Chroma Level	v_{4C1} v_{4C2}	OFF	a	ON	a	d	OFF	Max.	Min.	 burst : chroma = 1 : 1, 1 : 2 burst 100mVp-p Measure AC level at #4.
28	ACC Characteristics	e_a A	OFF	a	ON	a	d	OFF	Max.	Min.	 burst : chroma = 1 : 1 burst 10mVp-p, 100mVp-p, 300mVp-p (1) Measure AC level at #4.  (2) $A = \frac{e_{C2}}{e_{C1}}$

NOTE	CHARACTERISTIC	SYMBOL	TEST CONDITION								TEST METHOD
			SW2	SW7a	SW7b	SW7c	SW8	SW9	Color	Contrast	
29	Delay Line Amp. Characteristic	v_{2C}, v_{4C}, G_{DL}	a	a	ON	a		OFF	Max.	Max.	(1) Input "10" color bar signal of 3.58MHz/4.43MHz. (2) Measure AC levels at #2 and #4. (3) $G_{DL}=20\ell og \frac{v_{4C}}{v_{2C}}$
30	50/60Hz SW Threshold	V2 60	b	b	OFF	b	d	OFF	Max.	Min.	 Apply DC voltage at #2 from 0V to 9V. Monitor the output pulse frequency at #13.
31	Color Control Chracteristics	V3, ΔV3	OFF	a	ON	a	a	OFF	Adj.	Adj.	 (1) Sync. sepa. In, FBP in: no signal (2) Vary DC voltage at #3, and measure AC level at #4. 

NOTE	CHARACTERISTIC	SYMBOL	TEST CONDITION							TEST METHOD
			SW2	SW7a	SW7b	SW7c	SW8	SW9	Color	Contrast	
32	Uni-Color Control Characteristics	e_u	OFF	a	ON	a	a	OFF	Adj.	Adj.	(1) Sync. Sepa. in FBP in (2) Vary DC voltage at #30, and measure AC level at #4.
		V30									
		ΔV30									
33	Killer Threshold	e_{bcol}	OFF	a	ON	a	d	OFF	Max.	Max.	ebcol : B/W → Color ebB/W : Color → B/W
		$e_{bB/W}$									

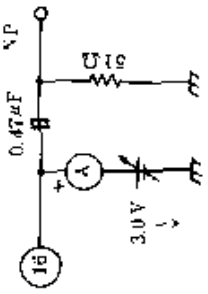
NOTE	CHARACTERISTIC	SYMBOL	TEST CONDITION							TEST METHOD
			SW2	SW7a	SW7b	SW7c	SW8	SW9	Color Contrast	
34	Killer Ident Threshold	V8B/W								 (1) Measure voltage at #8 with a high-impedance meter. V8B/W (2) Apply and vary voltage to #8, and measure the voltage when VCXO sweep starts. V8S (3) Measure the voltage at #8 when color terminal change high. (4) ΔV8=V8C-V8B/W
		V8S								
		V8C	OFF	b	OFF	b	c	OFF		
		ΔV8								
35	Pull-in/Hold Range	f12P	OFF	a	ON	a	d	OFF		 Measure pull-in and hold frequencies.
		f12H								

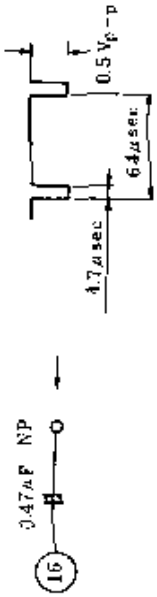
NOTE	CHARACTERISTIC	SYMBOL	TEST CONDITION							TEST METHOD
			SW2	SW7a	SW7b	SW7c	SW8	SW9	Color Contrast	
36	Subcarrier Frequency Control Sensitivity	β	OFF	b	OFF	b	d	ON		 $\beta = \frac{fC1-fC2}{40}$ fC=4.433618(MHz)
37	AFC Sweeping Period-1	Sv1	OFF	b	OFF	b	d	OFF		
		Sv2								
		Sv3								
38	AFC Sweeping Period-2	t1								
		t2								
		t3								

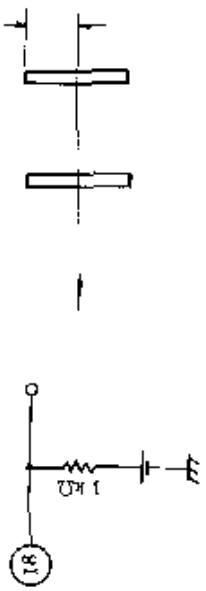
NOTE	CHARACTERISTIC	SYMBOL	TEST CONDITION								TEST METHOD
			SW2	SW7a	SW7b	SW7c	SW8	SW9	Color	Contrast	
39	Color Differential Signal Output Level	v_{22R}, v_{23G}, v_{24B}	OFF	a	ON	a	d	OFF	Max.	Max.	Input "10" color bar signal and measure R, G and B output levels.
40	Relative Ratio	$v_{R/B}$, $v_{G/B}$	OFF	a	ON	a	d	OFF			$v_{R/B} = \frac{v_{22R}}{v_{24B}}$, $v_{G/B} = \frac{v_{22G}}{v_{24B}}$
	Relative Phase	v_{R-B}, v_{G-B}	OFF	a	ON	a	d	OFF			Input "10" color bar signal and measure phase differences of R, G and B.
41	Residual Carrier	v_{RSC}, v_{GSC}, v_{BSC}	OFF	a → b	ON → OFF	a → b	d → b	OFF			(1) Yin, Chroma In : no signal (2) Measure residual carrier of R, G and B outputs.
42	Output Harmonics	v_{RHC}, v_{GHC}, v_{BHC}	OFF	a	ON	a	d	OFF	Adj.	Adj.	(1) Input "10" color bar signal. (2) Adjust Color and Contrast controls to set B-Y output to be 2Vp-p. (3) Measure output harmonics of B-Y, R-Y and G-Y

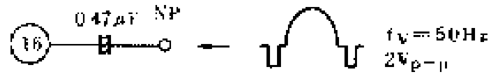
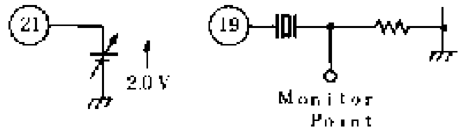
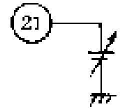
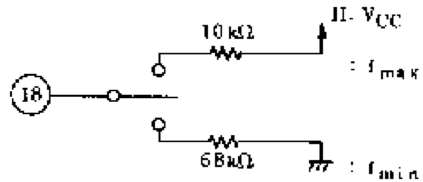
Deflection Stage: Test Circuit 3

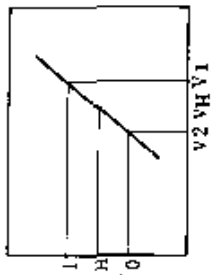
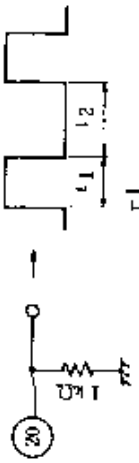
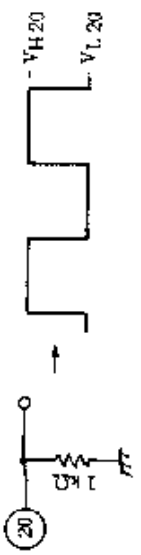
NOTE	CHARACTERISTIC	SYMBOL	TEST CONDITION SW3	SW4	SW5	TP13B	TEST METHOD
43	Sync. Sepn. Input Current Sensitivity	I_{TN16}	OFF	ON	ON	GND	Measure the current flows into #16 when signal frequency at TP13A changes into 268.25H from 353H.
44	H. AFC Phase Detector Current	I_{DET}	OFF	OFF	ON		(1) Measure DC voltage at #18 with no component, and apply that voltage to #18 with 1kΩ. (2) Measure V1, I_{DET}=V1÷1kΩ.

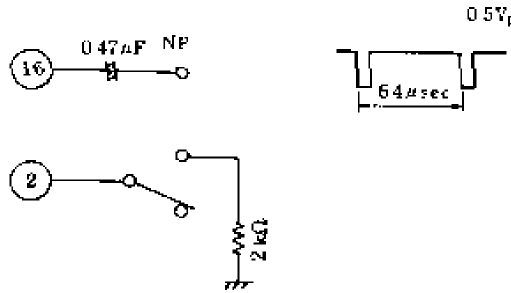
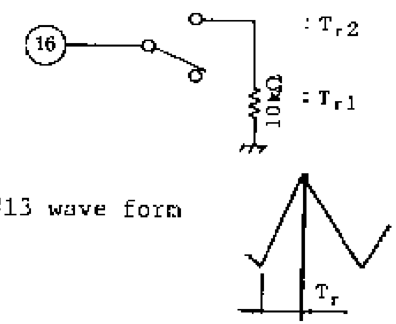


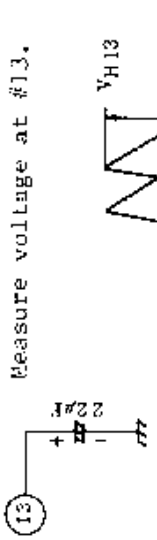
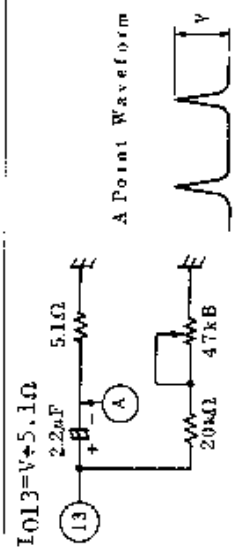
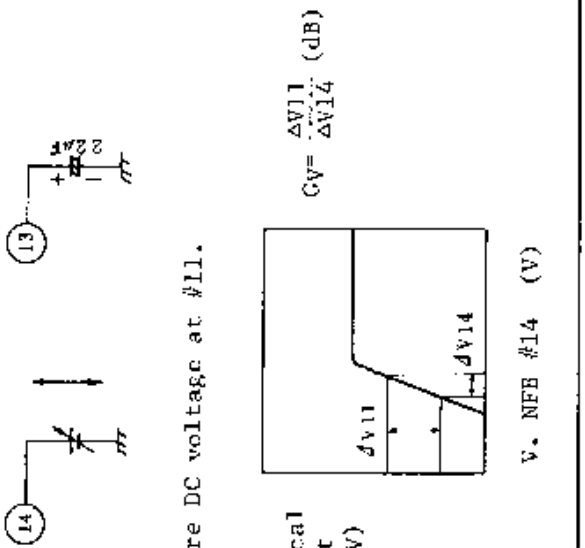


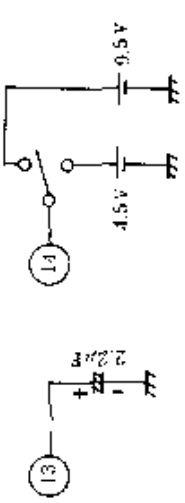
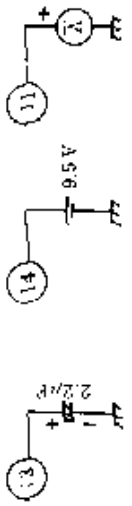
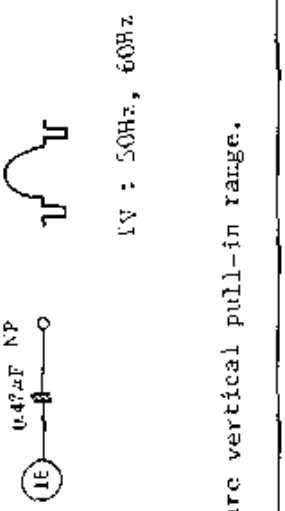


NOTE	CHARACTERISTIC	SYMBOL	TEST CONDITION SW3	SW4	SW5		TEST METHOD
45	H. AFC Masking Period	TG018	OFF	ON	ON		 Measure H. AFC masking period at #18.
46	32fH VCO Starting Voltage	VON	OFF	ON	ON		 Measure DC voltage at #21 when 32fH VCO starts, while V_{CC}=0V.
47	H. Output Starting Voltage	VON20	OFF	ON	ON		 Measure DC voltage at #21 when H. out starts, while V_{CC}=0V.
SL	Horizontal Free-running Frequency	f_o	OFF	ON	ON		(1) Sync. Sepa. In : no signal (2) Measure signal frequency at #20.
49	Horizontal Frequency Control Range	f_{max} f_{min}	OFF	ON	ON		 Measure signal frequencies f_{max} and f_{min} at #20.

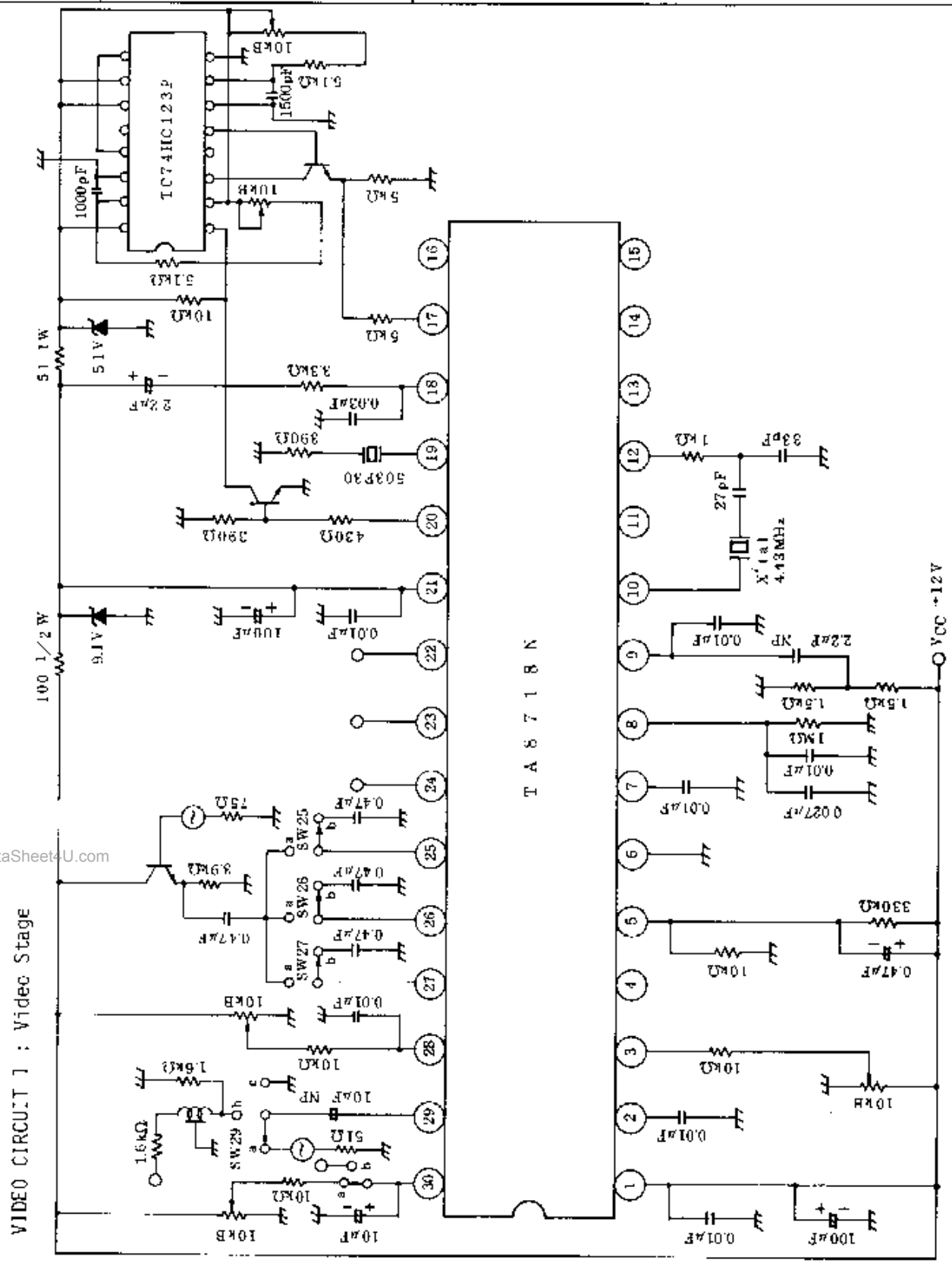
NOTE	CHARACTERISTIC	SYMBOL	TEST CONDITION SW3	SW4	SW5	V.R5	TEST METHOD
50	Horizontal Frequency Control Sensitivity	H	OFF	ON	ON	-	(1) Apply DC voltage at #18 and adjust the voltage so that the output frequency at #20 becomes 15.625kHz. (V18=VH) (2) Change the voltage at #18 by ±0.1V and measure the output frequency at #20. 
51	H. Output Duty-Cycle	T20	OFF	ON	ON	-	AFC Filter #18 (V)  T20 = t1 / t1+t2 × 100 (%)
52	H. Output Level	VH20 VL20	OFF	ON	ON	-	

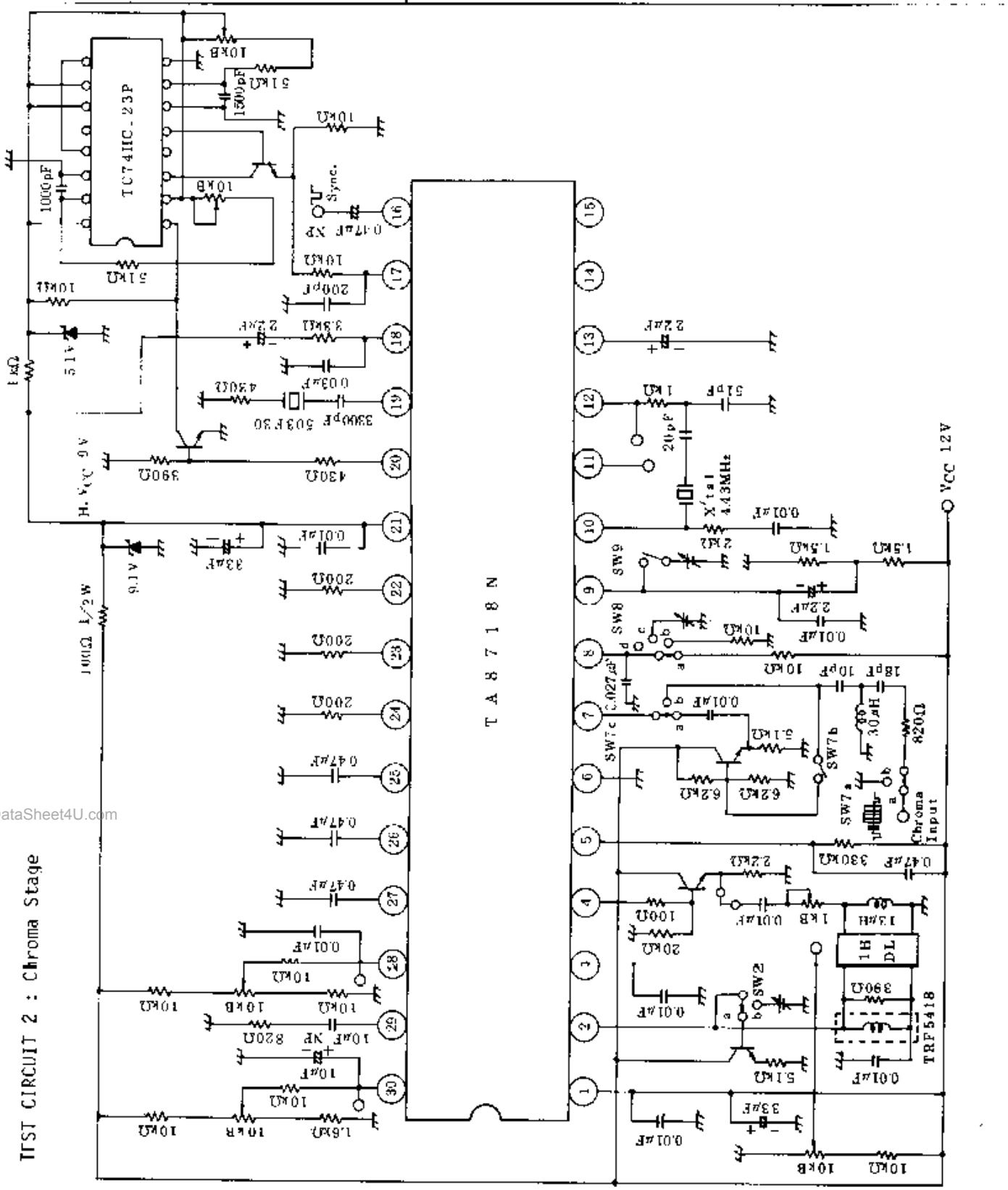
NOTE	CHARACTERISTIC	SYMBOL	TEST CONDITION SW3	SW4	SW5	V.R5	TEST METHOD
53	Horizontal Phase Adjustment Range	ΔG15	ON	ON	ON	Max. → Min.	 (1) Vary V.R.5 from max. to min. (2) Measure change of pulse timing at #17 against #16 signal.
54	Horizontal/ Phase Shift with 50/60 Switching	G17	OFF	ON	ON		 Measure change of pulse timing at #17 against #16 signal.
55	Vertical Retrace Pulse Period	T_{r1} T_{r2}	OFF	ON	ON		 #13 wave form

NOTE	CHARACTERISTIC	SYMBOL	TEST CONDITION SW3	SW4	SW5	TEST METHOD
56	Peak Voltage of Ramp Wave	V_{H13}	OFF	ON	ON	Measure voltage at #13. 
57	Ramp Output Current	I_{O13}	OFF	ON	ON	I_{O13}=V÷5.1Ω 
58	Vertical Amplifier Gain	Gv	OFF	ON	ON	Measure DC voltage at #11. 

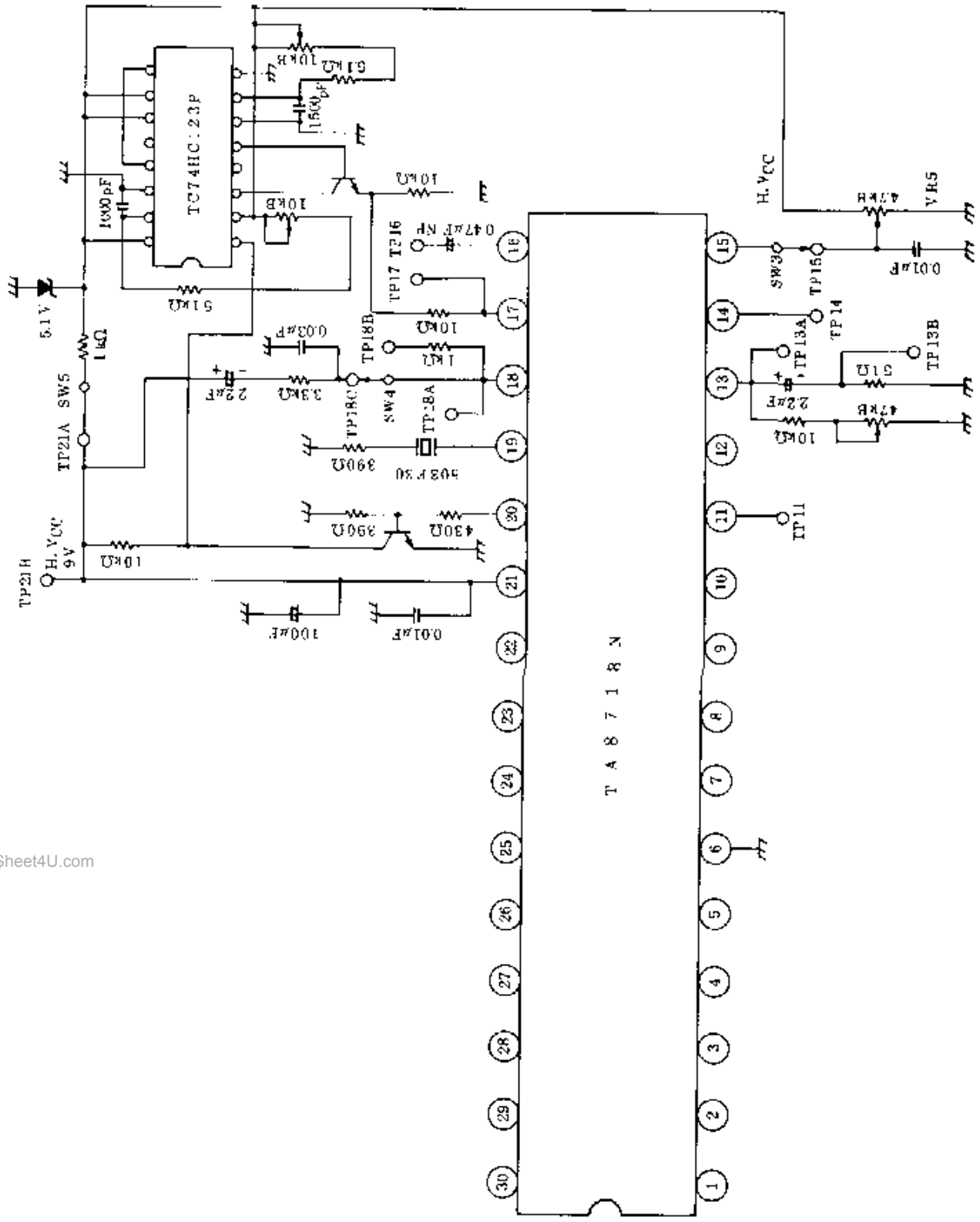
NOTE	CHARACTERISTIC	SYMBOL	TEST CONDITION SW3	SW4	SW5	TEST METHOD
59	Vertical Output Maximum Voltage	VH11	OFF	ON	ON	 Measure DC voltage at #11.
60	Vertical Output Minimum Voltage	VL11				
61	Vertical Output Current	IOL1		ON	OFF	 Measure output current at #11.
62	Vertical Pull-in Range 50Hz	fPV1				
		fPV2		ON	ON	
63	60Hz	fPV3				
		fPV4				

1V : 50Hz, 60Hz
Measure vertical pull-in range.



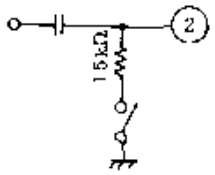
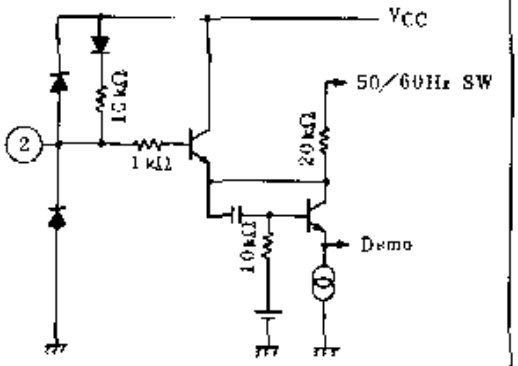
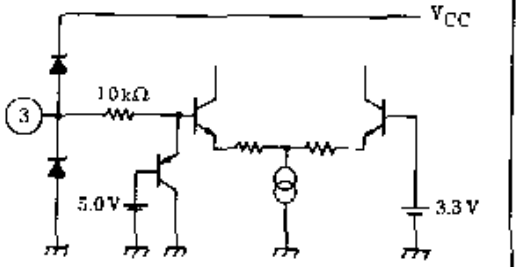
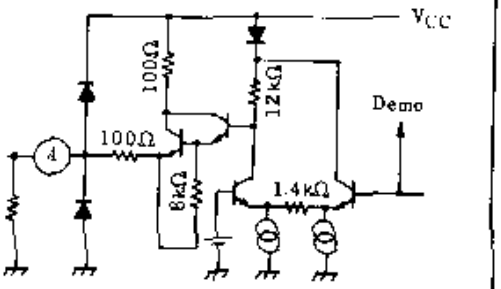
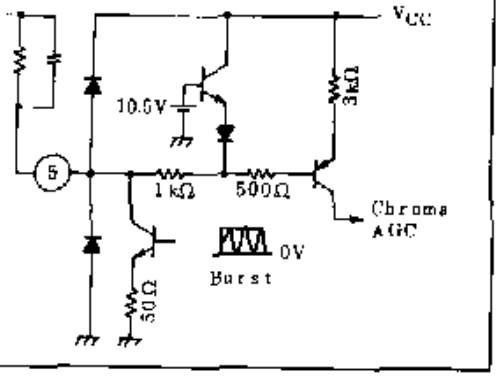


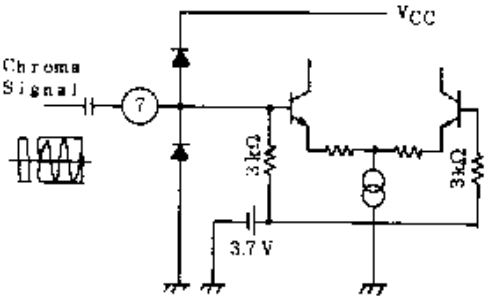
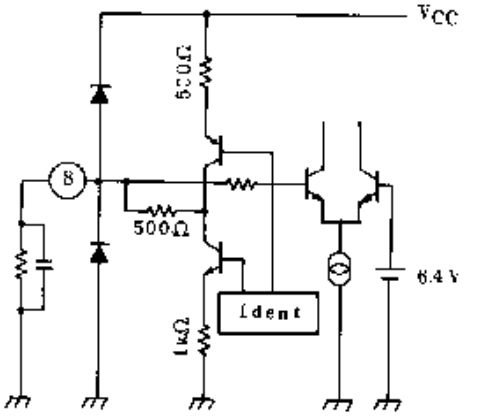
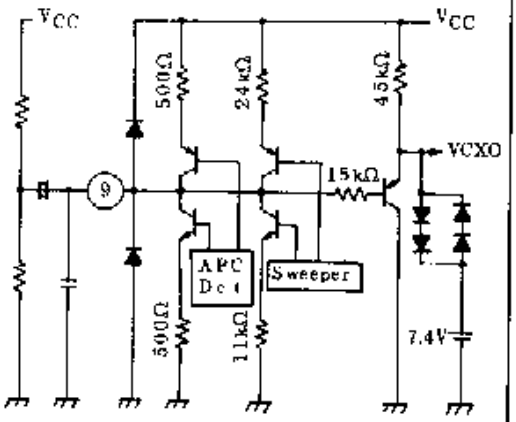
TEST CIRCUIT 2 : Chroma Stage

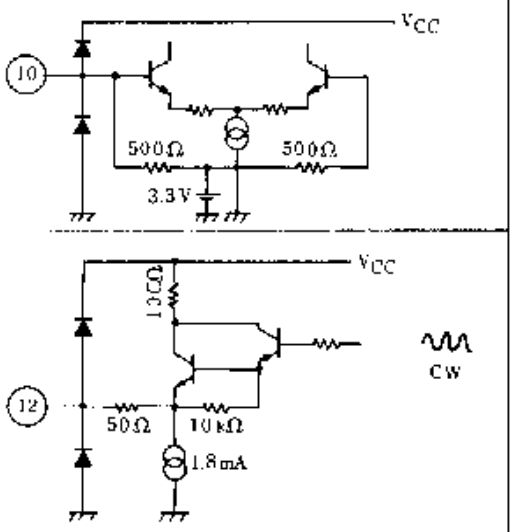
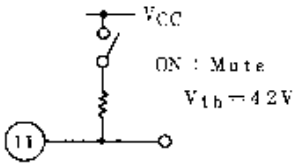
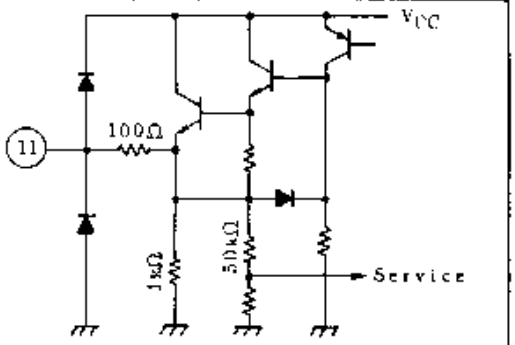
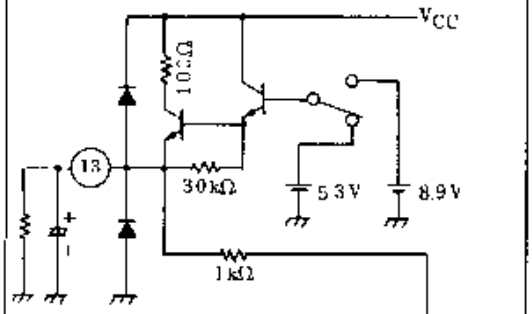
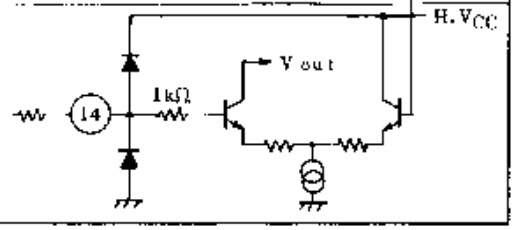


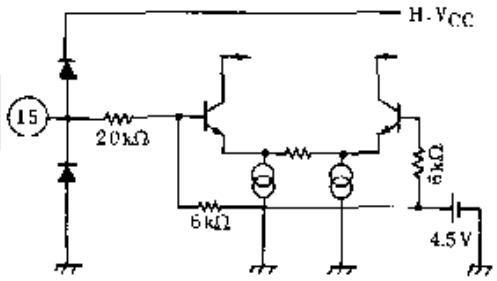
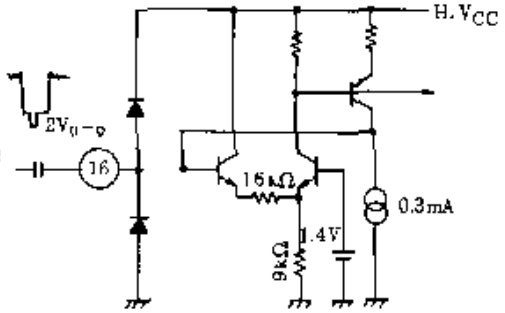
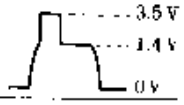
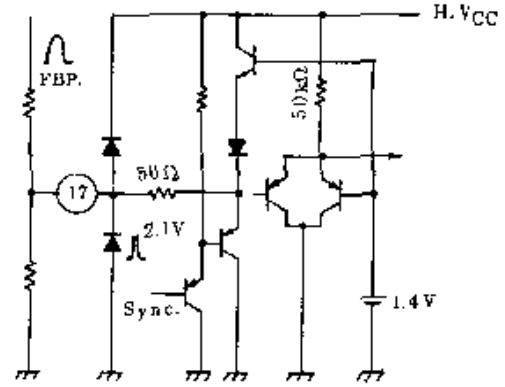
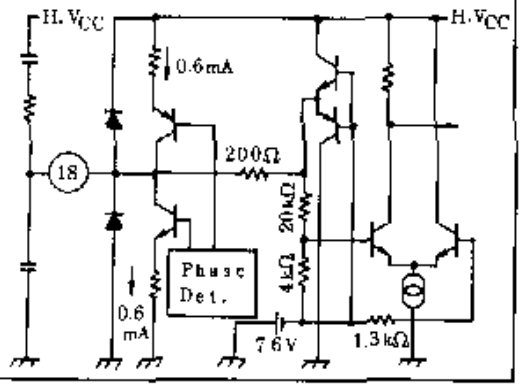
TEST CIRCUIT 3 : Deflection Stage

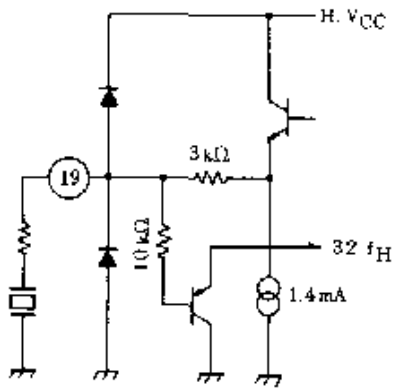
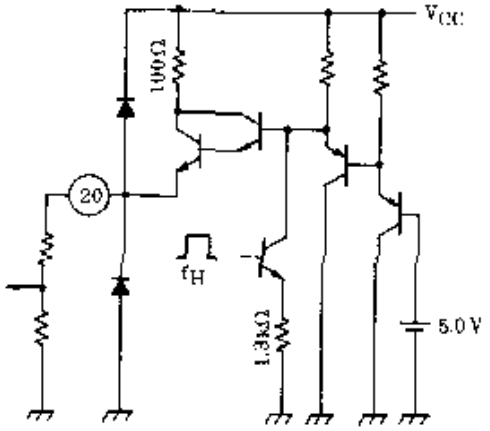
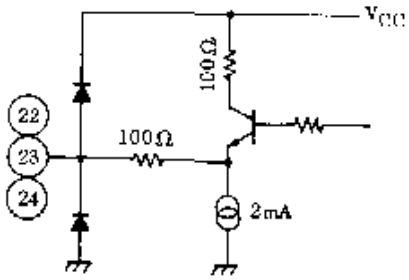
TERMINAL FUNCTION AND INTERNAL INTERFACE (V_{CC}=12V, H.V_{CC}=9V)

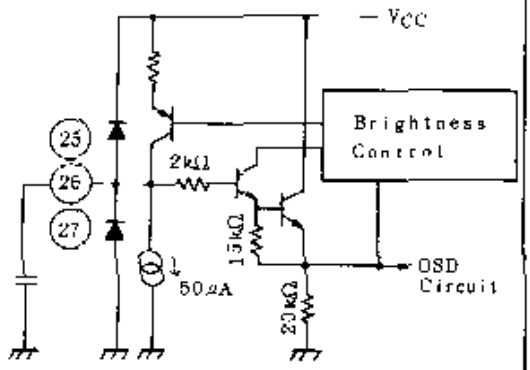
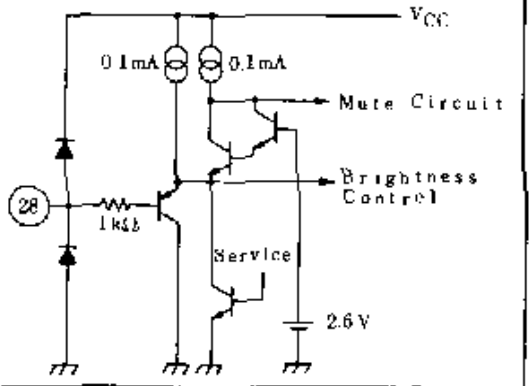
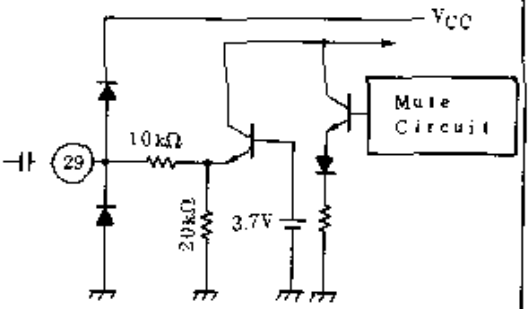
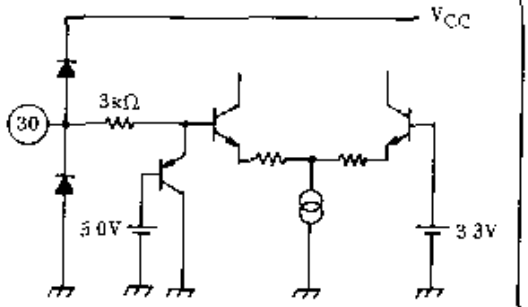
No.	TERMINAL	FUNCTION	INTERFACE
1	V_{CC}	Video and Chroma stage V_{CC}=12V(Typ.)	
2	DLin	An input terminal for 1H delayed chroma signal and a select SW for vertical frequency (50Hz or 60Hz) 	
3	Color	Color control terminal	
4	DLout	An output terminal for chroma signal to drive 1H glass delay line. A delay line of -16dB loss should be used.	
5	ACC Filter	ACC filter capacitance is connected.	

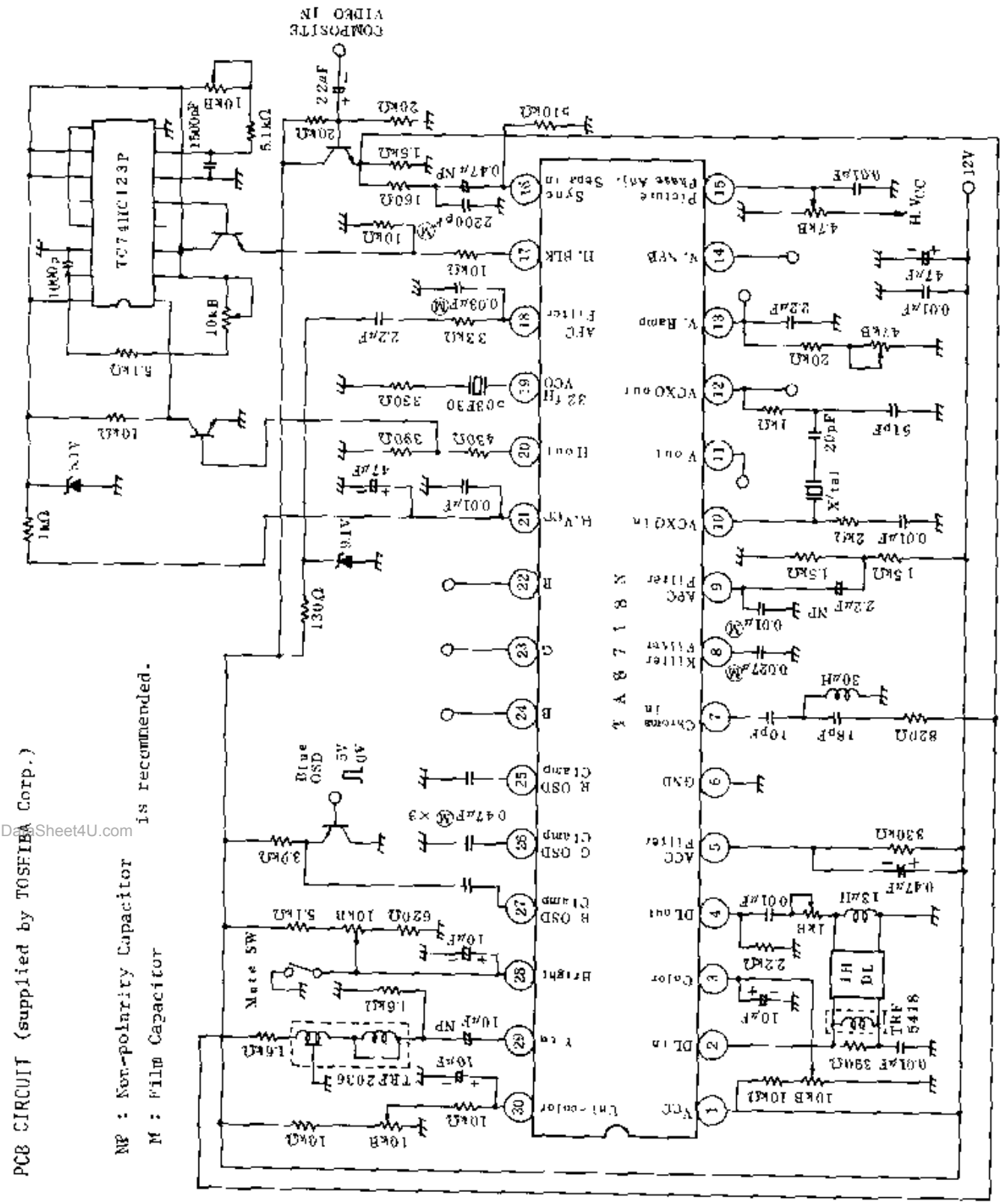
No.	TERMINAL	FUNCTION	INTERFACE
6	GND	Video, Chroma and Deflection stage GND	
7	Chroma in	An input terminal for chroma signal. Typical Burst level is 100mVp-p.	
8	Killer Filter	Killer ident filter capacitance is connected. The killer threshold is 6.4V typ. (In the B/W Mode, this terminal voltage is lower than this threshold voltage)	
9	APC Filter	APC filter capacitance is connected.	

No.	TERMINAL	FUNCTION	INTERFACE
10 12	VCXOin VCXOout	A f_{sc} X'tal is connected between #10 and #12. #12 is a drive output and #10 is an input.	
11	Vout	An output terminal for a vertical deflection drive circuit. This terminal also has Service SW function. 	
13	V.Ramp	The vertical ramp wave is generated at this terminal. During retrace period, an external capacitor is charged by an internal current source, then, during trace period, the external capacitor is discharged by an external resistor. The V.ramp voltage is subjected to the horizontal V_{CC}(7.6V(Typ) when H.V_{CC}=9V)	
14	V.XFB	An input terminal for AC and DC negative feedback of vertical deflection drive circuit.	

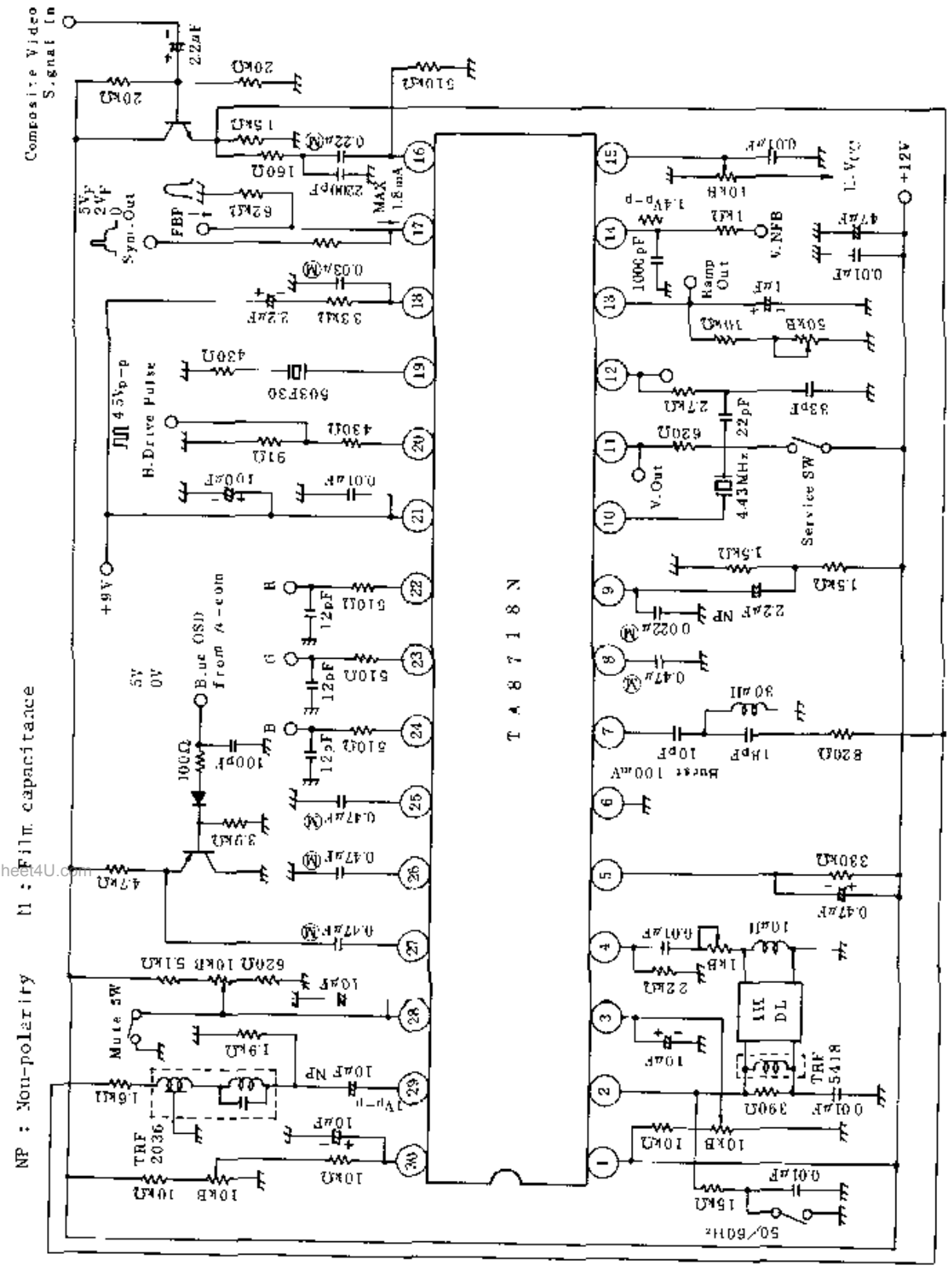
No.	TERMINAL	FUNCTION	INTERFACE
15	Horizontal Phase adj.	Horizontal output pulse phase is connected by the DC voltage applied #15. The adjustable range is 2μsec.	
16	Sync. Sep. in	An input terminal for a composite sync. signal. The sync. signal separated at this terminal can be observed at terminal #17.	
17	H. Blank	An input terminal of the F.B.P for H.Blanking and PAL SW driving pulse. Blanking threshould voltage is 1.4V (Typ.). The sync pulse output can be obtained at this terminal for a station detector. 	
18	AFC Filter	AFC filter capacitance is connected.	

No.	TERMINAL	FUNCTION	INTERFACE
19	32f_H VCO	An output terminal for 32f_H ceramic oscillator driver.	
20	Hout	An emitter follower output terminal for Horizontal drive pulse. Duty cycle is 43%.	
21	H.V_{CC}	V_{CC} for a horizontal deflection stage H.V_{CC}=9V(Typ.) External zener diode is required.	
22 23 24	Rout Gout Bout	An output terminal for R.C.B primary color signals.	

No.	TERMINAL	FUNCTION	INTERFACE
25 26 27	R Clamp/OSD in G Clamp/OSD in B Clamp/OSD in	Clamp capacitor for DC restration is connected. An On-Screen-Display signal can be applied through a coupling capacitance (TTL level).	
28	Brightness	Brightness control terminal. If this terminal is Low (<0.3V), R.G.B output signals are muted and the output DC voltage is clamped to 3.2V.	
29	Yin	This is an input terminal for Video signal.	
30	Uni-Color	Uni-Color control terminal. A luminance signal amplitude and a chrominance signal amplitude are controlled Simultaneously by the DC voltage applied at #30.	



APPLICATION CIRCUIT



NP : Non-polarity M : Film capacitance

1H Delay Line Adjustment Procedure

(1) #29: open

(2) #28: 5V

(3) #3: max.

(4) Adjust contrast control to set Red and Blue outputs, at #22 and #24 respectively, less than 4Vp-p, so that the ACL function does not work. Under this condition, R-Y and B-Y signals come out from #22 and #24.

(5) Apply Philips color pattern signal at #7, the burst level shold be set to 100mVp-p.

(6) Adjust a volume and a tank-coil (TRF5418) so as to minimize color at Anti-Pal region and Venetian Blind at color bar.